Designing an OTA for maximal gain

A project report submitted for
EC383:Mini Project in VLSI Design

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December 3, 2020

ACKNOWLEDGEMENTS

We would like to sincerely thank Dr. MS Bhat sir for his guidance in this project. He has been encouraging and motivating throughout and has been very approachable everytime we needed his support.

We would also like to thank prof. Nikhil K S and prof. Sushil Kumar Pandey for their feedback which has helped us gain a new perspective towards this project.

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Chapter 1

1.1. Introduction

In this project, we have tried to understand the significance and working of the Operational Transconductance Amplifier, commonly known as OTA. OTA is used for various applications, some of them being, Data converters, Active filters, frequency oscillators, and so on. In all these applications the gain of the OTA is a major factor for their performance. Here we specifically focus on the specifications required for that of a data convertor. For example , the delta sigma ADC requires a switch based integrator which needs a high gain in order to get a good resolution. We explore different topologies in order to achieve a gain as high as 100dB.

1.2 Motivation

Operational Transconductance Amplifier (OTA) is an integral part of many analog and mixed signal systems. The OTA is the versatile building block of any analog processing system. Designing these building blocks in terms of gain, power consumption and gain bandwidth product efficiently is still a challenging task. In this report, various single ended and fully differential OTA' s are discussed and their performances are compared with each other.

1.3 Objective

Main objective of this project is to achieve a very high gain OTA of about 100dB for ADC applications.

1.4 Overview

An Operational Transconductance Amplifier is to be implemented which typically provides a very high gain. We have discussed different OTA topologies from simple differential amplifiers to Folded cascode theoretically, along with simulation results. All simulations are done in LTSPICE. Differences between all these topologies are observed in terms of gain, swing limits and other specific parameters.

Chapter 2

2.1 OTA Fundamentals

The OTA is a transconductance device in which the input voltage controls the output current. An OTA is basically an operational amplifier (opamp) without an output buffer. The characteristic feature of an ideal transconductance amplifier is that it has infinite input and output resistances.

2.1.1 Performance Parameters

There are various parameters to validate the performance of the OTA. The important parameters that help in the designing of OTA are gain, slew rate, power dissipation, common mode rejection ratio, power supply rejection ratio.

Gain:

The gain is a measure of the ability of an amplifier to increase the power or amplitude of a signal from the input to the output. It is usually defined as the mean ratio of the signal output of a system to the signal input of the same system. It may also be defined on a logarithmic scale, in terms of the decimal logarithm of the same ratio (dB gain). DC gain can be improved by increasing the transconductance of the input transistors or the output impedance. The open loop gain of an amplifier determines the precision of the feedback system. A high open loop gain is necessary to suppress nonlinearity.

Power dissipation:

The power dissipation is easily calculated from the supply voltage and current when the output is open circuited. When current flows into a load, it is easy to calculate the total dissipation and then subtract the load dissipation to obtain the device dissipation. When the load capacitance is increased, both the slew rate and the unity gain frequency of the OTA circuit are reduced. To maintain a constant settling behavior, the power consumption of the OTA must be increased linearly with an increase in the load capacitance.

2.2 Different Topologies

We would like to start our discussion with a simple differential amplifier to a complex OTA.

2.2.1. Simple Fully Differential Amplifier with Current Source Load

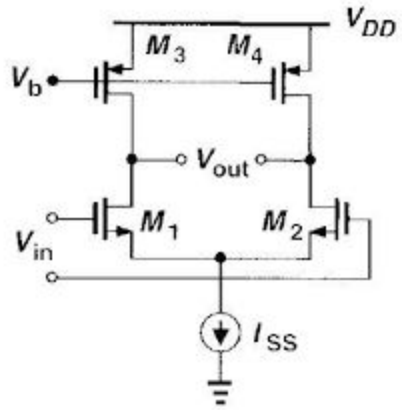


Fig1. Schematic of two ended differential amplifier with current source load

In 2.2.2 to obtain a higher gain, the passive resistance Rd, can be replaced with the current source as shown in the above figure. Here the current sources are realized with PMOS transistors M3 and M4 , and Vb is the dc bias voltage that ensures that Q3 and Q4 each conducts a current equal to Iss/2. The differential voltage gain can be found from the differential half circuit as,

Av = gm1 (ro2 || ro4)

2.2.2. Single stage OTA with current mirror load

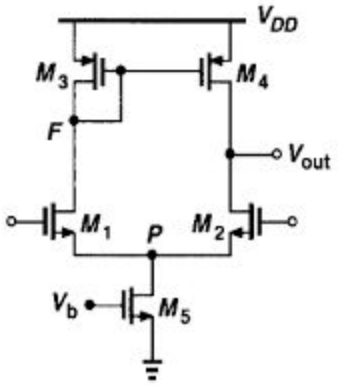


Fig2. Schematic of single ended differential amplifier with active load

In 2.2.3, the attempt is to obtain output at one output terminal. In the previous case, Vout1 was calculated in terms of current with respect to M1 and Vout2 in terms of current with respect to M2. But now we are intended for one output terminal, so we copy the current from M1 using the current mirror. This ensures that current of M1 also contributes at the output terminal along with M2 current.

2.2.3. Telescopic OTA

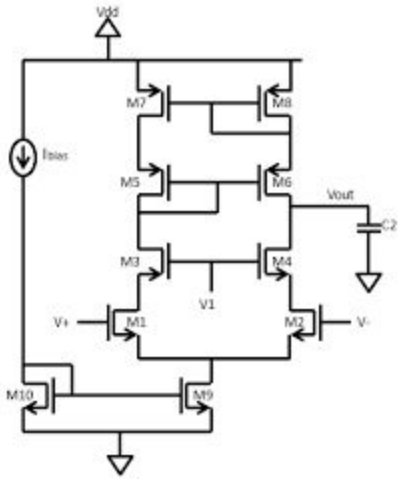


Fig3. Schematic of telescopic OTA

The Telescopic OTA uses an input differential pair along with Cascode current mirror. The transistors M5, M6, M7 and M8 form a Cascode Current Mirror. The cascode device in the circuit helps to achieve high gain and reduces the noise contributed by the bias transistors. The circuit gain is given as

Av=gm1 [(gm4.rds4.rds2) || (gm6.rds6.rds8)]

Swing limit obtained in this configuration is less to achieve a high swing limit along with gain; we prefer Folded cascode.

2.4.4 Folded OTA

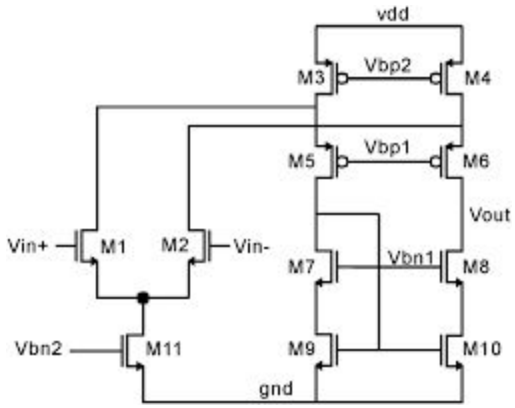


Fig4. Schematic of Folded OTA

Folded cascode is a very well known OTA topology which promises very high gain along with favourable swing limits. One can increase the gain by addition of cascode stages. Folded cascode involves a differential amplifier and telescopic amplifier within it. Lot of research has been done in this area to improvise specific parameters of folded cascode OTA. Gain of Folded cascode is as follows:

Av=gm1. Rout

Where Rout = { [gm6 .rds6 (rds4 || rds2)] || [gm8 . rds8. Rds10] }

2.3. Simulation and Analysis

All the simulations of OTA are carried out in LTspice using bsim4 180nm technology file with power supply 1.8V. In order to obtain higher gain transistors are sized as per requirement. DC analysis is done to ensure that transistors are in saturation. Using Transient analysis we have calculated gain and observed swing of output waveform. Threshold voltage for nmos is 0.366V and pmos is 0.39V (as per model file).

We start off with a simple fully differential amplifier configuration in order to understand the steps of analysis.

2.3.1 DIFFERENTIAL AMPLIFIER WITH ACTIVE LOAD

In order to improve the gain from the circuit compared to a resistive load circuit. We implement the loads using a pmos model instead of a resistor, the inbuilt output resistance of a pmos in saturation is larger than a typical value of Rd. We cannot increase Rd in the previous circuit because, else the transistors will slip into cutoff and there won't be any amplification. Hence we go for this model.
In this model we try to understand the steps of analysis involved while deal

In this circuit, we have biased the pmos and tail current source using a current mirror as shown below.

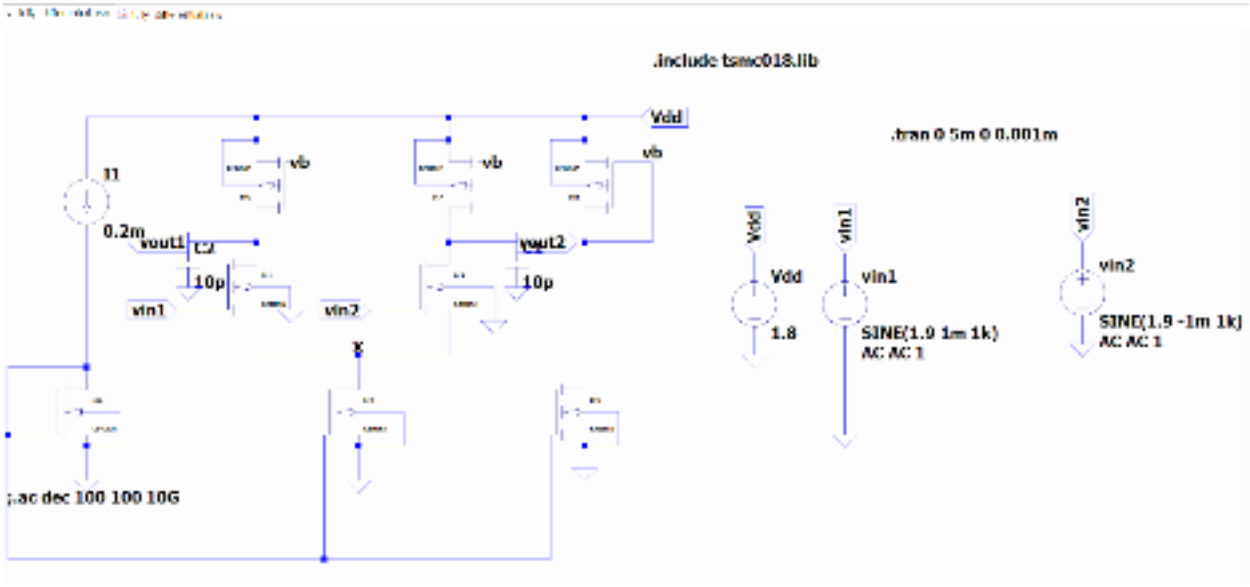


Fig5. LTspice schematic of fully differential amplifier with active load

DC analysis:

Steps used to Bias the circuit:

1. For this we have used 180nm technology models of the pmos(named as CMOSP) and nmos mosfets(named as CMOSN). From the model files, we have found that the VTH0 for nmos is 0.36 and VTH0 for pmos id 0.39. We also know the process transconductance parameters as 170.7uV/A^2 and 36 uV/A^2. Taking an overdrive of 0.1v ,vdd=1.8v ,vss=0v and tail current of 0.2mA we calculate the width needed for properly biasing the transistors.

2. We start off with the width of the M1 transistor and its value comes out to be 10.5um given we are taking the length to be the feature size, i.e 180nm. And from the transconductance ratio of pmos to nmos we find the widths of the pmos should be around 4.7 times the nmos widths in order to pass the same current (0.1mA), giving a value of 50um.

3. And for the current mirror circuit part depending on the current required on the particular branch we decide the widths of the nmos transistors. For the tail current since 0.2mA flows, that is twice the current from the previous nmos, we double its width. I.e 21um. And the

ideal current source we have used gives a current of 0.2mA, the nmos in that branch should also be 21um in length so that it gets copied properly to the tail current. And for biasing the pmos transistors we need to copy only 0.1mA from the ideal source so we use 10.5um at the nmos and as usual 50um as the pmos.

4. We make a copy of the current source using nmos m5 and then use another current mirror bias the pmos transistor in the differential amplifier. We also use a load capacitance of 10pf at the output.

5. We check for operating point by doing the DC analysis and seeing where the input and output plot meet, this is where we would want to bias the common mode input in order to get maximum differential gain. This occurs at 1.9 volts of input.

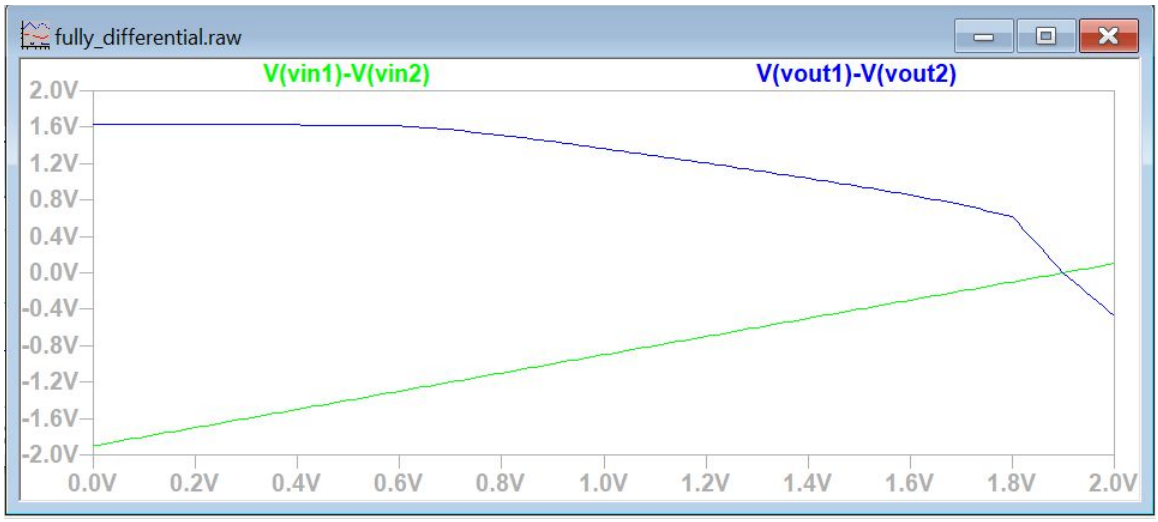
6. We also calculate the input and output swings we get from this calculation theoretically by checking for saturation conditions of all the transistors. After doing this we get a range of around 0.9 to 2.1 volts. Setting the input to 1.9 volts offset we see the voltages and currents at this operating point, just to make sure all the transistors are conducting. We run the .op in ltspice to do that and we the following text file:

```
V(vout1): 1.43969   voltage
V(vin1):  1.9       voltage
V(vout2): 1.43969   voltage
V(vin2):  1.9       voltage
V(vdd):   1.8       voltage
Id(M8):   -0.000130161      device_current
Id(M7):   -0.000121519      device_current
Id(M6):   -0.000121519      device_current
Id(M5):   0.000130161       device_current
Id(M4):   0.0002            device_current
Id(M3):   0.000243037       device_current
Id(M2):   0.000121519       device_current
Id(M1):   0.000121519       device_current
I(Vdd):   -0.000573199      device_current
```

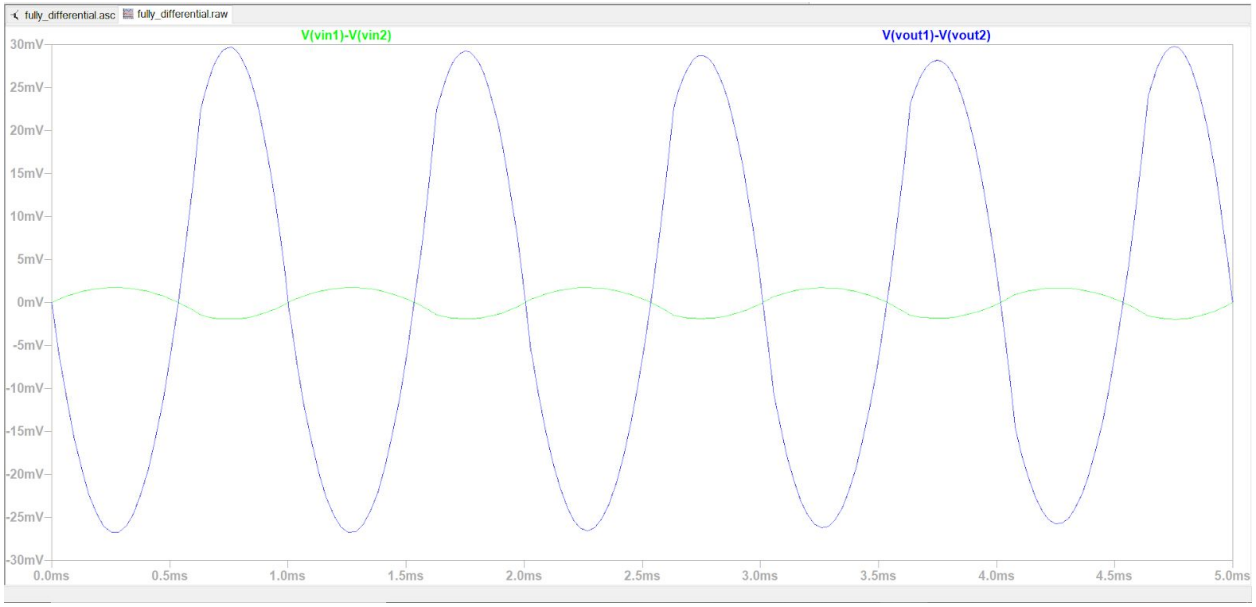
From this we see that all the transistors are working and there is approximately the same drain current passing through these transistors as expected.

Now we ride a 1m volt signal over this DC offset and do transient analysis, to check for gain.

DC analysis:



Transient analysis:



From the above schematic we see that, for an input peak to peak (vin1-vin2) of 3.63 millivolts we get an output peak to peak (vout2-vout2) of 54.98 millivolts. That is it has a gain of around 15.14 and a phase difference of 180 degrees. (because it is essentially designed out of a common source

amplifier). When calculated in dB, we get around 23.6dB gain from this amplifier.

Parameters	Single Stage OTA
Supply voltage(V)	1.8
Load capacitance(pF)	10
Bias current(mA)	0.3
Gain(dB)	23.6

Table1. Design specifications of Fully differential Amplifier

2.3.2. SINGLE STAGE OTA WITH CURRENT MIRROR LOAD

A single stage OTA is implemented whose schematic is shown in Fig6. Transistors are sized so as to make sure that all transistors are in saturation.

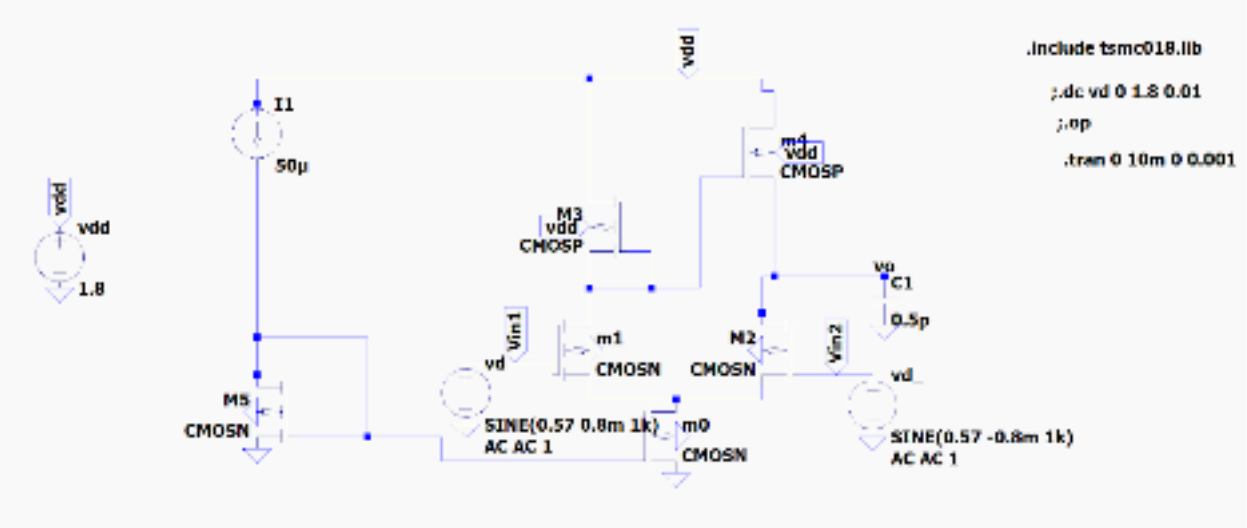


Fig6. LTspice schematic of single ended OTA

The single stage OTA here is a single ended OTA, therefore the load is a current mirror load. Transistor m1 and M2 are the transistors across which the differential input is applied. Transistor m0 is the tail current transistor which is biased by the current mirror configuration of the M5 transistor and therefore current of approximately 50uA is copied from the ideal current source.

Parameters	Single Stage OTA
Supply voltage(V)	1.8
Load capacitance(pF)	0.5
Bias current(uA)	50
Gain(dB)	28.9
Power Dissipation(uW)	132.03

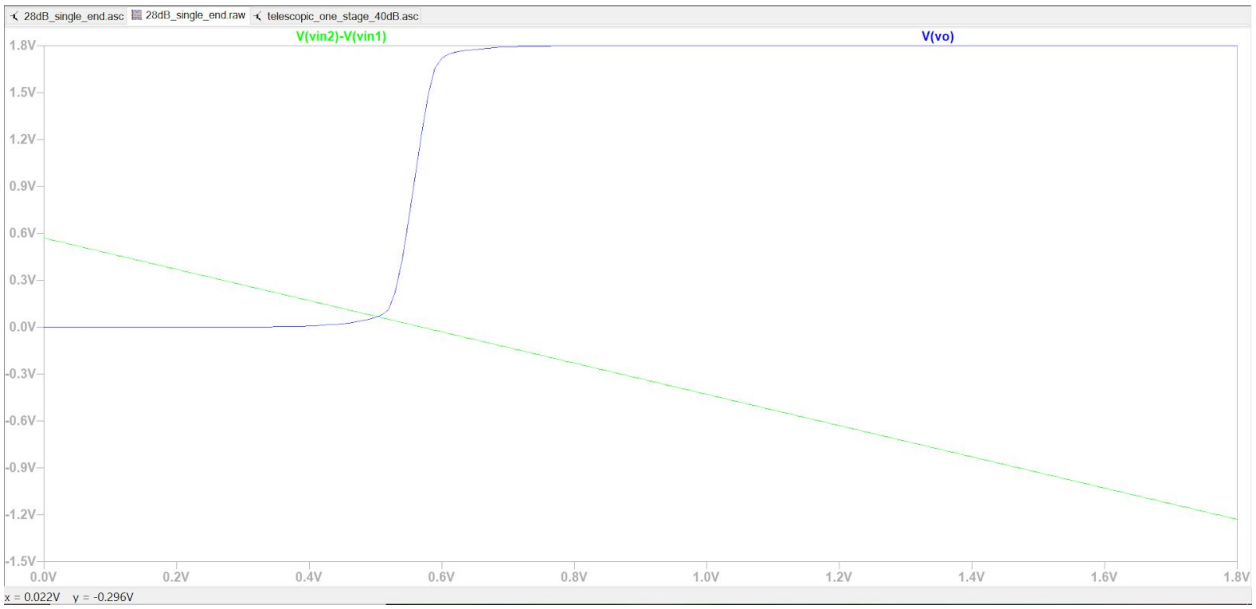
Table2. Design specifications of Single ended OTA

Transistor Sizing:

Transistor	MOSFET TYPE	L	W
M1, M2	NMOS	0.18um	3um
M3, M4	PMOS	0.18um	8um
M5, M0	NMOS	0.18um	5um

Table3. Transistor sizes of single stage OTA

DC Analysis:

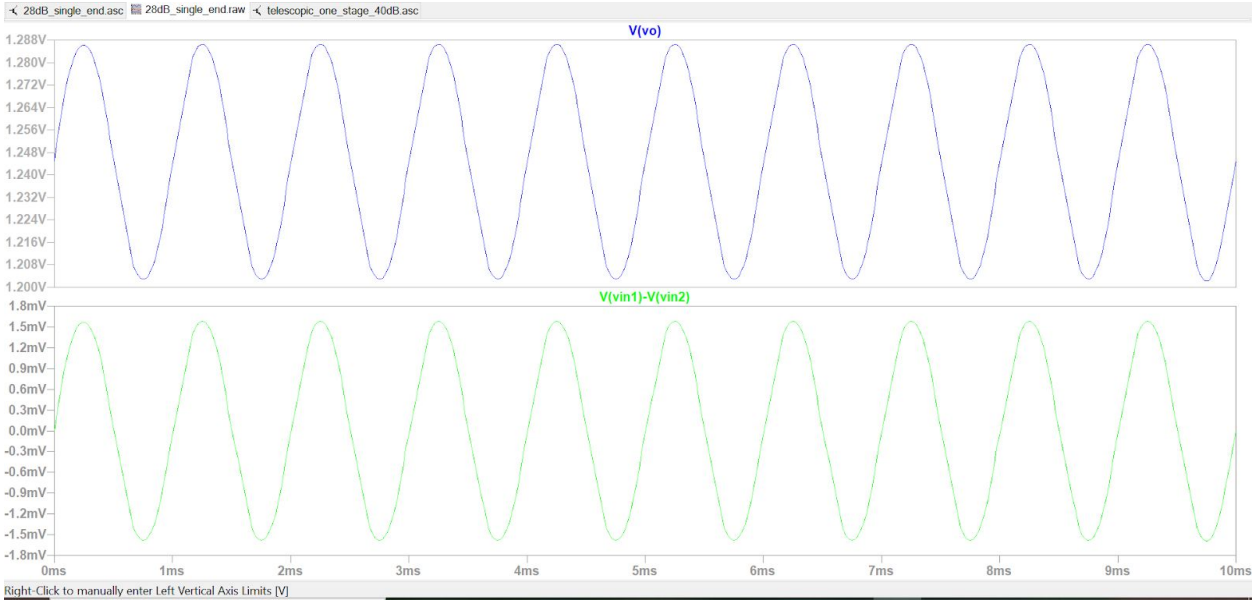


On doing Dc analysis and biasing the voltages accordingly we find that if we bias the input around 0.5 to 0.6 volts we can get maximal gain. We run the operating point, .op command and check if all the transistors are in saturation and if all the currents match the expected theoretical values.

V(vin1):	0.57	voltage
V(vin2):	0.57	voltage
V(vdd):	1.8	voltage
V(vo):	1.24503	voltage
Id(M3):	1.16788e-005	device_current
Id(M4):	1.16788e-005	device_current
Id(M5):	5e-005	device_current
Id(M2):	1.16766e-005	device_current
Id(M1):	1.16766e-005	device_current
Id(M0):	2.33532e-005	device_current
I(I1):	5e-005	device_current
I(Vdd):	-7.33532e-005	device_current

During current mirror copying at transistor m0, due to the approximate sizing of transistors, instead of copying a current of 50uA, it has copied 40uA and has split equally in the two branches. And all the mosfets are in saturation as expected. Power consumption of the circuit is P = Vdd*(Id(M0) + Id(M5)) = 132.03uW.

Transient Analysis:



From the above plot we can observe that input peak to peak voltage is 3mV and output peak to peak voltage is 0.084V. We obtained a gain of 28.9dB.

2.3.3 SINGLE STAGE TELESCOPIC OTA

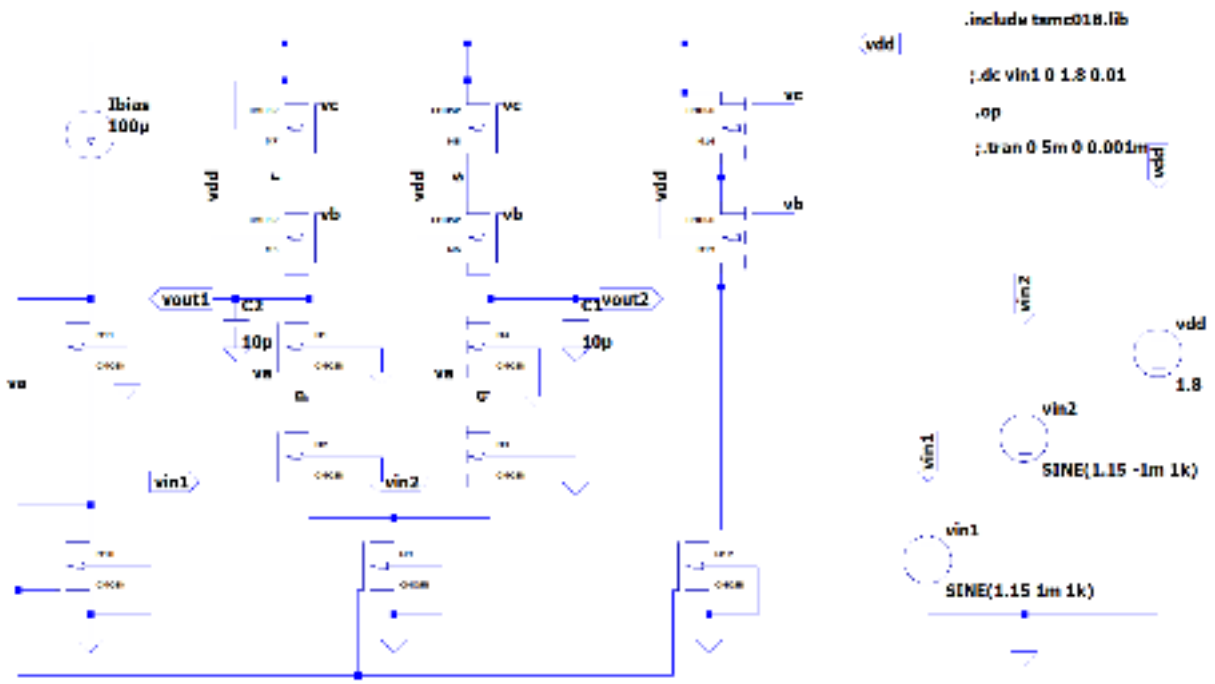


Fig7. LTspice schematic of a single stage telescopic OTA

In a telescopic OTA the load is a cascode structure, because of which the output impedance of this topology is much higher and we get a better gain compared to a simple current source load. This is a fully differential amplifier with a bias current equal to 100 microamps which biases the tail current of the telescopic structure. All the nmos substrates are connected to ground and all the pmos substrates are connected to supply voltage. The cascode device in the circuit helps to achieve high gain and reduces the noise contributed by the bias transistors. The circuit gain is given as

$$Av = g_{mN}[(g_{mN}r_{oN}^2)\|(g_{mP}r_{oP}^2)]$$

Where gmN is the transconductance of the NMOS whereas the gmP is the transconductance of the load(pmos) and roN and roP are the intrinsic impedance of the nmos and pmos transistors.

Design parameters:

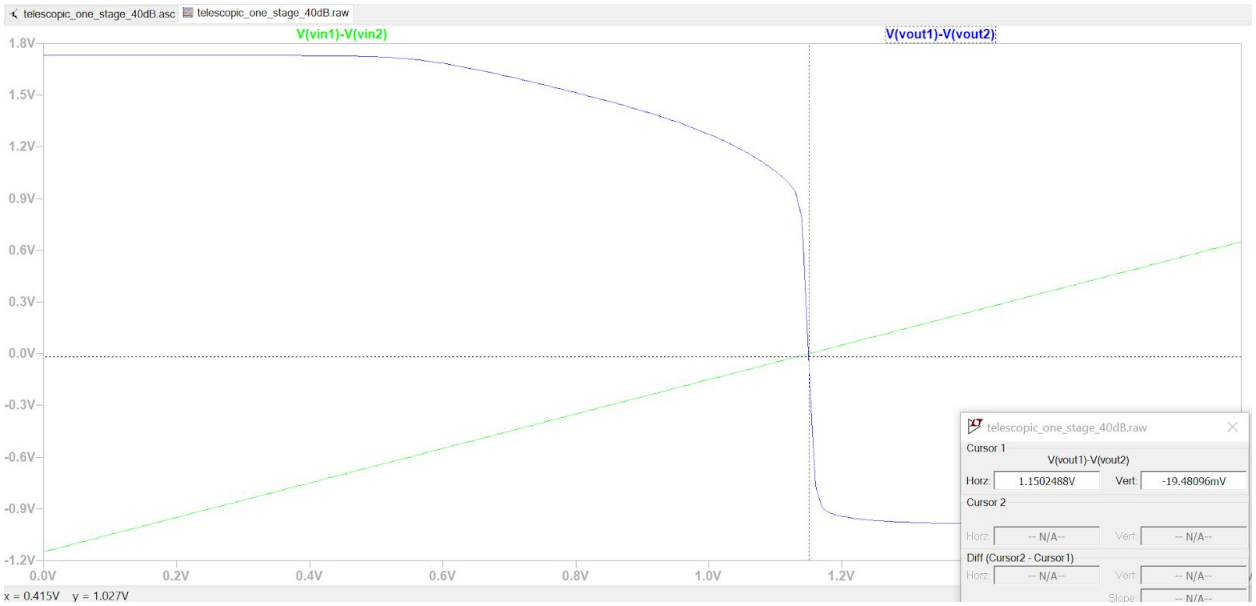
Transistor	Width	Length

M1, M2 , M3, M4	10.6 um	180 nm
M5, M6, M7, M8	50 um	180 nm
M9	21.2um	180 nm
M10, M11, M12	10.6 um	180 nm
M13, M14	50 um	180 nm

Table 4. Transistor sizes of Telescopic OTA

In the above simulation the labels, va,vb and vc are the biasing voltages that result from the current mirror configurations which hold the transistors in saturation. Using the steps given for the analysis we first check out the DC operating point of the circuit.

DC analysis:



As we can see, the input and output curves meet at a point of 1.15 volts. Setting the input common mode at 1.15 volts we can see that we would get a maximal gain from this structure. Now we need to set Vcm at 1.15 volts and check if all transistors are in saturation by checking for the operating point by running the command .op.

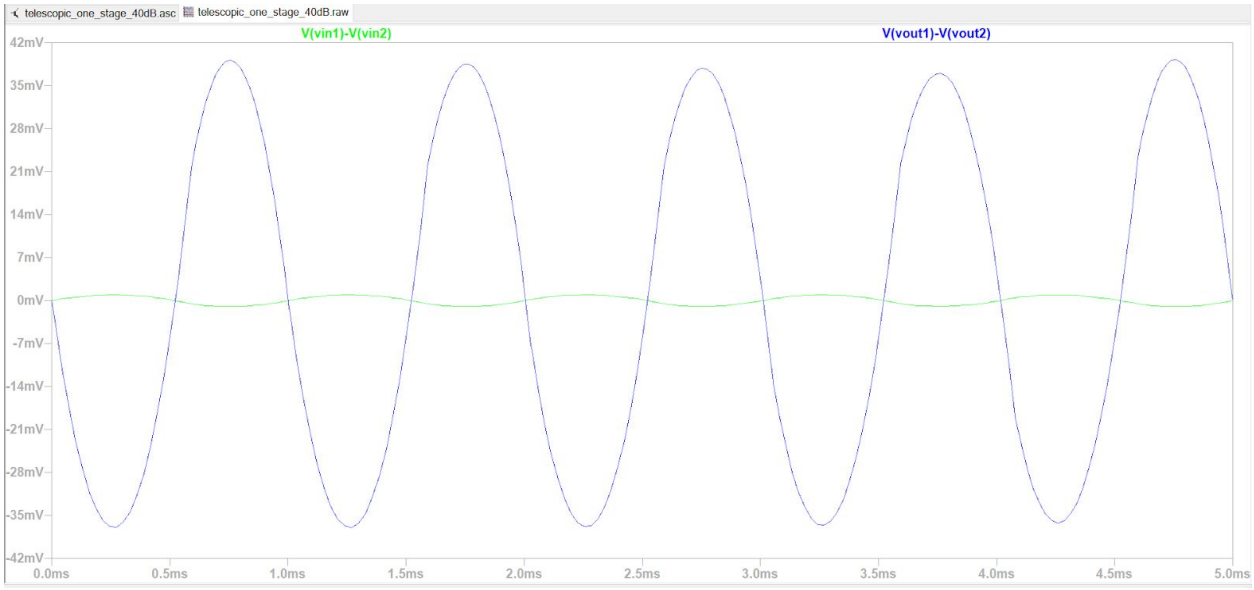
On checking the operating point we find that all the drain currents are close to the expected values. Some of the important currents and voltages from the list are as

follows. Here we list only the drain current because by checking their actual values from expected ones we can tell if the transistor is in saturation or not.

V(vout1):	1.36606	voltage
V(vin1):	1.15	voltage
V(vin2):	1.15	voltage
V(vout2):	1.36606	voltage
Id(M7):	-9.21463e-005	device_current
Id(M14):	-9.62969e-005	device_current
Id(M13):	-9.62969e-005	device_current
Id(M8):	-9.21463e-005	device_current
Id(M6):	-9.2135e-005	device_current
Id(M5):	-9.2135e-005	device_current
Id(M12):	9.62969e-005	device_current
Id(M11):	0.0001	device_current
Id(M10):	0.0001	device_current
Id(M9):	0.000184293	device_current
Id(M4):	9.21463e-005	device_current
Id(M3):	9.21463e-005	device_current
Id(M2):	9.21463e-005	device_current
Id(M1):	9.21463e-005	device_current
I(Ibias):	0.0001	device_current
I(Vdd):	-0.000380589	device_current

Since the bias current is 100uA, and from the width ratios of M9:M10, we need Id(M9) to be twice the bias current, that is 200uA, here we see that is actually 184uA, which is close to the required value, and all the other currents are expected to be around 100uA from the width ratios of their current mirrors and we see that it is around 90-95uA which is pretty close to the theoretical value. The transistors are sized such that they accommodate these currents given that the overdrive value of 0.1volt and threshold values are approximated to 0.4 volts from the model files. The actual values of threshold are little lesser than 0.4 and hence we see that there is a small difference between the theoretical and actual currents in the device. Nevertheless, we analyse the gain for this circuit by plotting the transient response and check if it is higher than a simple current source load as expected.
Power dissipation of the circuit is P = Vdd * (Id(M10) + Id(M9) + Id(M14)) = 685.06uW.

Transient analysis:



This is a fully differential configuration and hence the output is inverted with respect to the input(phase difference of 180 degrees). And they have the same DC level of 0 volts. We can see that the peak-to-peak voltage of 78.28 mvolts at the output for an input peak-to-peak of 1 mvolt. Which accounts to a gain of 37.87dB.

Parameters	Telescopic OTA
Supply voltage(V)	1.8
Load capacitance(pF)	10
Bias current(uA)	100
Gain(dB)	37.87
Power Dissipation(uW)	685.06

Table5. Design specifications of Telescopic OTA

But one of the limitations of the telescopic OTA is that it has a stack size of 5 transistors which reduces the swing at the output. This is because each transistor takes us a good amount of voltage headroom in order to keep itself in saturation. Hence, we go for the folded cascode structure, which has a single stage gain similar to that of a single stage telescopic structure but has a much better output voltage swing.

2.3.4. TWO STAGE FOLDED CASCODE OTA

The figure shown below represents two stage folded cascode where we can achieve higher gain as well as better output swing. The design is self biased in order to avoid the usage of more current mirrors to bias transistors. If we do small signal analysis we observe that the gain of Folded cascode is dependent on the transconductance of M1 and the output resistance. So the strategy to obtain high gain is to increase the parameters which increases output resistance and transconductance of M1.

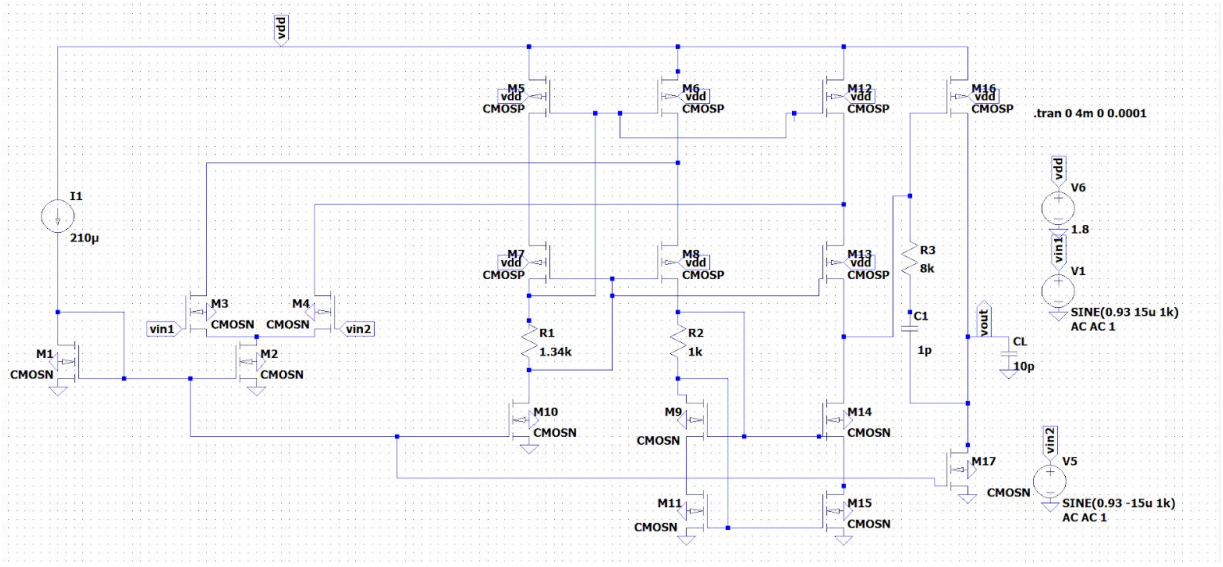


Fig8. LTSpice Schematic of two stage folded cascode OTA

Design parameters:

Transistor	Mosfet Type	L	W
M1, M2	NMOS	0.5u	7u
M3, M4	NMOS	0.5u	50u
M5, M6, M7, M8, M12, M13	PMOS	0.3u	170u
M9, M11, M14, M15	NMOS	0.5u	70u
M10	NMOS	0.5u	9u
M16	PMOS	0.5u	30u

M17	NMOS	0.5u	30u

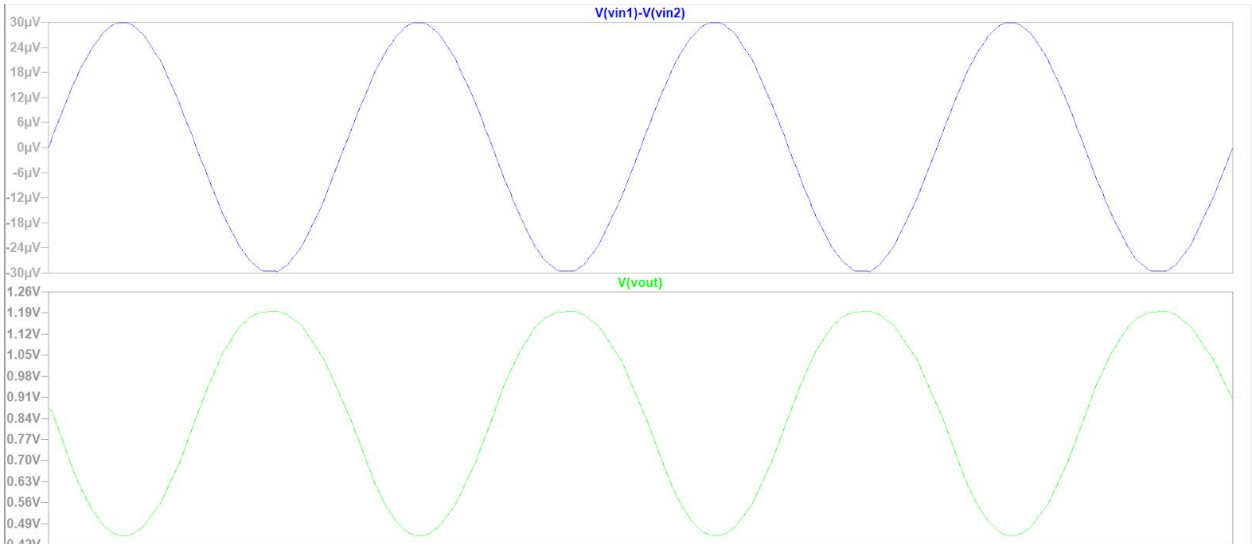
Table 6. Transistor sizes of two stage folded cascode OTA

In self bias one current mirror circuit is used and in order to bias transistors we connect resistors as and when required. The design parameters used in design are shown in the table. To bias the entire circuit current used is 210uA. Obviously, the gain obtained by this design is greater as we have cascode transistors at the output and also we obtain higher swing. Power dissipation of the circuit is P = Vdd * (Id(M1) + Id(M2) +Id(M6)) = 1218.06uW

DC analysis:

V(vin1):	0.93	voltage
V(vin2):	0.93	voltage
V(vdd):	1.8	voltage
V(vout):	0.874919	voltage
Id(M16):	0.000898837	device_current
Id(M13):	0.000174957	device_current
Id(M12):	0.000273154	device_current
Id(M8):	0.000174878	device_current
Id(M6):	0.000273086	device_current
Id(M7):	0.000270727	device_current
Id(M5):	0.000270727	device_current
Id(M17):	0.000898837	device_current
Id(M15):	0.000174957	device_current
Id(M14):	0.000174957	device_current
Id(M11):	0.000174878	device_current
Id(M9):	0.000174878	device_current
Id(M10):	0.000270727	device_current
Id(M1):	0.00021	device_current
Id(M2):	0.000196406	device_current
Id(M4):	9.81974e-005	device_current
Id(M3):	9.82082e-005	device_current
I(Cl):	8.74919e-024	device_current
I(C1):	-2.70916e-025	device_current
I(I1):	0.00021	device_current
I(R3):	0	device_current
I(R2):	0.000174878	device_current
I(R1):	0.000270727	device_current

TRANSIENT ANALYSIS:



On transient analysis, we observed that the output signal has a swing of about 0.74V which is nearly equal to half of supply voltage(1.8V). With this design we obtained a gain of about 81.82dB. To achieve gain greater than two stage folded OTA we go to three stage OTA.

Parameters	TWO STAGE FOLDED OTA
Supply voltage(V)	1.8
Load capacitance(pF)	10
Bias current(uA)	210
Gain(dB)	81.82
Power Dissipation(uW)	1218.06

Table7. Design specifications of Two stage folded cascode

2.3.5 THREE STAGE FOLDED CASCODE

Schematic of a three stage self biased folded cascode is shown below.

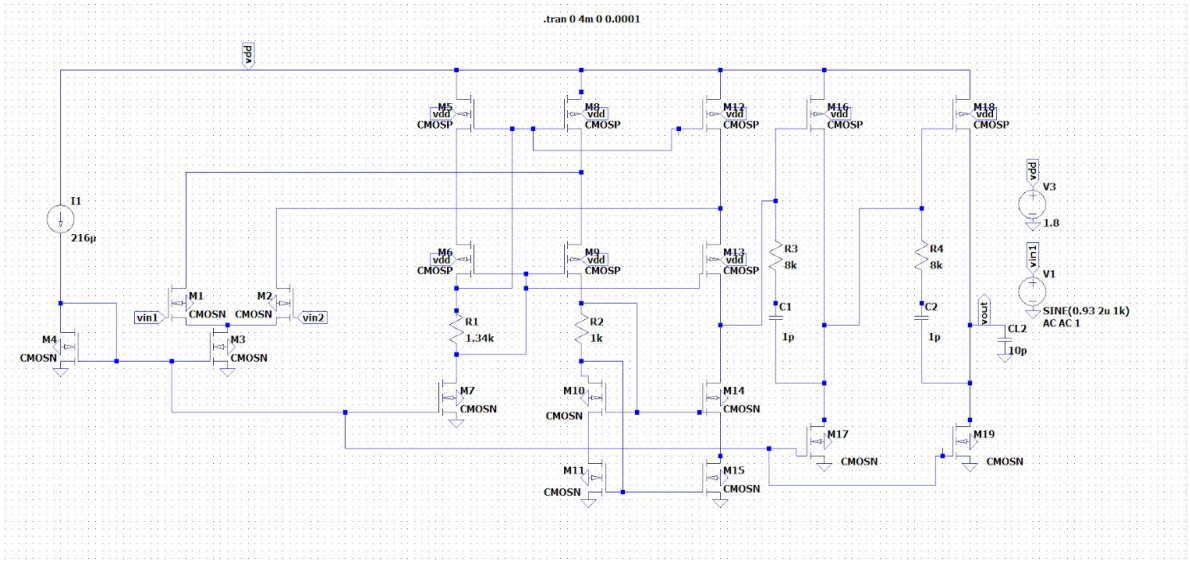


Fig9.LTSpice Schematic of three stage folded cascode

Design parameters:

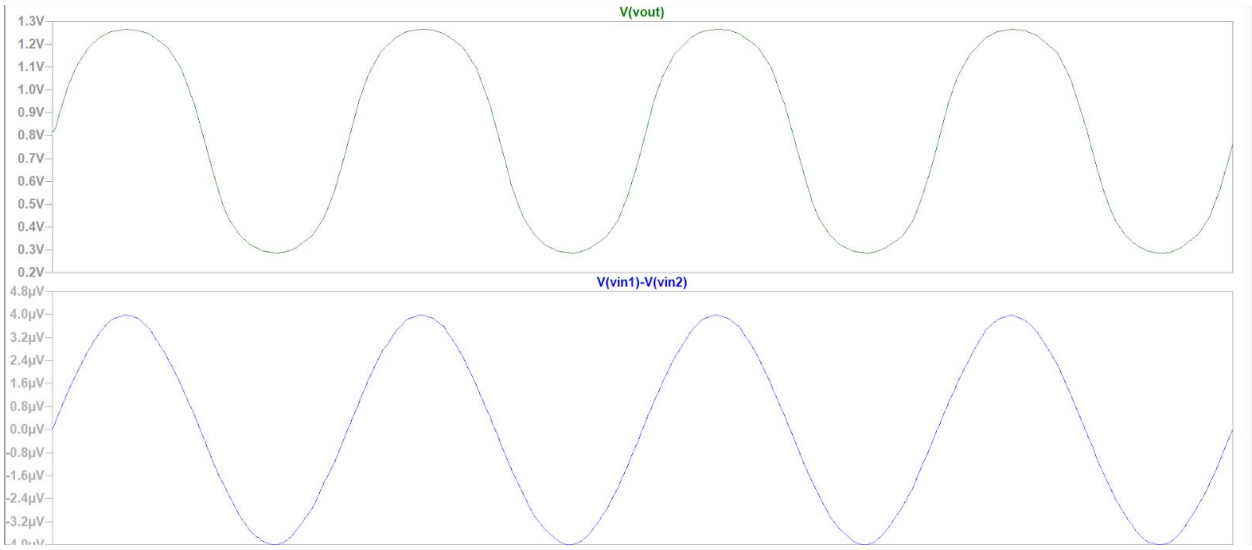
Transistor	Mosfet Type	L	W
M1, M2	NMOS	0.5u	7u
M3, M4	NMOS	0.5u	30u
M5, M6, M7, M8, M12, M13	PMOS	0.3u	170u
M9, M11, M14, M15	NMOS	0.5u	70u
M10	NMOS	0.5u	9u
M16	PMOS	0.5u	30u
M17	NMOS	0.5u	30u
M18	PMOS	0.5u	10u
M19	NMOS	0.5u	10u

Table8. Transistor sizes of three stage folded cascode OTA

DC operating point:

V(vin1):	0.93	voltage
V(vin2):	0.93	voltage
V(vdd):	1.8	voltage
V(vout):	0.814805	voltage
Id(M18):	0.000308055	device_current
Id(M16):	0.000905179	device_current
Id(M13):	0.000180923	device_current
Id(M12):	0.000280586	device_current
Id(M9):	0.000180842	device_current
Id(M8):	0.000280515	device_current
Id(M6):	0.000278165	device_current
Id(M5):	0.000278165	device_current
Id(M19):	0.000308055	device_current
Id(M17):	0.000905179	device_current
Id(M15):	0.000180923	device_current
Id(M14):	0.000180923	device_current
Id(M11):	0.000180842	device_current
Id(M10):	0.000180842	device_current
Id(M7):	0.000278165	device_current
Id(M4):	0.000216	device_current
Id(M3):	0.000199336	device_current
Id(M2):	9.96634e-005	device_current
Id(M1):	9.96731e-005	device_current
I(V3):	-0.0022685	device_current

Transient Analysis:



With this three stage cascading very high gain is obtained with a very good output swing. To self bias the entire three stage circuit bias current required is 216uA. From the peak to peak output and input waveforms we can calculate voltage gain which comes upto 101.7dB and voltage swing at the output is 1V which is slightly greater than half of supply voltage (1.8V). Power consumption of the circuit is P = 4083.3uW.

Parameters	THREE STAGE FOLDED CASCODE
Supply voltage(V)	1.8
Load capacitance(pF)	10
Bias current(uA)	216
Gain(dB)	101.7
Power Dissipation(uW)	4083.3

Table9. Design specifications of three stage folded cascode

2.3.6. FOUR STAGE FOLDED CASCODE

On cascading it's possible to achieve more gain but this trend also has its limitations. As we go on cascading the stability of the circuit decreases as the number of poles increases thus making the circuit unstable. Schematic of a four stage folded cascode is shown below.

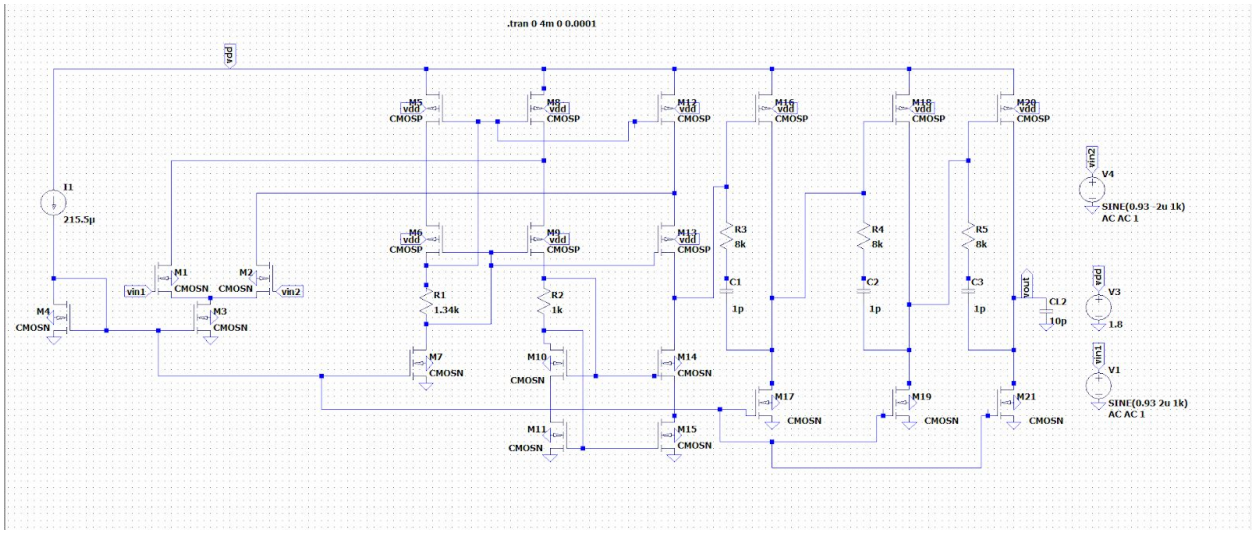
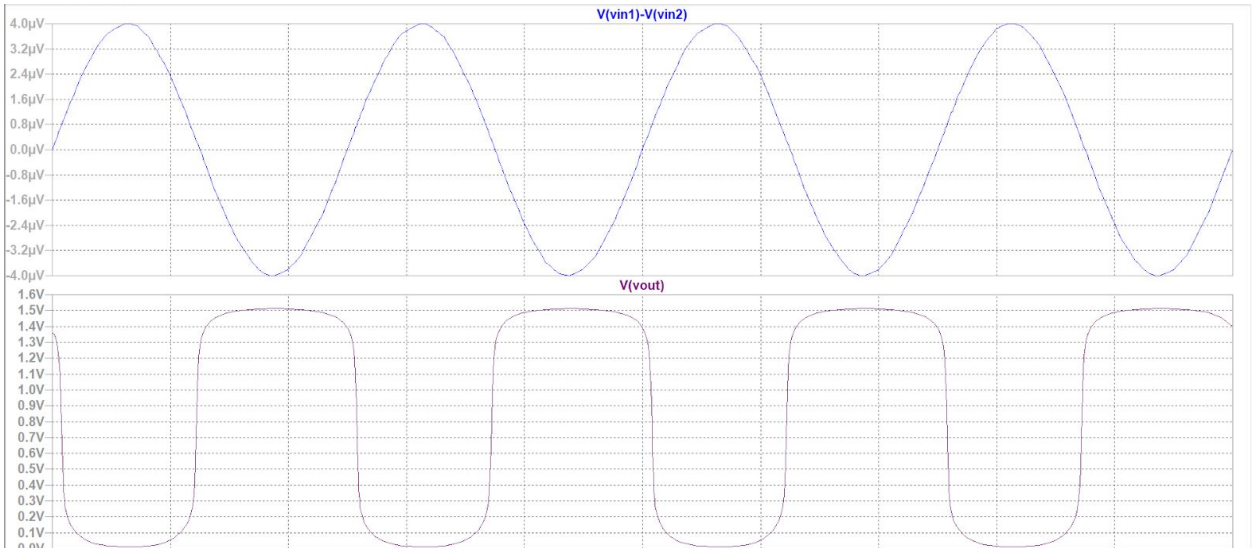


Fig10. LTSpice Schematic of four stage folded cascode

On proper dc analysis of the above circuit we did transient analysis whose outcomes are shown in Fig



Fig

With this design gain of about 106dB is obtained. But many theories say that there are drawbacks observed in cascoding more than three stages. So in order to obtain better performance of OTA in terms of gain and stability we should go for three stage cascode.

COMPARISON OF OTA TOPOLOGIES

Power = I(vdd) * vdd

Parameters	Single ended OTA	Telescopic OTA	Two stage Folded cascode	Three stage folded cascode
Supply voltage (V)	1.8	1.8	1.8	1.8
Gain(dB)	28.9	37.87	81.82	101.7
Ibias(uA)	50	100	210	216
Power Dissipation(uW)	132.03	685.06	1218.06	4083.3

Table10. Comparison of OTA topologies

From the above comparison table, we can observe that gain of three stage cascode is more when compared to other OTA topologies. We can also observe that the

power consumption for three stages is more as compared to others, this is because in three-stage we are driving more transistors and to make sure all these transistors are in required operation we need more bias current as we are self biasing the entire circuit.

Chapter 3

3.1 Conclusion

We have implemented single stage OTA with current source, single stage Telescopic OTA , Two stage Folded cascode OTA, Three stage Folded cascode OTA and Four stage folded cascode OTA. The single stage OTA with current source load has lesser gain(28.9dB) compared to telescopic OTA because it has a lower output impedance. Whereas the telescopic structure has a higher gain due to cascode load(37.87dB). But due to swing limitations at the output we go for folded cascode OTA which has almost the same gain at the output but a better swing. But the limitation of this topology is that it has higher noise at output due to increased number of devices. We implement two and three stage devices in order to get a better gain. We finally get a gain of 101.7 dB in the three stage structure. In terms of power, a folded cascode consumes more power compared to a telescopic because it has two extra current legs. Going for more stages results in instability at the output and hence we limit ourselves to three stages.

3.2 Future Scope

We can improvise the gain of OTA using three stages further and can reduce power consumption of the circuit by using suitable strategy. We can integrate OTA with any mixed signal and analog circuitry like ADC, DAC, Oscillators, Filters, etc. Based on application we can choose required specifications of OTA but as an overview gain of OTA should be reasonably high for better performance of any circuit.

3.3 References

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