3-Bit Flash Analog to Digital Converter (ADC)

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***Abstract*—This paper presents the design and implementation of a 3-bit Flash Analog-to-Digital Converter (ADC) using discrete hardware components. Flash ADCs are widely recognized for their high-speed performance, making them suitable for applications requiring rapid data conversion. The proposed 3-bit architecture employs seven comparators, a precision resistor ladder network for reference voltages, and a digital encoder to produce a 3-bit binary output from an analog input. The hardware prototype was developed and tested to verify functionality. This work demonstrates the feasibility of implementing compact and efficient Flash ADCs in practical systems where high-speed analog signal digitization is essential.**

I. Introduction

Analog-to-Digital Converters (ADCs) are pivotal in bridging the analog physical world with the digital processing domain. Flash ADCs are the fastest among the various ADC architectures due to their parallel comparator design, enabling real-time signal conversion with minimal latency. This speed makes them indispensable in applications such as digital oscilloscopes, radar systems, high-speed data acquisition, and modern communication systems.

Flash ADCs provide an excellent case study for applying analog principles such as voltage division, comparator behavior, and logic-level interfacing. This project presents the design and implementation of a 3-bit Flash ADC using discrete analog components. A resistor ladder network creates precise reference voltages, which are fed to comparators studied in the Linear Integrated Circuits (LIC) subject. The comparator outputs are then processed through a priority encoder to generate a corresponding 3-bit digital output.

This project concentrates on how each analog part of the 3-bit Flash ADC behaves in real hardware. The resistor ladder network, comparator array, and encoder were built and tested, confirming that the circuit works exactly as predicted by LIC theory.

II. Design Overview

The 3-bit Flash ADC designed in this project is structured into three principal stages: a resistor ladder network, a comparator array using LM393 ICs, and a priority encoder using the 74LS148 IC. Each stage plays a crucial role in converting an analog input signal into a corresponding 3-bit digital output.

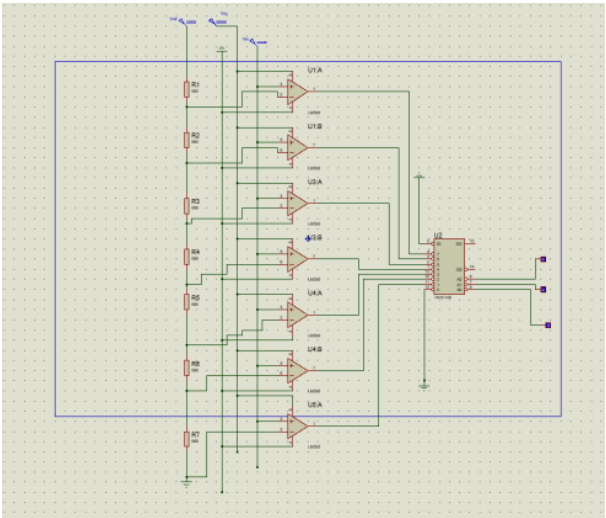

Fig. 1. Block Diagram of 3-Bit Flash ADC

A. Resistor Ladder Network

The resistor ladder network serves as a precision voltage divider that establishes seven discrete reference voltage levels across eight identical resistors, each of value 680 Ω. The reference voltage is assumed to be 5 V, and the voltage step is given by:

$$V_{\text{step}} = \frac{V_{\text{ref}}}{8} = 0.625 \text{ V}$$

B. Comparator Stage

Seven LM393 comparators are used to compare the analog input voltage with the reference voltages generated by the resistor ladder. The reference voltages are applied to the inverting terminals, while the analog input voltage (V_{in}) is applied to the non-inverting terminals. The LM393 is a fast comparator IC that requires an external pull-up resistor at the output stage. When the input voltage exceeds the reference voltage, the comparator output transitions to logic high.

TABLE I
REFERENCE NODE VOLTAGES OF RESISTOR LADDER

Node	Voltage (V)
V1	4.375
V2	3.75
V3	3.125
V4	2.5
V5	1.875
V6	1.25
V7	0.625

TABLE II
THERMOMETER CODE FOR $V_{in} = 2.8$ V

Comparator	Ref Voltage (V)	Condition	Output
C1	0.625	$V_{in} > V_{ref}$	1
C2	1.25	$V_{in} > V_{ref}$	1
C3	1.875	$V_{in} > V_{ref}$	1
C4	2.5	$V_{in} > V_{ref}$	1
C5	3.125	$V_{in} < V_{ref}$	0
C6	3.75	$V_{in} < V_{ref}$	0
C7	4.375	$V_{in} < V_{ref}$	0

C. Priority Encoder Stage

The thermometer code generated by the comparator outputs is converted into a 3-bit binary output using a 74LS148 priority encoder. The encoder prioritizes the highest-order active input and generates the corresponding binary output. This ensures a unique digital representation for each voltage range and simplifies the decoding of comparator outputs in Flash ADC architectures.

III. ANALYSIS AND METHODOLOGY

A. Design Specifications

The reference voltage (V_{ref}) is chosen as 5 V. The total resistance of the ladder is assumed to be 5 kΩ, resulting in a reference current of 1 mA and a power dissipation of approximately 5 mW.

B. Node Voltage Calculation

Using the step size of 0.625 V, the individual node voltages are calculated as shown in Table I.

These voltages are supplied to the inverting terminals of the LM393 comparators, while the analog input voltage is applied to the non-inverting terminals.

C. Thermometer Code and Encoder Operation

For a 3-bit Flash ADC, there are $2^3 = 8$ quantization levels and 7 comparators. For an input voltage of 2.8 V, the comparator outputs are shown in Table II.

The resulting thermometer code is 1111000, which is encoded by the 74LS148 priority encoder as the binary output **100**.

IV. CONCLUSION

In this project, a 3-bit Flash Analog-to-Digital Converter was successfully designed and implemented using basic linear integrated circuit components. The design employs a resistor ladder network for reference voltage generation, LM393 comparators for analog comparison, and a 74LS148 priority encoder for digital encoding. The Flash ADC demonstrates fast conversion without the use of clock signals and accurately maps analog input voltages to corresponding digital outputs. This project clearly demonstrates the practical application of LIC concepts such as voltage division, comparator operation, and digital encoding in real-time data conversion systems.

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