Yagna Vivek B

Student

I'm an Electronics and Communication Engineering student at PES University. I like VLSI based topics and try to increase my knowledge about them by attending talks, sharing knowledge with friends and by working on projects. I spend my time efficiently and will be ready to explore any new topics that i encounter to help others. I am actively looking for an opportunity to show my work attitude, get office experience, increase my skills and knowledge depth in the domain.

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EDUCATION

Pre-University
Sree Vasavi vidya kendra

04/2018 - 04/2020   *Kollegal, Karnataka, India*

Electronics and Communication Engineering
PES University

08/2020 - 08/2024   *Bengaluru,India*

Minors in Computer Science Enginnering
- CGPA - 8.73

PERSONAL PROJECTS

Layered testbench for D_flipflop in system verilog
- A testbench that verifies the functionality of a D-flip-flop

RISC4R
- This is a part of RISC-V processor built just to understand the R-type instruction execution.(arithmetic and logical operations)

FPGA prototyping using Xilinx IP
- written a verilog code for described RTL, Implemented it on a Remote FPGA using Xilinx

Varunavriti (09/2022 - Present)
- varunavriti is the name of our project when we are participating in the E-Yantra innovation challenge organised by IIT Bombay and we got selected into top 50 among thousand of teams that had applied

Sequence Detector
- Detect a sequence of bits from an input given using an FPGA

Simulation and Synthesis of Quantum NanoDevices (02/2023 - Present)
- working on literature survey

WORK EXPERIENCE

Regulatory Affairs - Research Intern
Meditix Solutions

07/2022 - 08/2022   *Bengaluru,India*

Got Stipend for the work
- Research on non active medical devices
- Documentation of required information from IEEE papers
- successfully completed the task before time
- Experienced Office environment
- Was offered to work there for a longer period of time

SKILLS

Computer Aided Digital Design   Cadence Virtuoso
Matlab   Electronic Device Automation - OpenLane
System verilog   RISC-V   OPAMP   C language
Problem Solving

ACHIEVEMENTS

Distinction award and MRD Scholarship
Being honored with scholarships every semester for good Academic performance

CERTIFICATES

FPGA Architecture and Programming using Verilog

Regulatory Affairs Certification

Robofest 2.0

LANGUAGES

Kannada
Native or Bilingual Proficiency

Telugu
Native or Bilingual Proficiency

English
Professional Working Proficiency

Hindi
Professional Working Proficiency

Tamil
Elementary Proficiency

INTERESTS

VLSI   Biology   Indian History(Mythology)

Philately and Numismatics