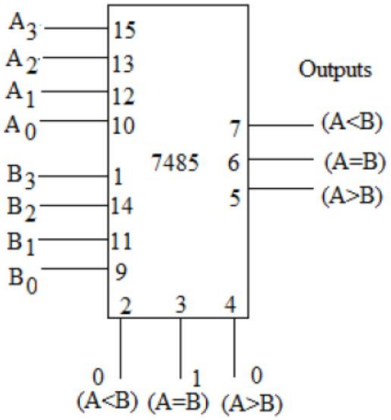
TASK 4 - GROUP 1

DESIGN AND IMPLEMENTATION OF 4BIT COMPARATOR USING EDA TOOL

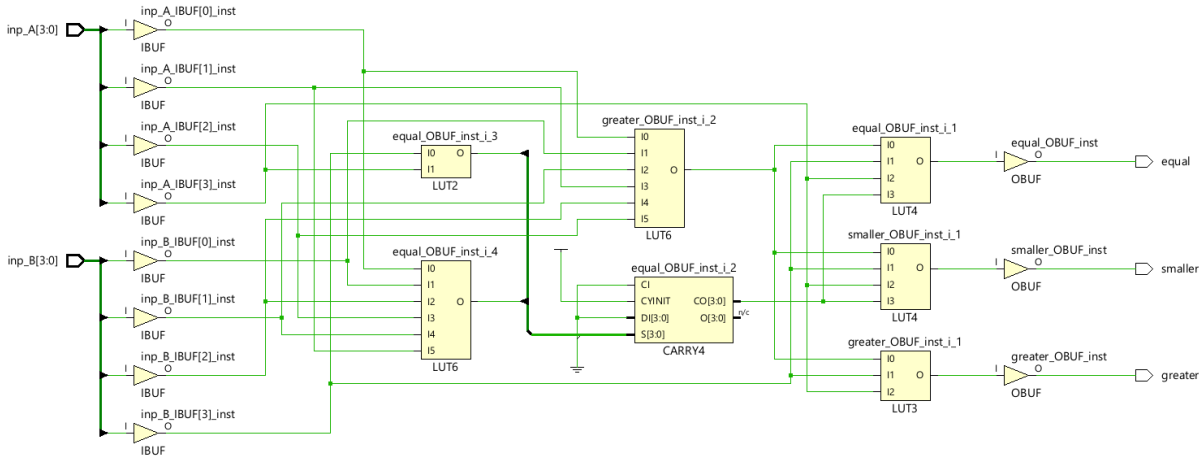
BLOCK DIAGRAM OF 4-bit COMPARATOR:



VHDL CODE:

```
library ieee;
use ieee.std_logic_1164.all;
use ieee.numeric_std.all;
entity FRBTCOMP is
  port (
      inp_A, inp_B   : in std_logic_vector(3 downto 0);
      greater, equal, smaller  : out std_logic);
end FRBTCOMP;
architecture Behavioral of FRBTCOMP is
begin
  process(inp_A, inp_B)
    variable a_int, b_int: integer;
  begin
    a_int := to_integer(unsigned(inp_A));
    b_int := to_integer(unsigned(inp_B));
      if a_int > b_int then
      greater <= '1';
      equal <= '0';
      smaller <= '0';
    elsif a_int = b_int then
      greater <= '0';
      equal <= '1';
      smaller <= '0';
    else
      greater <= '0';
      equal <= '0';
      smaller <= '1';
    end if;
  end process;
end Behavioral;
```

RTL:



TESTBENCH:

```
library ieee;
use ieee.std_logic_1164.all;
use ieee.numeric_std.all;
entity TB_FRBTCOMP is
end TB_FRBTCOMP;
architecture Behavioral of TB_FRBTCOMP is
  component FRBTCOMP is
    port (
      inp_A, inp_B   : in std_logic_vector(3 downto 0);
      greater, equal, smaller  : out std_logic
    );
  end component;

  -- Inputs
  signal inp_A : std_logic_vector(3 downto 0) := (others => '0');
  signal inp_B : std_logic_vector(3 downto 0) := (others => '0');

  -- Outputs
  signal greater : std_logic;
  signal equal : std_logic;
  signal smaller : std_logic;

begin

  -- Instantiate the Unit Under Test (UUT)
  uut: FRBTCOMP
```

```
  port map (
    inp_A => inp_A,
    inp_B => inp_B,
    greater => greater,
    equal => equal,
    smaller => smaller
  );

-- Stimulus process
stim_proc: process
begin

  inp_A <= "1010";
  inp_B <= "0110";
  wait for 10 ns;
  assert (greater = '1' and equal = '0' and smaller = '0')
    report "Test case 1 failed" severity error;


  inp_A <= "0011";
  inp_B <= "0101";
  wait for 10 ns;
  assert (greater = '0' and equal = '0' and smaller = '1')
    report "Test case 2 failed" severity error;


  inp_A <= "0100";
  inp_B <= "0100";
  wait for 10 ns;
  assert (greater = '0' and equal = '1' and smaller = '0')
    report "Test case 3 failed" severity error;


  inp_A <= "0000";
  inp_B <= "0000";
  wait for 10 ns;
  assert (greater = '0' and equal = '1' and smaller = '0')
    report "Test case 4 failed" severity error;


  inp_A <= "1111";
  inp_B <= "1111";
  wait for 10 ns;
```

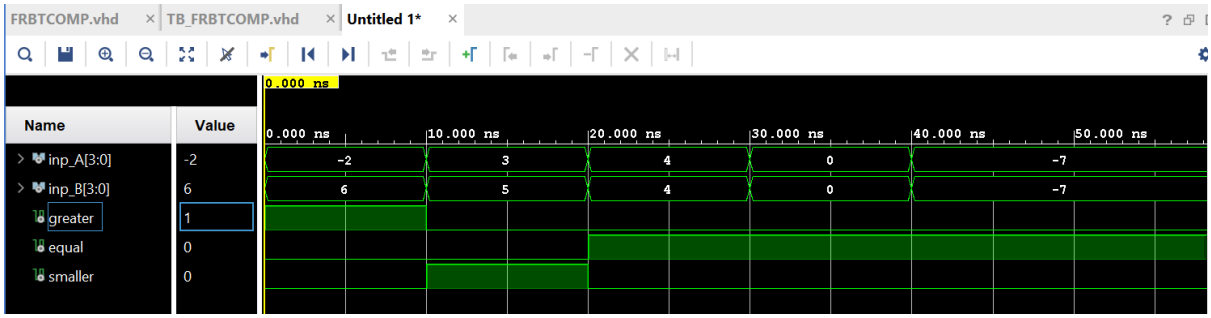
```
    assert (greater = '0' and equal = '1' and smaller = '0')
      report "Test case 5 failed" severity error;


    inp_A <= "0000";
    inp_B <= "0000";
    wait for 10 ns;
    assert (greater = '0' and equal = '1' and smaller = '0')
      report "Test case 4 failed" severity error;

    wait;
  end process;

end Behavioral;
```

SIMULATION:

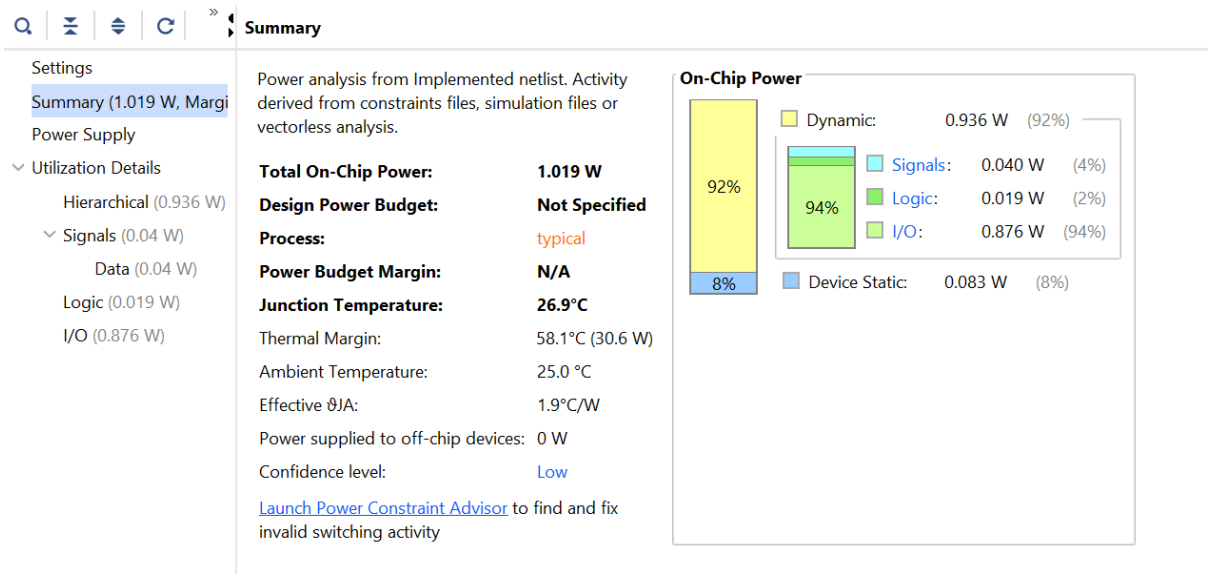


TIMING REPORT:

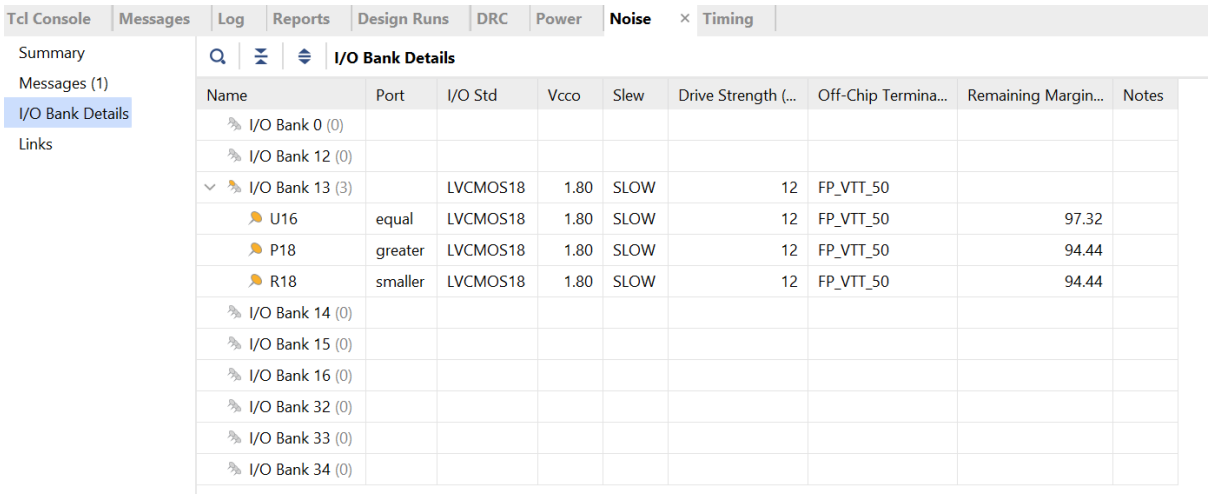
Design Timing Summary

Setup		Hold		Pulse Width	
Worst Negative Slack (WNS):	inf	Worst Hold Slack (WHS):	inf	Worst Pulse Width Slack (WPWS):	NA
Total Negative Slack (TNS):	0.000 ns	Total Hold Slack (THS):	0.000 ns	Total Pulse Width Negative Slack (TPWS):	NA
Number of Failing Endpoints:	0	Number of Failing Endpoints:	0	Number of Failing Endpoints:	NA
Total Number of Endpoints:	3	Total Number of Endpoints:	3	Total Number of Endpoints:	NA

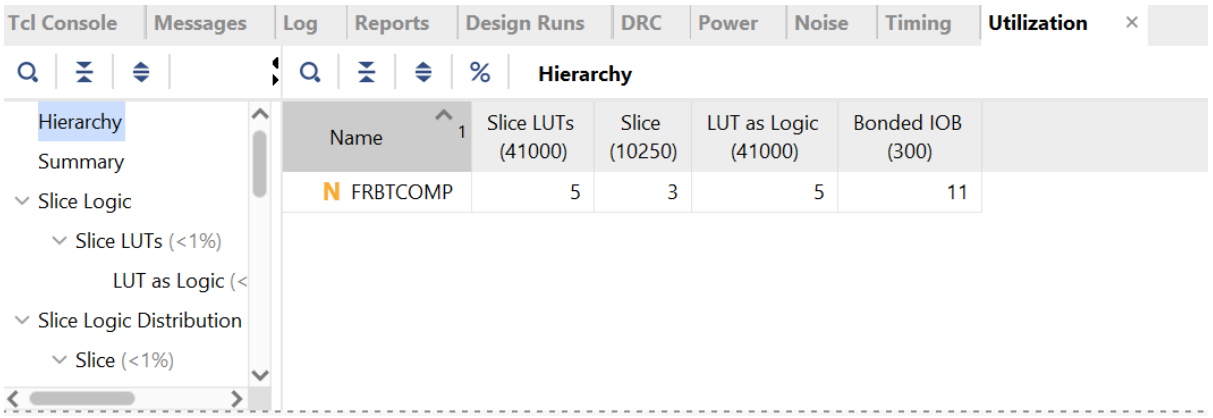
REPORT POWER:



REPORT NOISE:



UTILIZATION REPORT:



DEVICE IMPLIMENTATION: