Task-3

Features & Design flow of Mentor graphics EDA Questasim

Schematic-Based Design Flow Overview

The following describes the design flow for creating a design using the Design Architect Schematic capture program, QuickSim II simulator, and Actel Designer Series software. For instructions on how to use the Designer Series software and its tools, refer to the Designing with Actel manual.

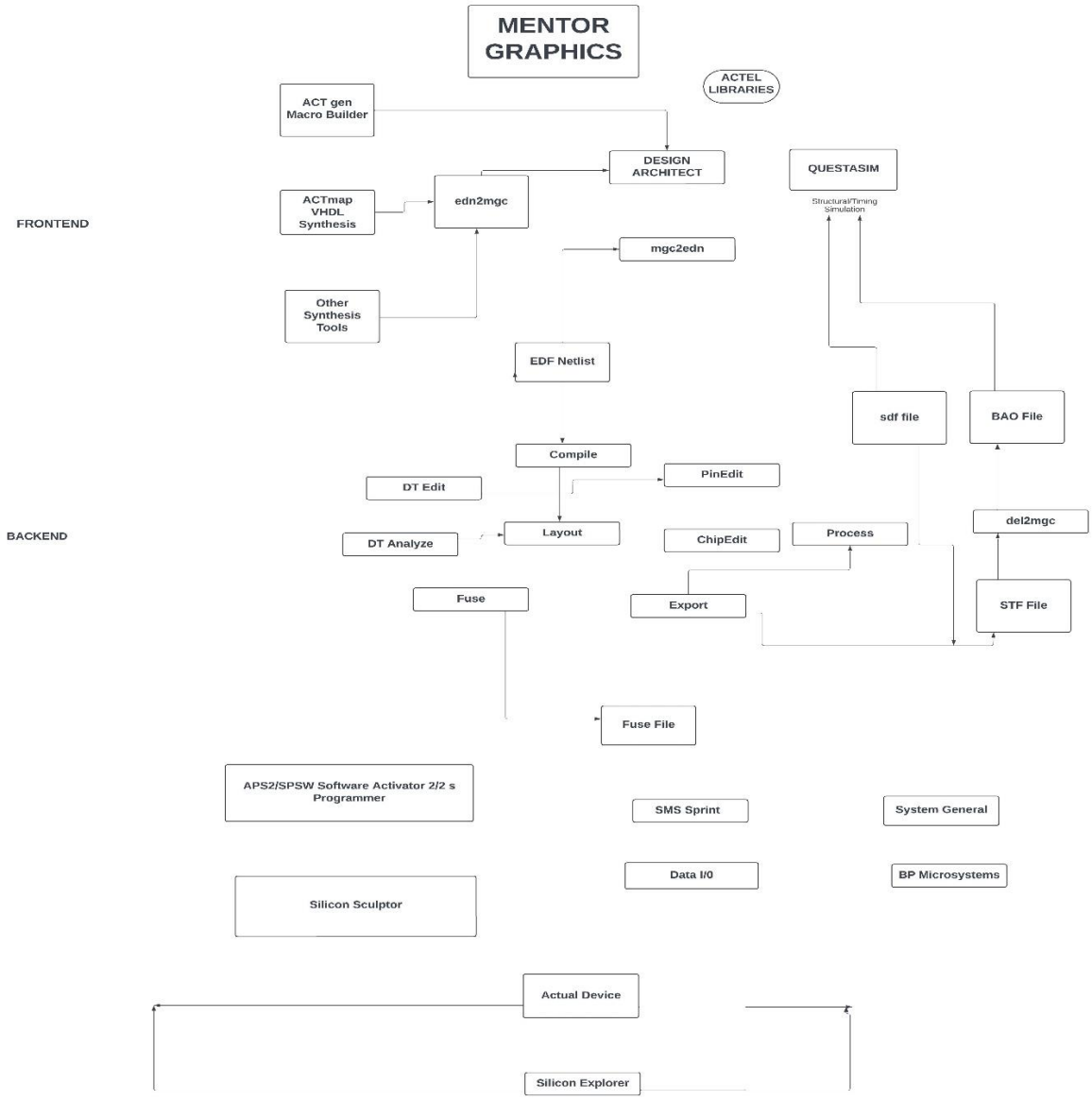

Fig: Flow for Mentor graphics EDA

Design Creation/ Verification

Design Creation/Verification consists of Schematic Capture, Functional Simulation, and EDIF netlist generation.

Schematic Capture

Enter your design in Design Architect. Use one of the Actel family symbol libraries. Save the design. Refer to Mentor Graphics documentation for more information.

EDIF Netlist

After you create the schematic, use mgc2edn to create an EDIF".edn" netlist

Functional Simulation

Use QuickSim II to perform a functional simulation of your design.

Note: The functional simulation sets all delays to one nanosecond

Design Implementation

During design implementation, a design is placed and routed using Designer. Additionally, static timing analysis may be performed in Designer with the DT Analyze tool. After place and route, post-layout (timing) simulation is performed with QuickSim II.

Place and Route

Use Designer to place and route your design. Refer to the Designing with Actel manual for information about using Designer.

Timing Analysis

Use the DT Analyze tool in Designer to perform static timing analysis on your design.

Timing Simulation

To perform a timing simulation on your design using QuickSim II after placing and routing it. Timing simulation verifies that the design meets your timing requirements. Timing simulation requires information extracted and back annotated from Designer.

Programming

Schematic-Based Design Flow Overview Timing Analysis Use the DT Analyze tool in Designer to perform static timing analysis on your design.

Timing Simulation & Verification

To perform a timing simulation on your design using QuickSim II after placing and routing it. Timing simulation verifies that the design meets your timing requirements. To perform system verification on a programmed device using the Actel Action Probe or Silicon Explorer.

Lucid Chart Link:

https://lucid.app/lucidchart/afa62942-3b2f-4760-b614-8cbe87c3e66f/edit?viewport_loc=-714%2C-563%2C3636%2C1510%2C0_0&invitationId=inv_de431c50-10a3-4c7e-94c9-d7b3d70cf302