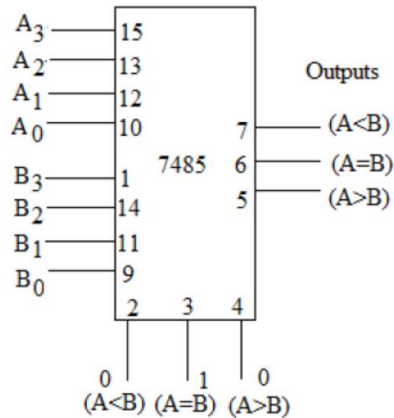


TASK 4 - GROUP 1

DESIGN AND IMPLEMENTATION OF 4BIT COMPARATOR USING EDA TOOL

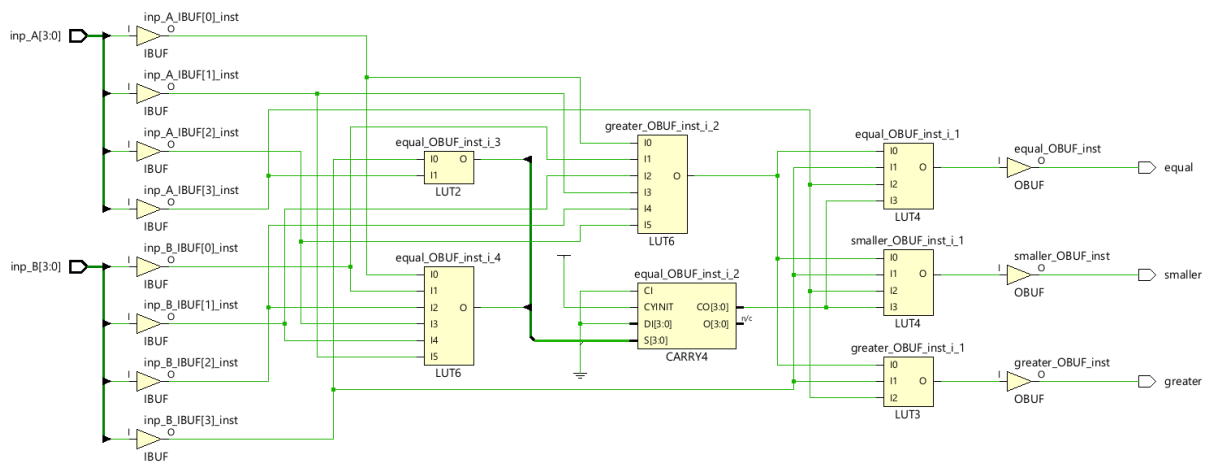
BLOCK DIAGRAM OF 4-bit COMPARATOR:



VHDL CODE:

```
20 | library ieee;
21 | use ieee.std_logic_1164.all;
22 | use ieee.numeric_std.all;
23 | entity FRBTCOMP is
24 |     port (
25 |         inp_A, inp_B    : in std_logic_vector(3 downto 0);
26 |         greater, equal, smaller : out std_logic);
27 | end FRBTCOMP;
28 | architecture Behavioral of FRBTCOMP is
29 | begin
30 |     process(inp_A, inp_B)
31 |         variable a_int, b_int: integer;
32 |     begin
33 |         a_int := to_integer(unsigned(inp_A));
34 |         b_int := to_integer(unsigned(inp_B));
35 |         if a_int > b_int then
36 |             greater <= '1';
37 |             equal <= '0';
38 |             smaller <= '0';
39 |         elsif a_int = b_int then
40 |             greater <= '0';
41 |             equal <= '1';
42 |             smaller <= '0';
43 |         else
44 |             greater <= '0';
45 |             equal <= '0';
46 |             smaller <= '1';
47 |         end if;
48 |     end process;
49 | end Behavioral;
```

RTL:



TESTBENCH:

```
library ieee;
use ieee.std_logic_1164.all;
use ieee.numeric_std.all;
entity TB_FRBTCOMP is
end TB_FRBTCOMP;
architecture Behavioral of TB_FRBTCOMP is
  component FRBTCOMP is
    port (
      inp_A, inp_B : in std_logic_vector(3 downto 0);
      greater, equal, smaller : out std_logic
    );
  end component;

  -- Inputs
  signal inp_A : std_logic_vector(3 downto 0) := (others => '0');
  signal inp_B : std_logic_vector(3 downto 0) := (others => '0');

  -- Outputs
  signal greater : std_logic;
  signal equal : std_logic;
  signal smaller : std_logic;

begin

  -- Instantiate the Unit Under Test (UUT)
  uut: FRBTCOMP
```

```
port map (  
    inp_A => inp_A,  
    inp_B => inp_B,  
    greater => greater,  
    equal => equal,  
    smaller => smaller  
);
```

```
-- Stimulus process
```

```
stim_proc: process
```

```
begin
```

```
inp_A <= "1010";  
inp_B <= "0110";  
wait for 10 ns;  
assert (greater = '1' and equal = '0' and smaller = '0')  
    report "Test case 1 failed" severity error;
```

```
inp_A <= "0011";  
inp_B <= "0101";  
wait for 10 ns;  
assert (greater = '0' and equal = '0' and smaller = '1')  
    report "Test case 2 failed" severity error;
```

```
inp_A <= "0100";  
inp_B <= "0100";  
wait for 10 ns;  
assert (greater = '0' and equal = '1' and smaller = '0')  
    report "Test case 3 failed" severity error;
```

```
inp_A <= "0000";  
inp_B <= "0000";  
wait for 10 ns;  
assert (greater = '0' and equal = '1' and smaller = '0')  
    report "Test case 4 failed" severity error;
```

```
inp_A <= "1111";  
inp_B <= "1111";  
wait for 10 ns;
```

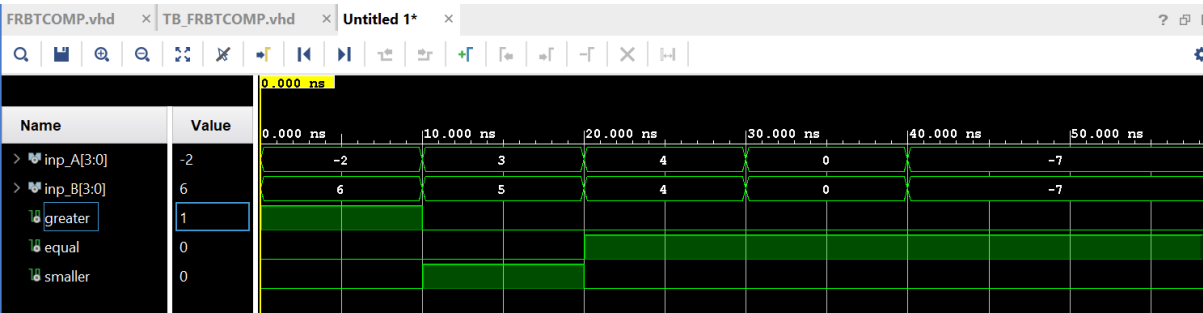
```
assert (greater = '0' and equal = '1' and smaller = '0')
report "Test case 5 failed" severity error;
```

```
inp_A <= "0000";
inp_B <= "0000";
wait for 10 ns;
assert (greater = '0' and equal = '1' and smaller = '0')
report "Test case 4 failed" severity error;
```

```
wait;
end process;
```

```
end Behavioral;
```

SIMULATION:



TIMING REPORT:

Design Timing Summary					
Setup		Hold		Pulse Width	
Worst Negative Slack (WNS):	inf	Worst Hold Slack (WHS):	inf	Worst Pulse Width Slack (WPWS):	NA
Total Negative Slack (TNS):	0.000 ns	Total Hold Slack (THS):	0.000 ns	Total Pulse Width Negative Slack (TPWS):	NA
Number of Failing Endpoints:	0	Number of Failing Endpoints:	0	Number of Failing Endpoints:	NA
Total Number of Endpoints:	3	Total Number of Endpoints:	3	Total Number of Endpoints:	NA

REPORT POWER:

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Summary

Settings

Summary (1.019 W, Margin: 8%)

Power Supply

Utilization Details

- Hierarchical (0.936 W)
- Signals (0.04 W)
 - Data (0.04 W)
 - Logic (0.019 W)
 - I/O (0.876 W)

Power analysis from Implemented netlist. Activity derived from constraints files, simulation files or vectorless analysis.

Total On-Chip Power: 1.019 W

Design Power Budget: Not Specified

Process: typical

Power Budget Margin: N/A

Junction Temperature: 26.9°C

Thermal Margin: 58.1°C (30.6 W)

Ambient Temperature: 25.0 °C

Effective θJA: 1.9°C/W

Power supplied to off-chip devices: 0 W

Confidence level: Low

[Launch Power Constraint Advisor](#) to find and fix invalid switching activity

On-Chip Power

92%

8%

Dynamic: 0.936 W (92%)

Device Static: 0.083 W (8%)

94%

Signals: 0.040 W (4%)

Logic: 0.019 W (2%)

I/O: 0.876 W (94%)

REPORT NOISE:

Tcl Console

Messages

Log

Reports

Design Runs

DRC

Power

Noise

Timing

Summary

Messages (1)

I/O Bank Details

Links

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I/O Bank Details

Name	Port	I/O Std	Vcco	Slew	Drive Strength (...)	Off-Chip Termina...	Remaining Margin...	Notes
I/O Bank 0 (0)								
I/O Bank 12 (0)								
I/O Bank 13 (3)		LVC MOS18	1.80	SLOW	12	FP_VTT_50		
U16	equal	LVC MOS18	1.80	SLOW	12	FP_VTT_50	97.32	
P18	greater	LVC MOS18	1.80	SLOW	12	FP_VTT_50	94.44	
R18	smaller	LVC MOS18	1.80	SLOW	12	FP_VTT_50	94.44	
I/O Bank 14 (0)								
I/O Bank 15 (0)								
I/O Bank 16 (0)								
I/O Bank 32 (0)								
I/O Bank 33 (0)								
I/O Bank 34 (0)								

UTILIZATION REPORT:

Tcl Console

Messages

Log

Reports

Design Runs

DRC

Power

Noise

Timing

Utilization

Hierarchy

Summary

Slice Logic

- Slice LUTs (<1%)
 - LUT as Logic (<1%)
- Slice Logic Distribution
 - Slice (<1%)

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Hierarchy

Name	Slice LUTs (41000)	Slice (10250)	LUT as Logic (41000)	Bonded IOB (300)
FRBTCOMP	5	3	5	11

DEVICE IMPLIMENTATION:

