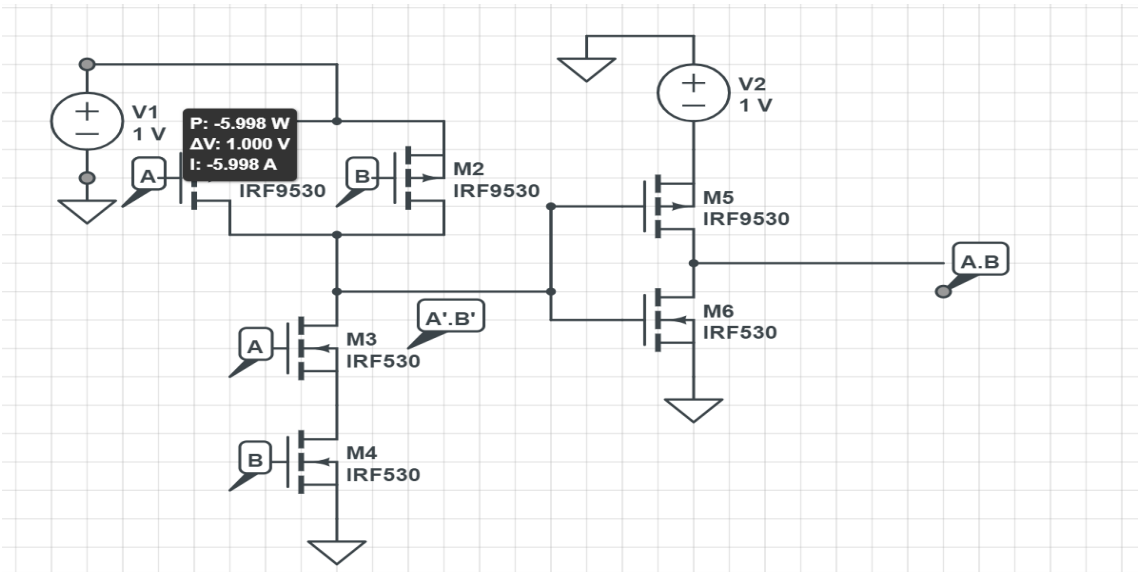
Task-7

Schematic of AND Gate



Layout for AND Gate