GUJARAT TECHNOLOGICAL UNIVERSITY

(GTU)

INNOVATION COUNCIL (GIC)

Patent Search & Analysis Report

(PSAR)

Date of Submission : 24/09/2016

Dear **Patel Miloni,**

Studied Patent Number for generation of PSAR	:	**16BE7_130020107065_3**

PART 1: PATENT SEARCH DATABASE USED

1. Patent Search Database used	:	Google Patents
Web link of database	:	https://patents.google.com/
2. Keywords Used for Search	:	ERP,BACKEND,SQL
3. Search String Used	:	ERP with backend in sql
4. Number of Results/Hits getting	:	627

PART 2: BASIC DATA OF PATENTED INVENTION /BIBLIOGRAPHIC DATA

5. Category/ Field of Invention	:	Computer/IT Engineering
6. Invention is Related to/Class of Invention	:	Process for optimizing software components for an enterprise resource planning (ERP) application SAP
6 (a) : IPC class of the studied patent	:	G06F11/3471,G06F11/3428,G06F9/5083,G06Q10/06
7. Title of Invention	:	Process for optimizing software components for an enterprise resource planning (ERP) application SAP
8. Patent No.	:	US7805706B1
9. Application Number	:	US11157395
9 (a) : Web link of the studied patent	:	https://patents.google.com/patent/US7805706B1/en?q=erp&q=backend&q=sql
10. Date of Filing/Application (DD/MM/YYYY)	:	21/06/2005
11. Priority Date (DD/MM/YYYY)	:	21/06/2005
12. Publication/Journal Number	:	9/5083 (20130101), 11/3428 (20130101)
13. Publication Date (DD/MM/YYYY)	:	28/09/2010
14. First Filled Country : Albania	:	Albania

15. Also Published as

Sr.No	Country Where Filled	Application No./Patent No.
1	Albania	11/157,395

16. Inventor/s Details.

Sr.No	Name of Inventor	Address/City/Country of Inventor
1	Ly Tania Trinh	Irvine, CA
2	Praditphollert Kulwipa	Mission Viejo, CA

17. Applicant/Assignee Details.

Sr.No	Name of Applicant/Assignee	Address/City/Country of Applicant
1	Unisys Corp	Blue Bell, PA

18. Applicant for Patent is : College

PART 3: TECHNICAL PART OF PATENTED INVENTION

19. Limitation of Prior Technology / Art

In a three-tier ERP implementation, multiple servers are interconnected through one or more network infrastructure. Users may observe poor performance due to the complexity and the number of interconnected components in the implementation. Herein is devised a process for tuning the software component by applying tuning techniques to the OS, SAP application and Database Management System software. For each component, the process identifies potential tuning opportunities of various subcomponents. The process is iterated numerous times through all software components while applying the tuning techniques to derive the most optimal performance for the ERP implementation.

20. Specific Problem Solved / Objective of Invention

In the three-tier client/server SAP Sales and Distribution (SD) implementation, where multiple servers are interconnected with one or more network infrastructure, there is provided a process where one can systematically apply proven methodology for tuning the software components to achieve the best results and avoid poor performance and thereby improve the overall results of the SAP SD implementation. This process is a template for tuning software components on multiprocessor servers.

21. Brief about Invention

In order for the Enterprise Resource Planning (ERP) SAP to run efficiently on a multiprocessor server in a multi-tier client/server environment, there is devised a process where one can systematically apply proven methodology to evaluate and optimize the software components to achieve the best system performance on multiprocessor servers.

In the entire ERP implementation, software comprises fifty percent of the tuning opportunity. The other fifty percent is hardware tuning. Thus, a fine tuned software component ensures that one is halfway to achieving the goal of a well-tuned ERP implementation.

The description of how each tier interacts with each other, as well as how the SD benchmark was simulated was described in detail in the co-pending application, U.S. Ser. No. 11/157,393, entitled “Process For Optimizing An Enterprise Resource Planning (ERP) Application SAP On Multiprocessor Servers”.

Further information on how to fine-tune hardware components was described in the co-pending application, U.S. Ser. No. 11/157,394, entitled “Process For Optimizing Hardware Components For An Enterprise Resource Planning (ERP) Application SAP On Multiprocessor Servers”.

22. Key learning Points

1. CROSSBAR INTERCONNECT (CI): A scalable switch device consists of multiple, independent data paths, or pipes that connect processors and Peripheral Component Interconnect (PCI) modules to memory.
2. PROCESSOR MODULE (POD): A module that consists of a crossbar interconnect (CI) and one or two processor submodules (subpod).
3. PROCESSOR/MEMORY NODULE: A hardware module consisting of processor and memory components for 64-bit ES7000 servers. Each module provides mounting locations and supports an interconnection circuitry for four processor chips and 16 dual inline memory modules (DIMMs).
4. PROCESSOR SUBMODULE (SUBPOD): It is one of the two processing units in a processor module (pod). One processor submodule

contains up to four processors, first- and second-level cache, shared cache, and interconnection logic.
5. ES7000: A family of Unisys multiprocessor servers. ES7000 is a multiplatform server supporting Windows™, Linux, MCP operating systems, OS2200 systems and other applications.
6. SHARED CACHE: A cache shared by multiple processors in the same processor submodule.
7. VIRTUAL INTERFACE ARCHITECTURE (VIA): Virtual Interface Architecture (VIA) is a communication protocol that provides a direct path for applications, bypassing the operating system interfaces and achieving very high throughput. Giganet cLAN is the first native implementation of VIA and is used in the Unisys benchmark environment. Giganet cLAN delivers high throughput and low latency interconnection of multiple servers. Giganet cLAN provides full-duplex throughput of 1.25 Gb/s (20 Gb/s aggregate). Due to small port-to-port latency and minimal CPU overhead, Giganet cLAN is used for data transferring between application servers and the database server.
8. DIRECT I/O BRIDGE (DIB): DIB is hardware unit in the ES7000 where the peripheral component interconnect (PCI) buses are located. It provides a path from the processors and memory to the PCI buses.
9. 32-BIT ARCHITECTURE: 32-bit is a term applied to processors, and computer architectures that manipulate the address and data in 32-bit “chunks” of 4 bytes data.
10. 64-BIT ARCHITECTURE: A computer architecture described as “64-bit” generally has integer registers that are 64 bits wide and thus directly supports 64-bit “chunks” of data.
11. INTERRUPTS: Interrupts are signals that a device can send to a processor when the device is ready to accept or send information.
12. DATA LOCALIZATION: Data localization refers to a method of placing data in a local cache or the nearest memory area in order to provide fast access to the data and reduce memory latency.
13. SYSTEM LATENCY: System latency refers to the delay required to complete a given operation. For example, memory latency describes the delay introduced when a data needs to be transferred from memory to the processors.

23. Summary of Invention

In the entire ERP implementation, software comprises fifty percent of the tuning opportunity. The other fifty percent is the hardware tuning. Thus, a fine tuned software component ensures that one is halfway to achieving the goal of a well-tuned ERP implementation.

Devised herein is a process with proven tuning techniques to optimize an ERP application SAP for better performance on multiprocessor servers in a three-tier client/server implementation.

For the devised process, the focus is only on the software components. This process takes into consideration the Operating System (OS), the SAP application and the Database Management System (DBMS) software. It identifies the potential tuning opportunities for each of those software components.

The process considers each component and evaluates its potential tuning opportunities. For each component, the process further identifies the subcomponents for potential tuning opportunities. For example, after identifying the OS, the process also evaluates the type of OS and the drivers that are supported on that OS.

The process is thus reiterated through all the software components to identify each tuning opportunity and apply tuning techniques to derive at the optimal result. Once all the opportunities are identified and all the tuning techniques are applied, the process is deemed completed. Once the process is completed, optimal performance is achieved and bottlenecks and poor performance is thus avoided.

24. Number of Claims : 21

25. Patent Status : Published Application

26. How much this invention is related with your IDP/UDP?

< 70 %

27. Do you have any idea to do anything around the said invention to improve it? (Give short note in not more than 500 words)

The patent does not include / mention anything about the security of the same data that has been input and stored.
Hence, as solutions/ improvements to it, we can consider:
i) adding certain measures to the security of the data so the unauthorized accesses can be prevented
ii) making sure that when the newer data is added then the older data is preserved in a safe environment, without geting damaged or changed
iii) the patent is supporting the display of the analyzed data on multiple platforms, but if the entry of the data is also made available on multiple platforms then the process of the collection of the data would become much more easier
iv) the attendance taking should also be made available on the mobile phones in the classroom for the faculty members / teachers so that at-thetime
accurate attendance can be taken