CS F342 COMPUTER ARCHITECTURE
QUIZ 1: SET 1

Name:

ID:

Write your answer only in the following table.

Q#	Q1	Q2	Q3	Q4	Q5	Q6	Q7	Q8	Q9	Q10
Ans (a/b/c/d)	a	d	b	a	c	d	c	d	a, c	b

Q1. Which of the following best describes the role of an Instruction Set Architecture (ISA)?

a. Acts as the interface between hardware and software
b. Determines only the physical design of hardware
c. Provides compiler optimizations only
d. Is only concerned with operating system design

Answer: a. Acts as the interface between hardware and software

Q2. In MIPS, how many fields are present in an R-type instruction format?

a. 3
b. 4
c. 5
d. 6

Answer: d. 6

Q3. The MIPS instruction 'addi $s1, $zero, 10' belongs to which type?

a. R-type
b. I-type
c. J-type
d. Pseudo-instruction

Answer: b. I-type

Q4. What is the function code (funct) for the 'add' instruction in MIPS?

a. 32
b. 34
c. 36
d. 0

Answer: a. 32

Q5. In MIPS, the instruction 'sw $s0, 8($s2)' uses which addressing mode?

a. Immediate
b. Register Direct
c. Base Addressing
d. PC-relative

Answer: c. Base Addressing

Q6. The maximum range of a branch offset in MIPS (using 16-bit signed immediate) is:

a. ±16 KB
b. ±32 KB
c. ±64 KB
d. ±128 KB

Answer: d. ±128 KB

Q7. Which of the following instructions uses a 26-bit address field?

a. addi
b. lw
c. j
d. bne

Answer: c. j

Q8. If MIPS is modified to have only 16 registers, how many bits are needed to represent a register?

a. 2
b. 3
c. 5
d. 4

Answer: d. 4

Q9. If an assembler cannot fit the branch offset in 16 bits, which instruction is typically used as a workaround?

a. jr
b. jal
c. j
d. lui + ori

Answer: c. j or a. jr

Q10. Which of the following is a pseudo-instruction in MIPS?

a. add
b. li
c. mult
d. sll

Answer: b. li