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Unit-2

Digital Logic Families

A logic Family is a group of electronic logic gates constructed using one of several different designs usually with compatible logic levels and power supply characteristics with a family.

Classification of logic families based on Circuit complexity

1. SSI - Small Scale Integration < 10 components
2. MSI - Medium Scale Integration < 100 components
3. LSI - Large Scale Integration > 100 components
4. VLSI - Very large Scale Integration > 1000 component

Classification based on devices used

- Bipolar
  - Saturated
    - Resistor-transistor logic (RTL)
    - Diode Transistor logic (DTL)
    - Direct coupled transistor logic (DCTL)
    - Integrated Injection logic (I^2L)
    - High Threshold logic (HTL)
    - Transistor transistor logic (TTL)
  - Unsaturated
    - Schottky TTL
    - Emitter coupled logic (ECL)
- Unipolar
  - PMOS (P channel MOSFE
  - NMOS (N-channel MOS
  - CMOS (complementa MOSFET

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✱ Characteristics of Digital ICs

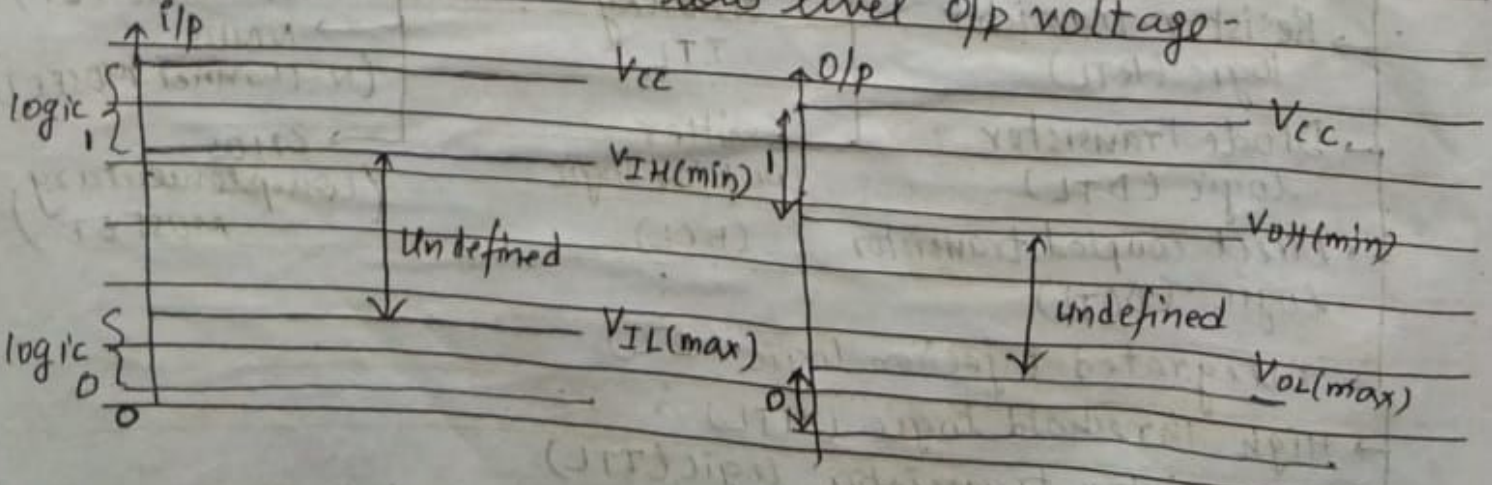
1) Voltage and current parameters:-

a) $V_{IL(max)}$ - Worst case low level i/p voltage. This is the max value of i/p voltage which will be considered as a logic 0 level. Value above $V_{IL(max)}$ will not be treated as i/p low.

b) $V_{IH(min)}$ - Worst case high level i/p voltage - This is the min value of i/p voltage which will be considered as a logic 1 level.

c) $V_{OH(min)}$ - Worst case high level o/p voltage - This is the min value of o/p voltage which will be considered as a logic high (1) level.

d) $V_{OL(max)}$ - Worst case low level o/p voltage -



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e) I_{IL} - Low level i/p current - It is the current that flows into the i/p when a low level i/p voltage in the specified range is applied.

f) I_{IH} - High level i/p current

g) I_{OL} - Low level o/p current - This is the current that flows from the o/p when the o/p voltage is in the specified low voltage range.

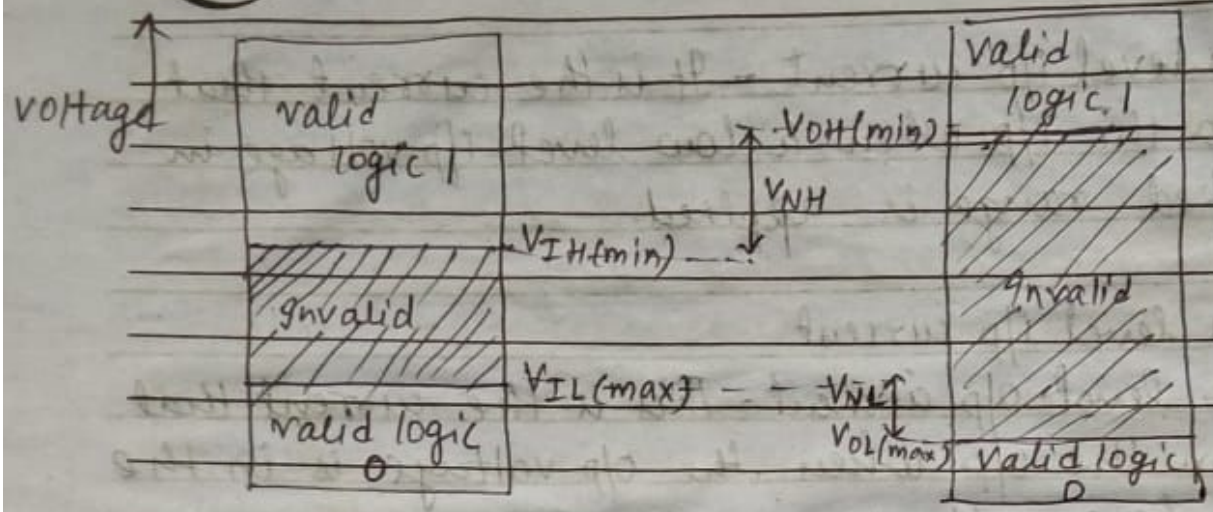
h) I_{OH} - High level o/p current.

2) Fan-in and Fan-out - Fan-in is defined as the no. of inputs a gate has.

Fanout is defined as the max no. of i/p's of the same IC family that a gate can drive with falling outside the specified o/p voltage limits.

3) Noise Margin - Noise is an unwanted electrical disturbance which may induce some voltage in the connecting wires used b/w 2 gates. Noise immunity is defined as the ability of a logic circuit to tolerate the noise without causing any unwanted changes in the o/p.

A quantitative measure of noise immunity is called as Noise margin.



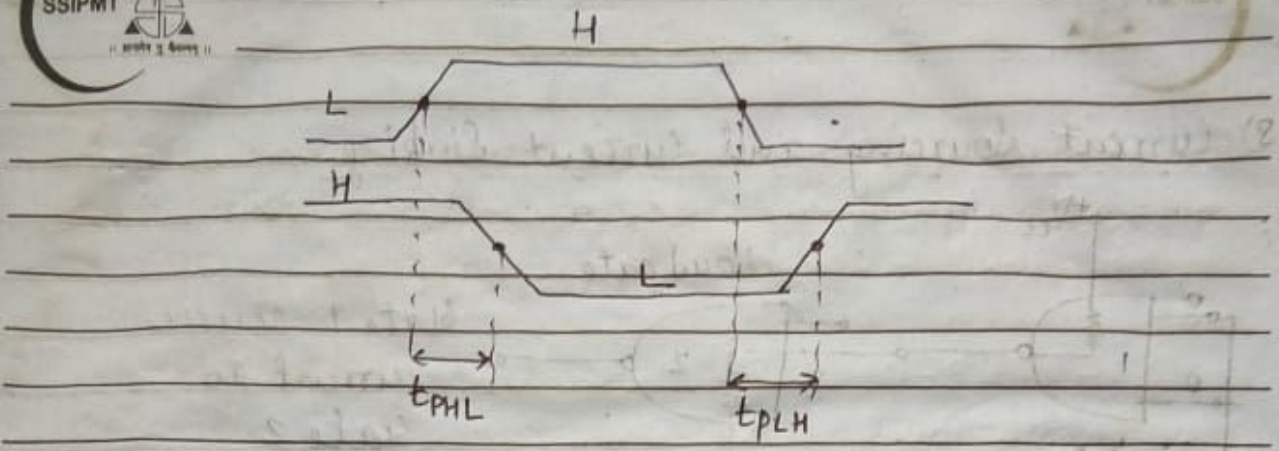
i/p Profile o/p profile

V_{NH} - High level noise margin = $V_{OH(min)} - V_{IH(min)}$

V_{NL} - low level noise margin = $V_{IL(max)} - V_{OL(max)}$

4) Propagation Delay - The o/p of a logic gate does not change its state instantaneously in response to the change in the state of its i/p. There is a time delay between these 2 events, which is called as the propagation delay.

Thus Propagation delay is defined as the time delay b/w the instant of application of an i/p pulse and the instant of occurence of the corresponding o/p pulse.



where t_{PHL} - Propagation delay measured when the O/p is making a transition from High(1) to low(0) state. and t_{PLH} - Propagation delay measured when the O/p is making a transition from Low(0) to High(1) state.

5) Power dissipation- As a result of applied voltage and currents flowing through the logic ICs, some power will be dissipated in it in the form of heat. It is given by - $P = V_{cc} \times I_{cc}$

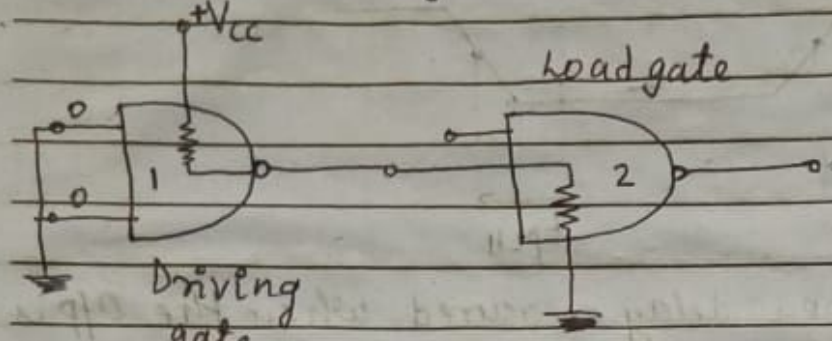
6) Operating temperature- For consumer & - 0° to 70°C
Industrial app.
- For military app - -55°C to 125°C

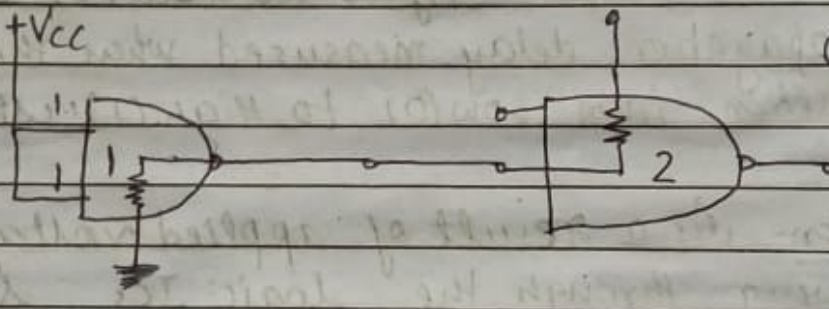
7) Figure of Merit (FOM) or Speed power product (SPP):-

FOM = Propagation delay time X Power dissipation
ns x Watt

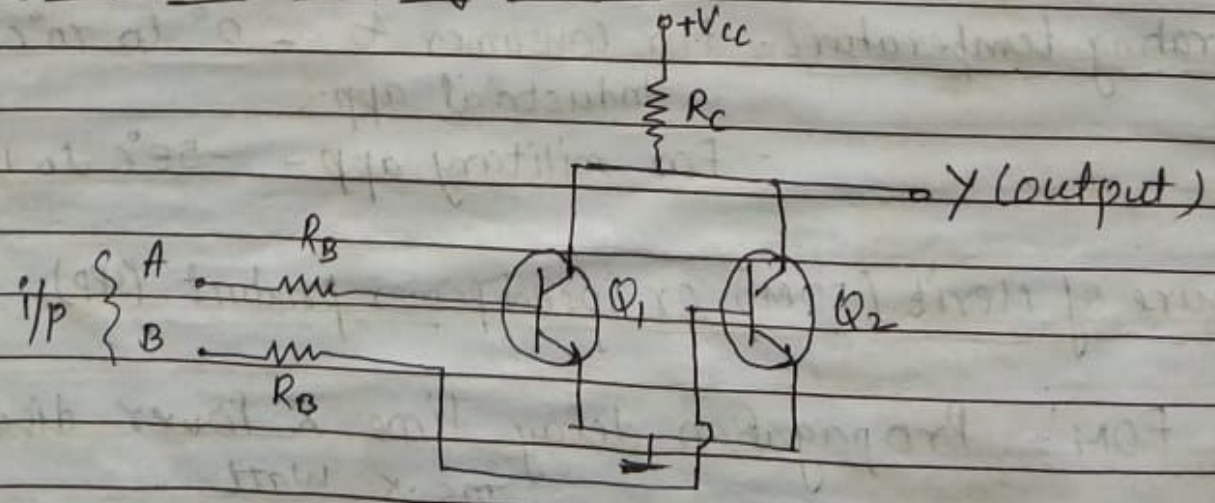
Practically FOM should be as low as possible.

8) Current Sourcing and current Sinking-





1] Resistor Transistor logic (RTL)-



2 i/p RTL NOR gate

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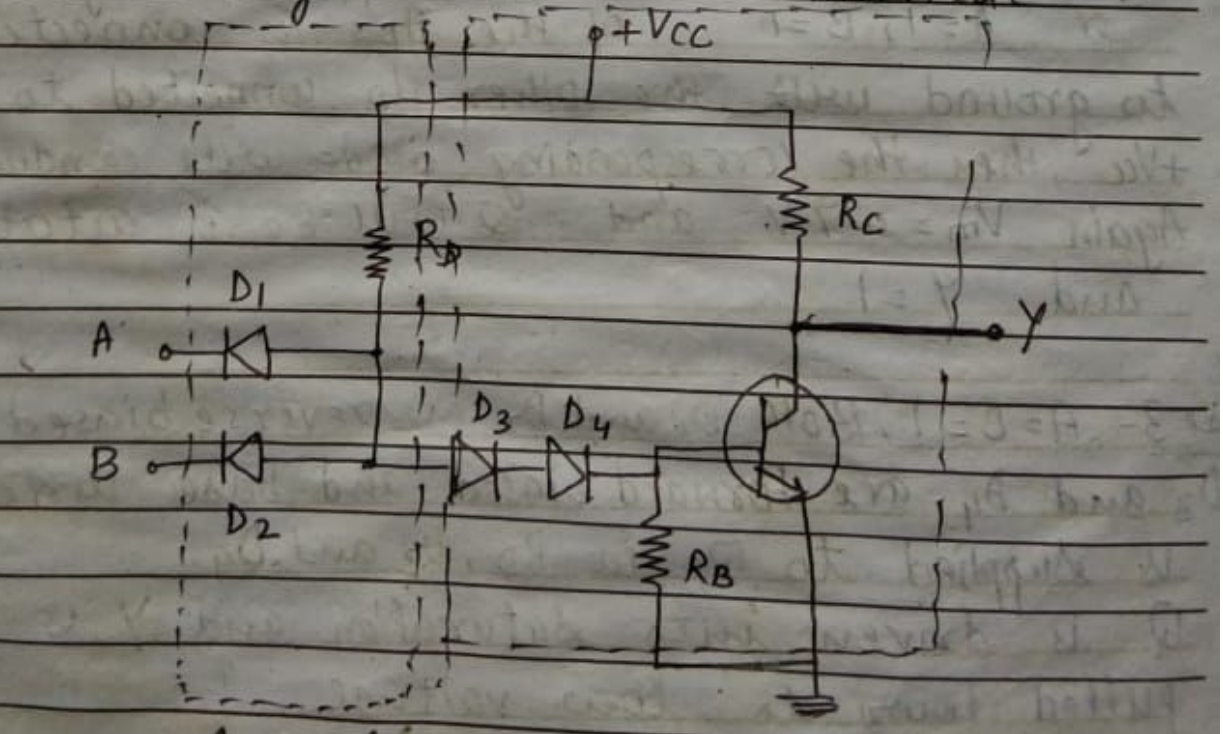
with A=B=0, both the transistors remain off. The current through R_c is zero, so drop across it is 0. So o/p voltage is equal to V_{cc} i.e. 1

Similarly with A=0, B=1, Y=0
A=1, B=0, Y=0
A=1, B=1, Y=0

Some characteristics of this logic - a) Poor noise margin
b) Poor fan out
c) Low speed
d) High Power dissipation.

2] Diode Transistor logic (DTL)



It consist of i/p stage comprising of diodes D_1, D_2 and R_D forming an AND. It is followed by a transistorized inverter.

Case 1- A=B=0, Both D_1 and D_2 will get forward biased.
Hence the potential at M is one diode voltage drop i.e. 0.7V. But to drive the transistor Q we require 2.1V to forward bias D_3, D_4 and Base emitter junction of Q. Therefore Q is cut off and O/p Y = V_{cc} = 1

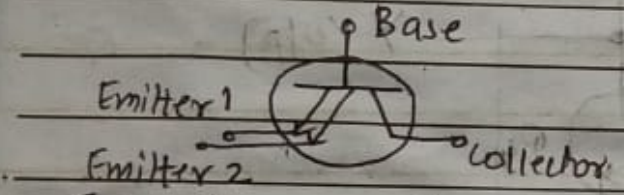
Case 2- A=0, B=1 or A=1, B=0 ⇒ In both the case any one of the i/p's is connected to ground with the other i/p connected to +V_{cc}, then the corresponding diode will conduct Again V_m = 0.7V and Q will be in cutoff and Y=1

case 3- A=B=1, Both D_1 and D_2 are reverse biased. D_3 and D_4 are forward biased and base current is supplied to Q via R_D, D_3 and D_4.
Q is driven into saturation and Y is pulled down to low voltage
Y = 0

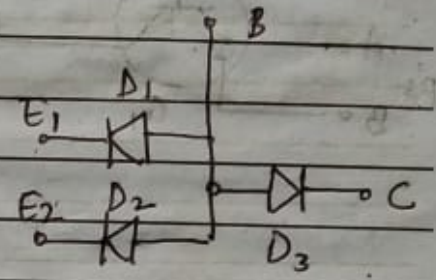
Some characteristics - (i) Greater Fan out
(ii) Greater noise immunity
(iii) Economical

3] 7400 TTL Series - It stands for transistor transistor logic

In TTL we use a special type of transistor with more than one emitter.



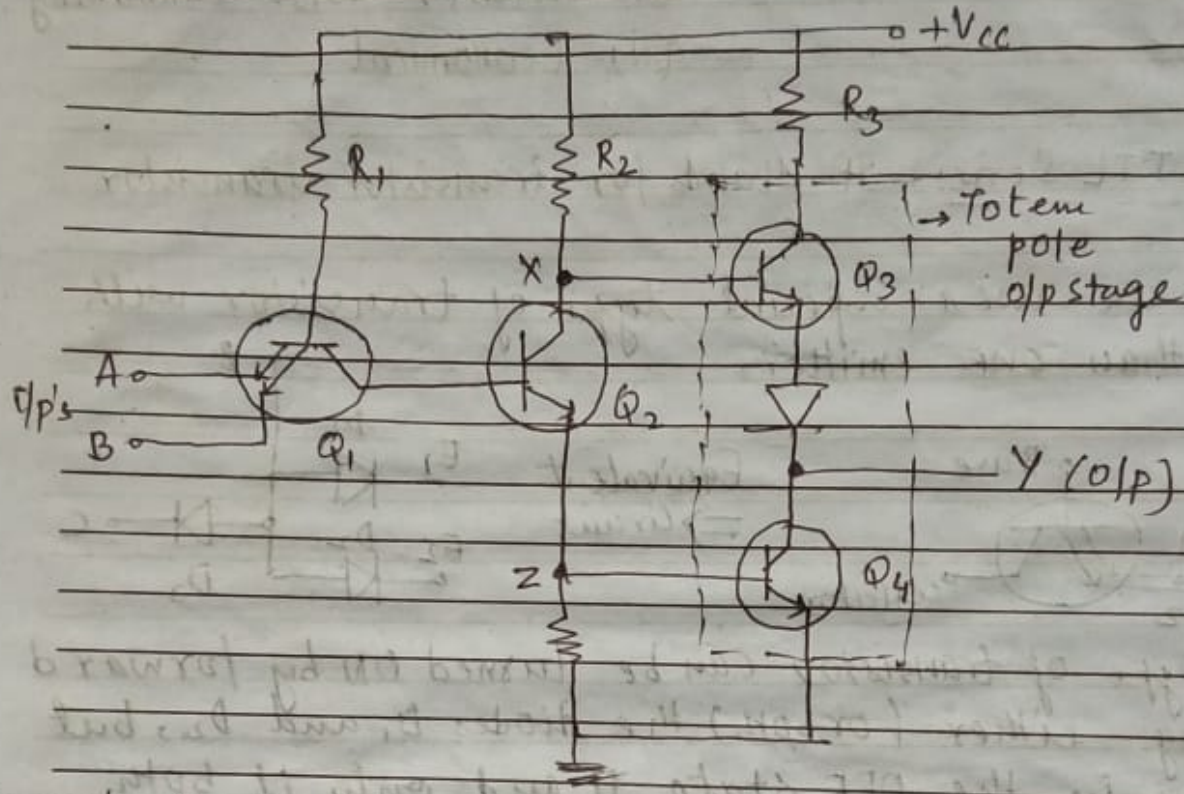
Equivalent ⇒ Circuit



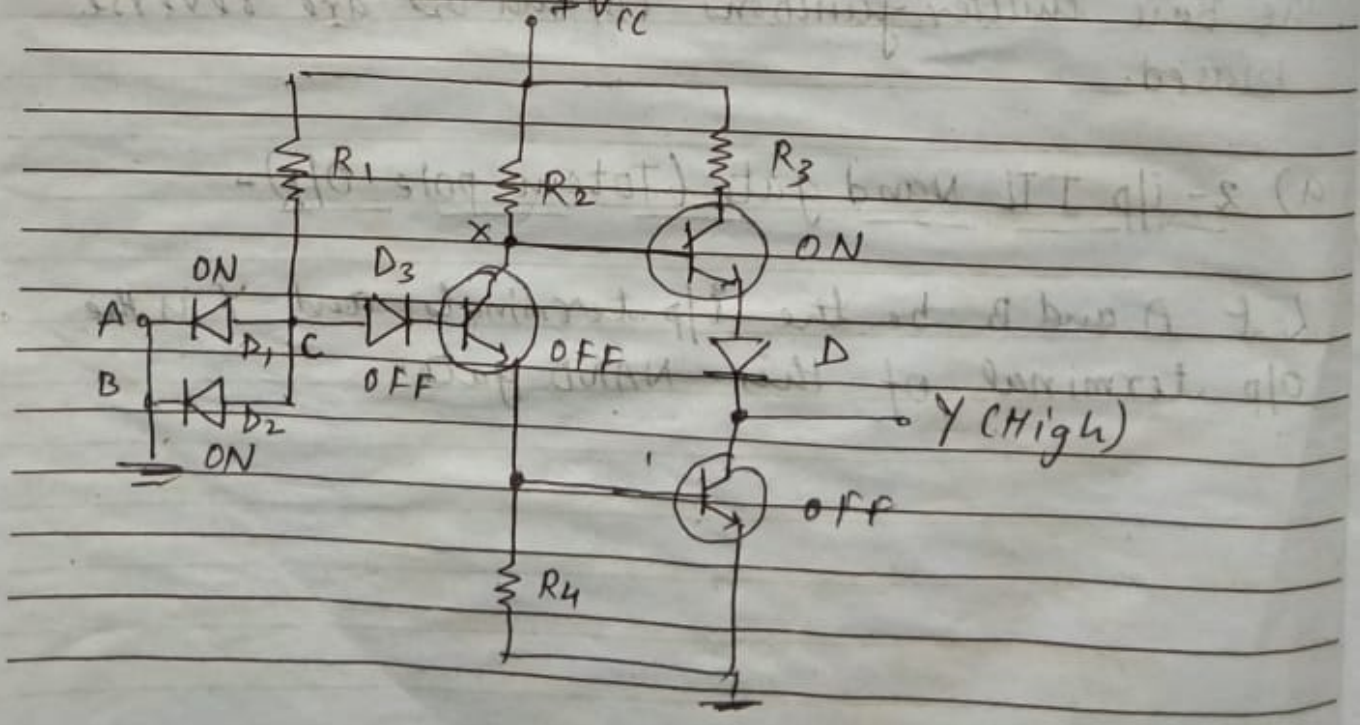
This type of transistor can be turned ON by forward biasing either (or both) the diodes D_1 and D_2, but will be in the OFF state if and only if both the Base emitter junctions (D_1 and D_2) are reverse biased.

a) 2-I/p TTL Nand gate (Totem pole O/p) -

Let A and B be the i/p terminals and Y is the o/p terminal of this NAND gate.

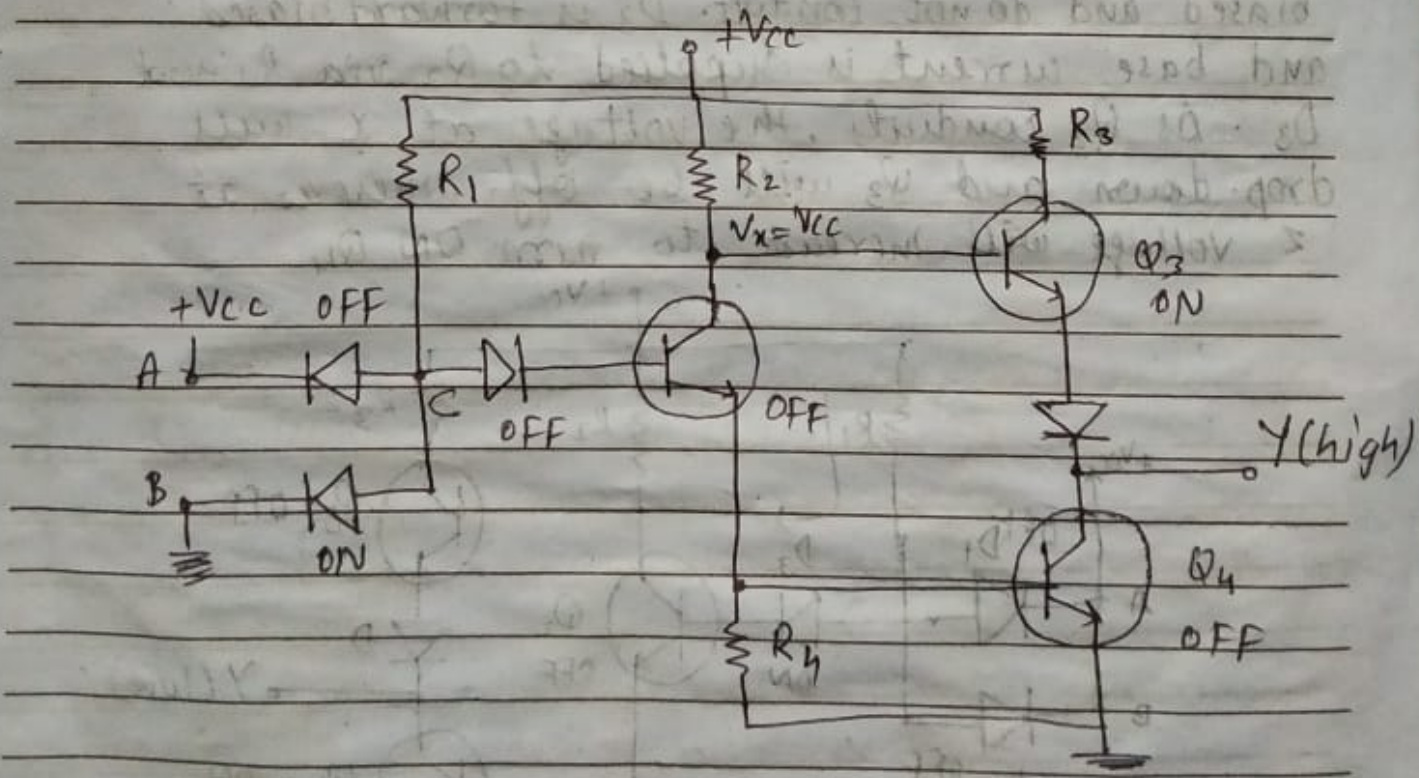

+Vcc
R3
R1
R2
Totem pole o/p stage
X
Q3
A
I/p's
B
Q2
Q1
Y (o/p)
Z
Q4

Case (i) A = B = 0


+Vcc
R1
R2
R3
X
ON
D3
A
D1
C
OFF
OFF
D
B
D2
Y (High)
ON
off
R4

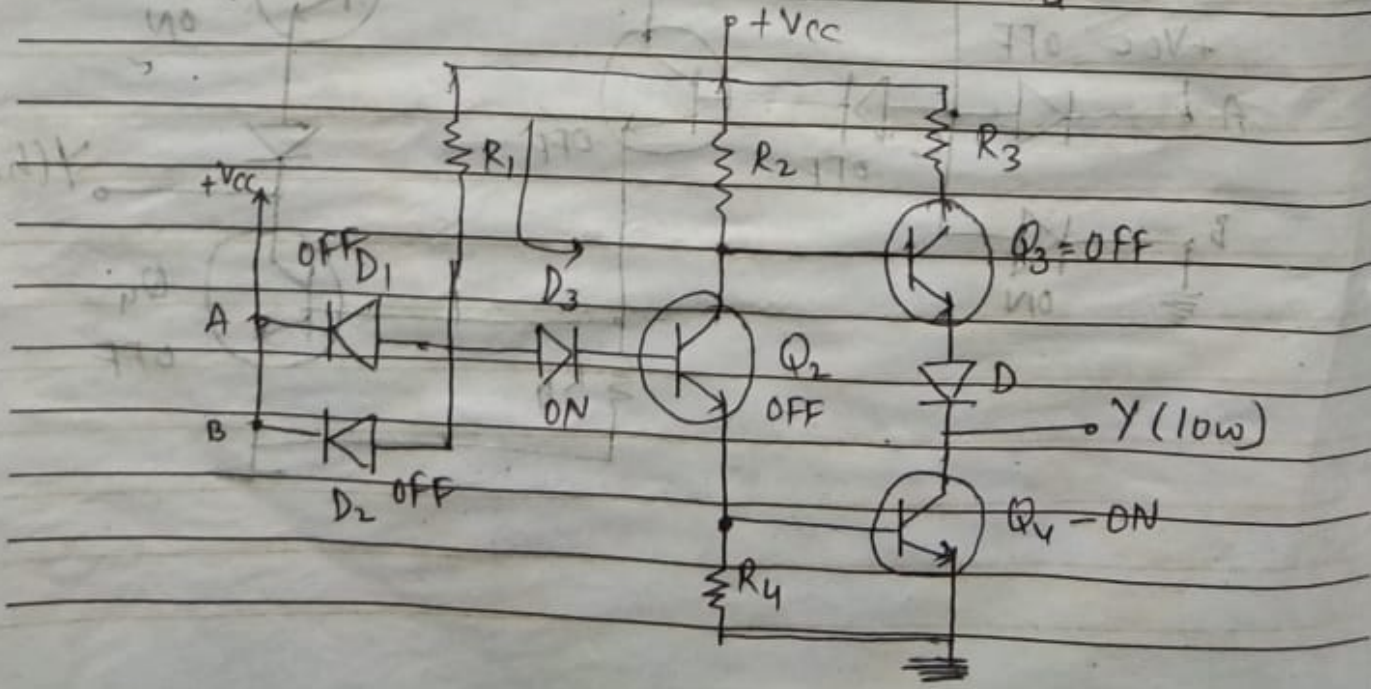
If A and B both are connected to ground then both the B-E junctions of transistor Q_1 are Forward biased.
Hence D_1 and D_2 will conduct to force the voltage at point C to 0.7 V which is insufficient to forward bias Base emitter of Q_2. Hence Q_2 remains off. Therefore its collector voltage V_x rises to V_{cc}.
Hence Y will be pulled up to high voltage
$Y = 1$ (High)

Case (ii) Either A or B Low -

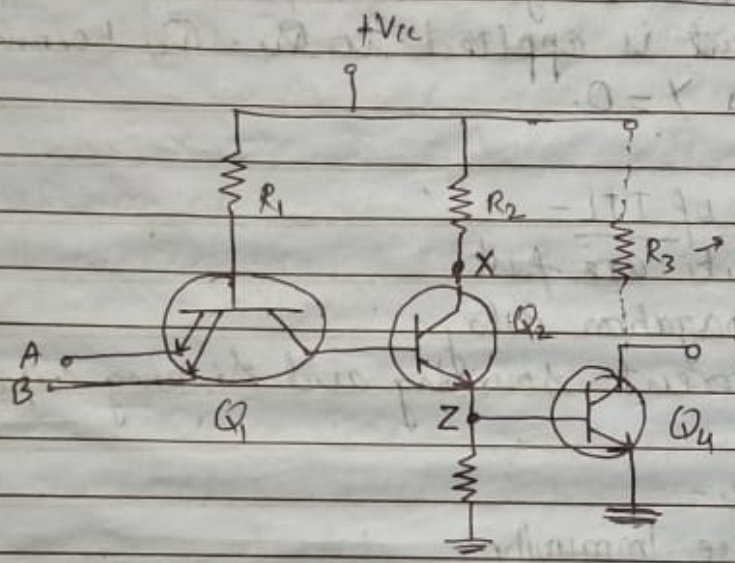


If any one i/p (A or B) is connected to ground with the other terminal left open or connected with $+V_{CC}$ then corresponding diode (D_1 or D_2) will conduct
This will pull down the voltage at C to 0.7 V which is insufficient to turn ON Q_2 so it remains OFF. So collector voltage of Q_2 will be equal to V_{CC}. So output Y will be pulled to V_{CC}
$\therefore Y = 1$

case (iii) - A = B = 1 - Both D_1 and D_2 are reverse biased and do not conduct. D_3 is forward biased and base current is supplied to Q_2 via R_1 and D_3. As Q_2 conducts, the voltage at x will drop down and Q_3 will be off, whereas at z voltage will increase to turn ON Q_4



b) Open collector outputs TTL-



In this the collector point of Q_4 is brough out as o/p

with both A=B=0, both Base emitter junction of Q_1 are forward biased so Q_2 remains off. Hence no current flows through R_4 and $V_Z = 0$ V. Therefore Q_4 is off and its collector voltage is equal to V_{cc} so Y=1

with A=0, B=1 or A=1, B=0 - One of the Base emitter junction of Q_1 is Forward biased, so Q_2 is off and Q_4 also is off. So its collector voltage is equal to V_{cc}
∴ Y=1 when any one i/p is low.

with A=B=1, Q_1 is turned off so Q_2 will be turned ON. Sufficient voltage is developed across R_4. Base current is applied to Q_4. Q_4 becomes ON. Thus Y=0.

Advantages of TTL-

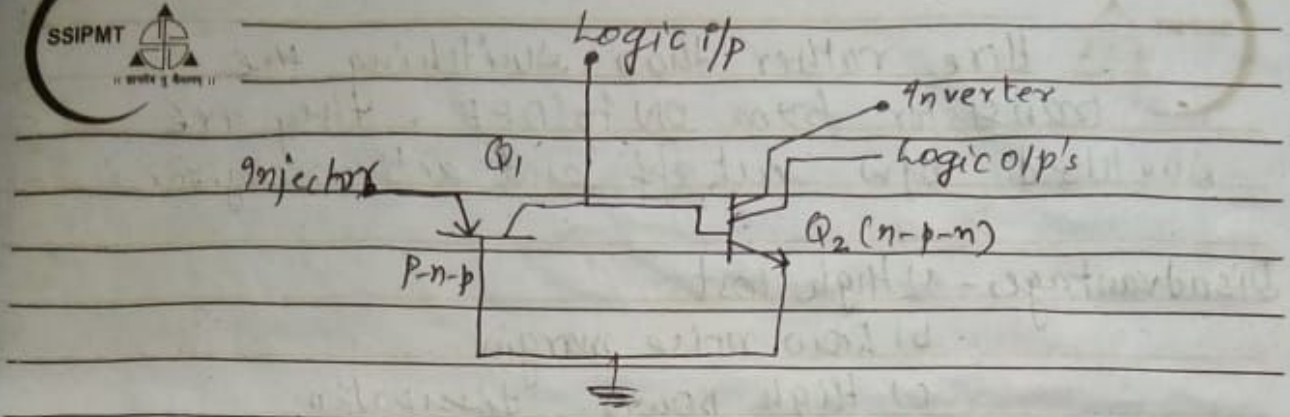
a) TTL circuits are fast.
b) Low propagation delay
c) High current sourcing and sinking capabilities

Disadvantages-

a) Poor noise immunity
b) Operates only on +5V supply
c) Large power dissipation.

4] Integrated Injection logic (I^2L) - Also called Merged transistor logic. It uses both n-p-n and p-n-p BJT to form a large no. of IC gates on a chip

Advantages- a) less power dissipation
b) High speed



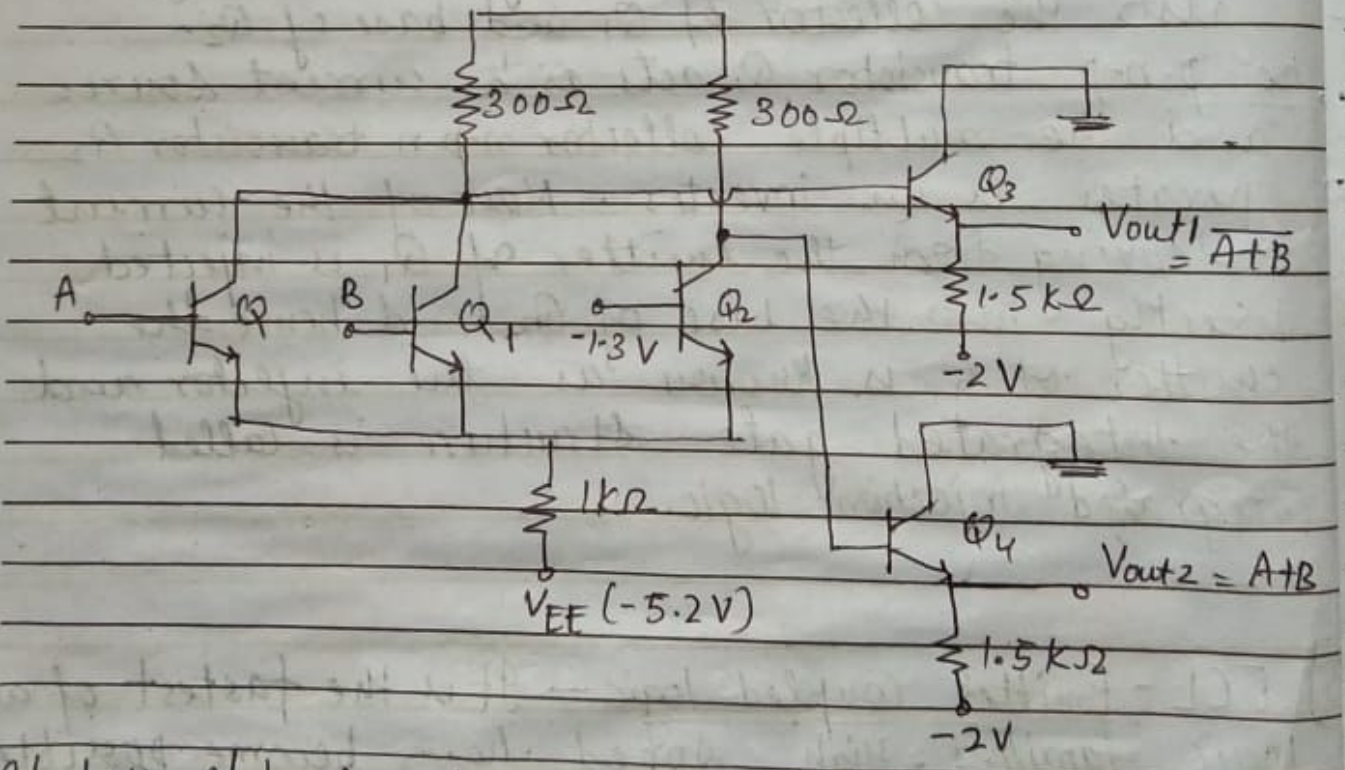
Due to the absence of resistors the I^2L inverter occupies much smaller area than a TTL inverter.
The Base of Q_1 and emitter of Q_2 are merged, so also the collector of Q_1 and base of Q_2.
The p-n-p transistor Q_1 acts as a current source and the multiple collector n-p-n transistor Q_2 operates as an inverter. Most of the current leaving from the emitter of Q_1 is injected directly into the base of Q_2 and hence the emitter of Q_1 is known as the injector and the integrated gate structure is called Integrated Injection logic.

5] ECL - Emitter coupled logic — It is the fastest of all logic families. High speed have become possible because the transistors are used in difference amplifier configuration, in which they are never driven into saturation and thereby storage time is eliminated.

Here rather than switching the transistor from ON to OFF, they are switched b/w cut off and active regions

Disadvantages - a) High cost
b) Low noise margin
c) High power dissipation.

Basic ECL OR/NOR circuit



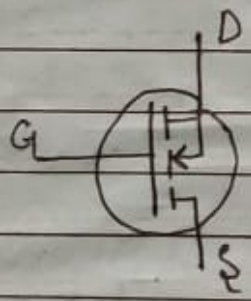
If both i/p's A and B are low then both Q and Q1 are OFF while Q2 is in active region and its collector is in a low state.

If either A or B is High, then accordingly either Q and Q_1 conducts and Q_2 becomes OFF resulting in High state at its collector

Transistor Q_3 and Q_4 provide the necessary dc shift for voltage correction. Thus if the O/p is taken from V_{out1}, the circuit acts as a NOR gate and if the O/p is taken at V_{out2}, it acts as an OR gate.

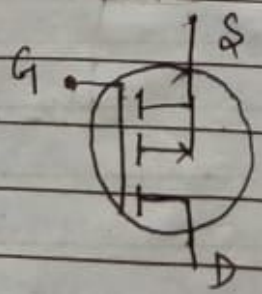
6] CMOS logic - A CMOS circuit consist of a NMOS and PMOS component

A NMOS or N-Channel MOSFET looks like this



G - Gate
S - Source
D - Drain

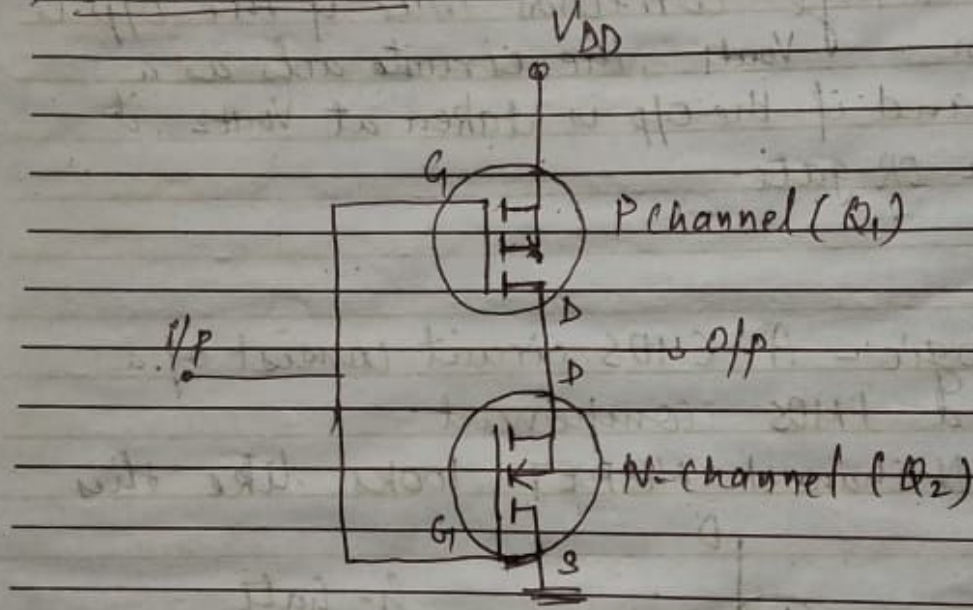
A PMOS or P-Channel MOSFET looks like this

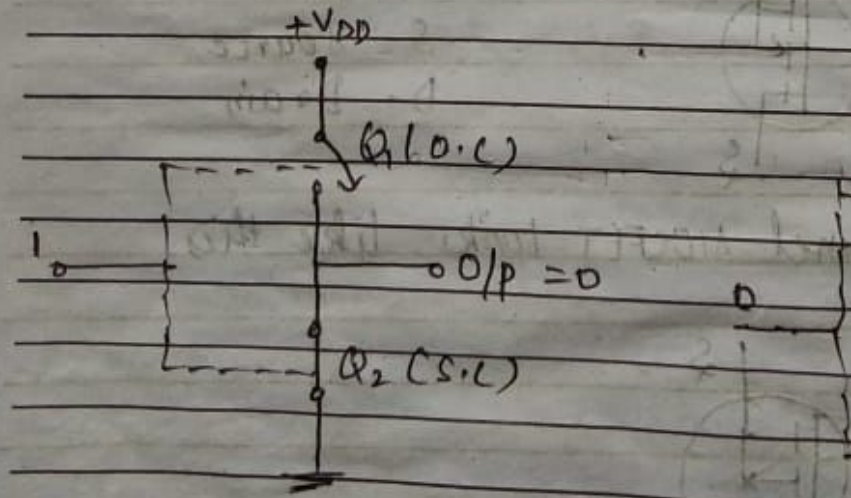


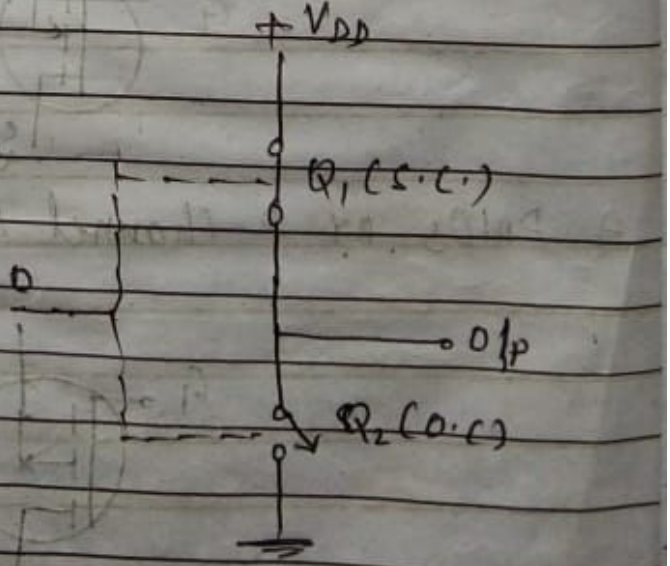
Advantages:- a) High speed
b) Low power dissipation

Disadvantages:- a) Complex
b) Lowest packaging density.

a) CMOS Inverter-







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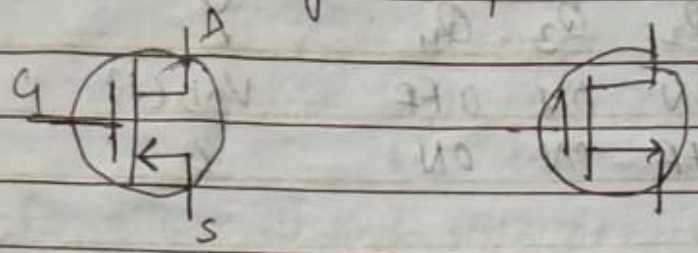
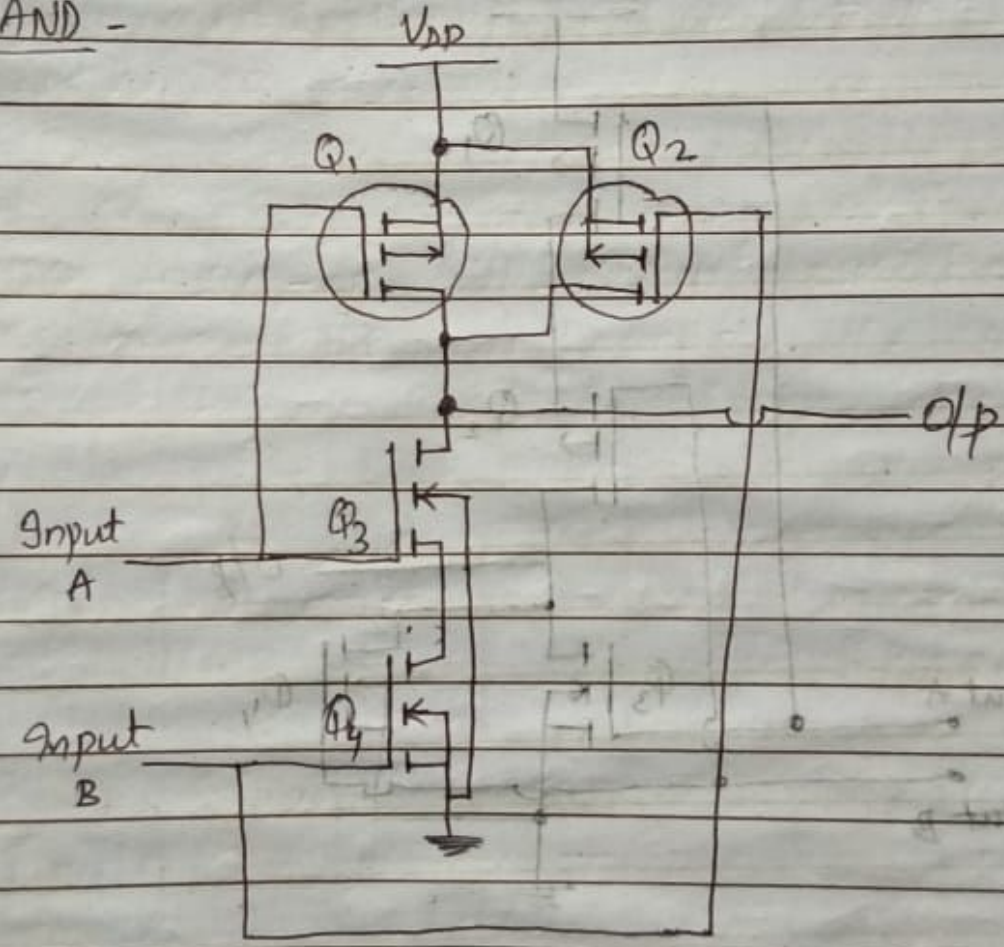
Alternate Symbol for PMOS and NMOS



PMOS NMOS

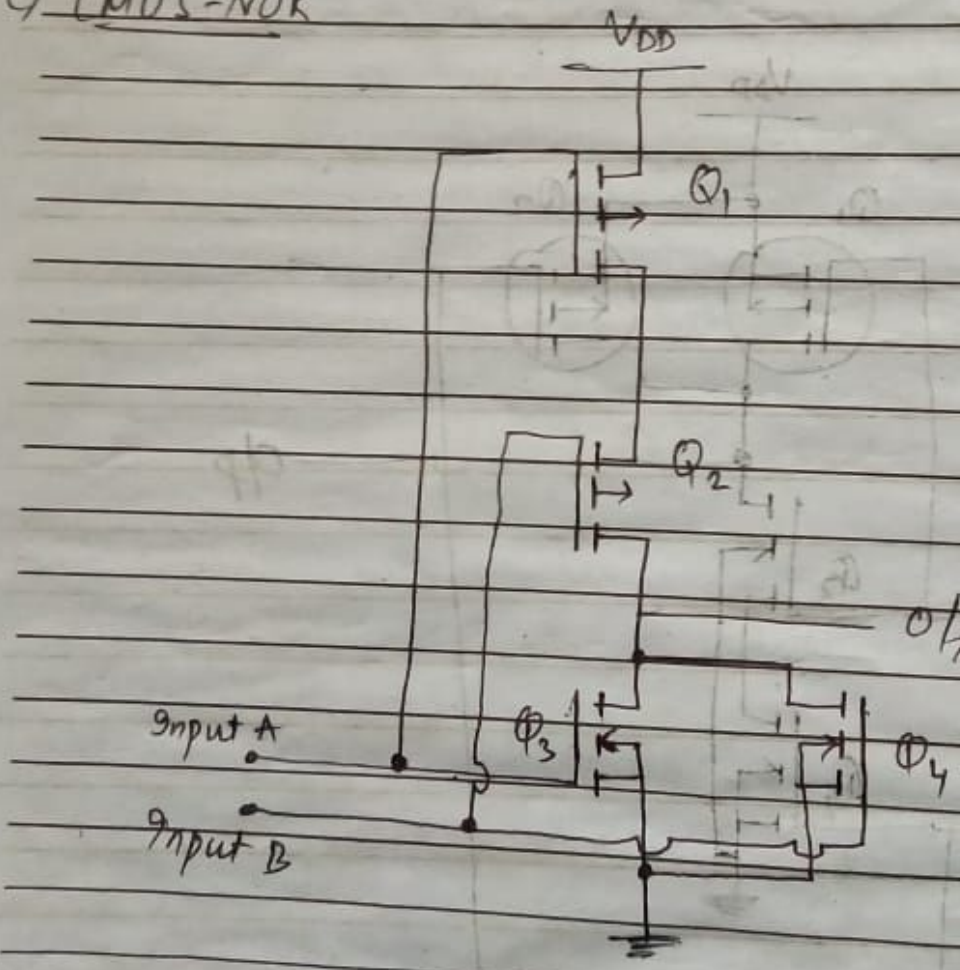
b) CMOS NAND -



I/P		States of MOS devices				O/P
A	B	Q_1	Q_2	Q_3	Q_4	Y
0	0	ON	ON	OFF	OFF	V_{DD} (1)
0	V_{DD}(1)	ON	OFF	OFF	ON	V_{DD} (1)

A	B	Q_1	Q_2	Q_3	Q_4	Y
V_{DD}	0	OFF	ON	ON	OFF	V_{DD} (1)
V_{DD}	V_{DD}	OFF	OFF	ON	ON	0

c) CMOS-NOR



I/P		State of MOS				O/P
A	B	Q_1	Q_2	Q_3	Q_4	Y
0	0	ON	ON	OFF	OFF	V_{DD} (1)
0	V_{DD}	ON	OFF	OFF	ON	0
V_{DD}	0	OFF	ON	ON	OFF	0
V_{DD}	V_{DD}	OFF	OFF	ON	ON	0

★ Comparison of various logic families

Parameter	RTL	DTL	TTL	IIL	ECL	CMOS
Basic Gate	NOR	NAND	NAND	NAND	OR/NOR	NOR/NAND
Fanout	5	8	10	12	25	50
Fan In	3	10	8	5	5	8
Power (mW) dissipated	15	12	10	0.1	40-55	0.010
Noise Immunity (V)	0.2-0.4	0.7	0.4	0.35	0.4	5
Propagation delay (ns)	12	30	6-12	0.7-20	1-4	70
Cost	Avg	Avg	Low	very low	High	Low