Indian Institute of Technology, Delhi

FALL, 2012

CSL 211: COMPUTER ARCHITECTURE

Minor 1

One and Half Hours

NOTE:
- All answers need to be brief and to the point.
- Please make any assumptions that you deem to be reasonable.
- Whenever we ask you to write ARM code, write the basic functionality.
- Enclose your final answer in a rectangular box, e.g., answer
- **NO QUESTIONS WILL BE ANSWERED**

Total Marks: 50
Total Number of Pages : 2

Easy

1. Very briefly answer the following(1-2 lines): (10 marks)

(a) If machine A runs at 5 Ghz, and machine B runs at 4 GHz. Can we say that machine A is faster than machine B? Why or why not?

(b) What is Amdahl's Law?

(c) The power dissipated by a processor is proportional to a function of three variables. What is the relationship?

(d) What is the structure of the CPSR in ARM?

(e) What is the difference between computer architecture and organization?

2. Compare the performance of $\mathcal{D}$, $\mathcal{D}_1$, $\mathcal{D}_2$. (5 marks)

Design	Instruction Type 1		Instruction Type 2		Clock Cycle
	Frequency(%)	CPI	Frequency (%)	CPI	Time
$\mathcal{D}$	80	2	20	1	1
$\mathcal{D}_1$	80	2.6	20	0.7	0.8
$\mathcal{D}_2$	80	1.2	20	1.3	1.2

Medium

3. You are given a 32 bit binary number in register R1. You want to check if the number is a palindrome. This means that the number is the same if it is read forwards or backwards. For example, the 4-bit sequence, 1001 is a palindrome. The 8 bit sequence 11011011 is a palindrome. You need to save 0 in R7 if the value is not a palindrome, and 1 if it is. Try to minimize the number of ARM instructions. (8 marks)

4. Consider the following instruction mix and IPCs of individual instructions for design $\mathcal{D}_1$:

Operation	Frequency(%)	IPC
ALU	45	1
Loads	20	0.5
Stores	10	0.5
Branches	25	0.5

Let us now assume in design $\mathcal{D}_2$ that 20% of the ALU operations are modified to create new instructions that directly use a loaded operand from memory, which is not used again. These new register-memory instructions have a CPI of 2. Secondly, these new instructions do not require any associated *load* instructions since they use a loaded operand from memory. Hence, *load* instructions get reduced accordingly. The extended instruction set also increases the CPI of branches by 1, but does not affect the clock cycle time. What is the ratio of the performance between the two designs, i.e. $Perf(\mathcal{D}_2)/Perf(\mathcal{D}_1)$? (7 marks)

5. Consider the $ldmfd$ and $stmfd$ instructions in ARM. These instructions take a set of 1 to 16 registers as input and load or store them on the stack. Secondly, they can either store the registers in ascending order or in descending order. How would you succinctly represent this information in ARM's 32 bit instruction format? Try to conform as much as possible with ARM's existing instruction encoding. (5 marks)

Hard

6. Let us consider two n bit binary numbers, A, and B. Further assume that the probability of a bit being equal to 1 is p in A, and q in B. Let us consider $(A + B)$ as one large chunk(block).

(a) What are the generate and propagate functions of this block as n tends to infinity?

(b) If $p = q = \frac{1}{2}$, what are the values of these functions?

(c) What can we infer from the answer to part (b) regarding the fundamental limits of binary addition?

(5 marks)

7. Design an $O(log(n)^k)$ time algorithm to find out if a number is divisible by 3. Try to minimize k. (5 marks)

Research

8. Design an $O(log(uv)^2)$ algorithm to find the greatest common divisor of two binary numbers u and v. (5 marks)

[HINT: The gcd of two even numbers u and v is $2 * gcd(u/2, v/2)$]