# Strong Arm Latch Comparator

## Objective:

To design, simulate, Strong Arm Latch Comparator using eSim.

## Introduction:

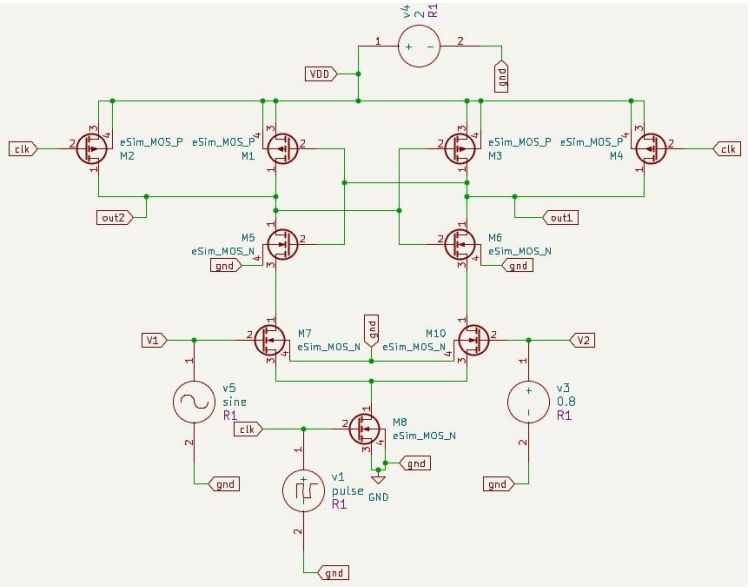
The Strong-ARM Latch is a highly popular and efficient circuit topology used as a dynamic comparator or sense amplifier in high-speed, mixed-signal applications, notably in Analog-toDigital Converters (ADCs) and static random-access memory (SRAM) arrays. It was originally introduced by Kobayashi et al. and popularized in Digital Equipment Corporation's StrongARM microprocessor, which gives the circuit its name.

Its three key advantages over traditional comparator designs are:

- Zero Static Power Consumption: The circuit is dynamically clocked and only consumes power during the short evaluation phase.
- Rail-to-Rail Outputs: It directly produces full-swing output voltages (from Vss to Vdd), which are directly compatible with digital logic gates.
- High Sensitivity: Its architecture relies on a fast, regenerative positive feedback loop, allowing for rapid decision-making even with very small differential input voltages.

The core operation involves two phases controlled by a clock signal: a Pre-charge Phase (reset) and an Evaluation/Regeneration Phase (decision).

## Circuit Schematic:

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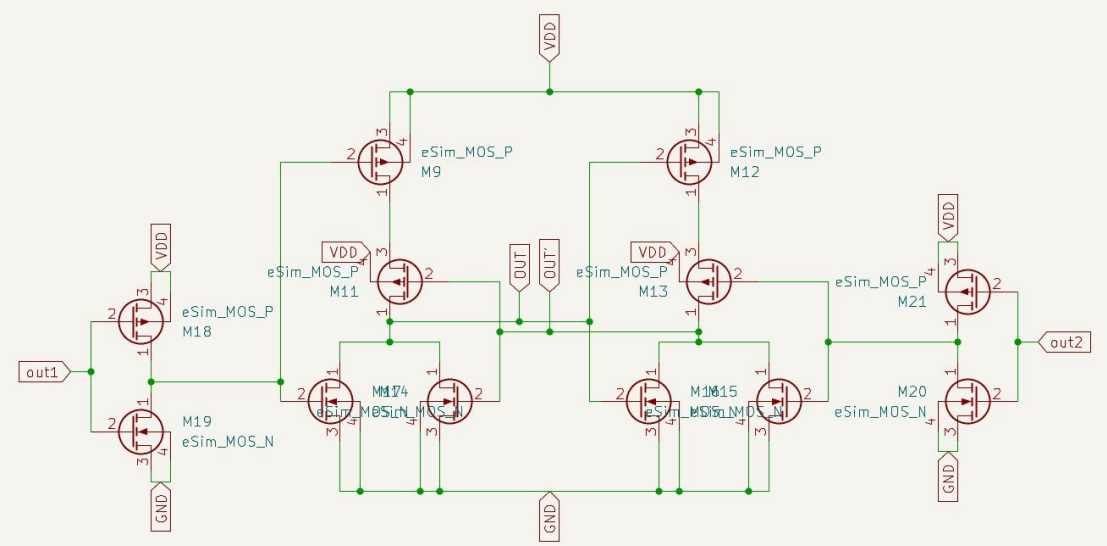
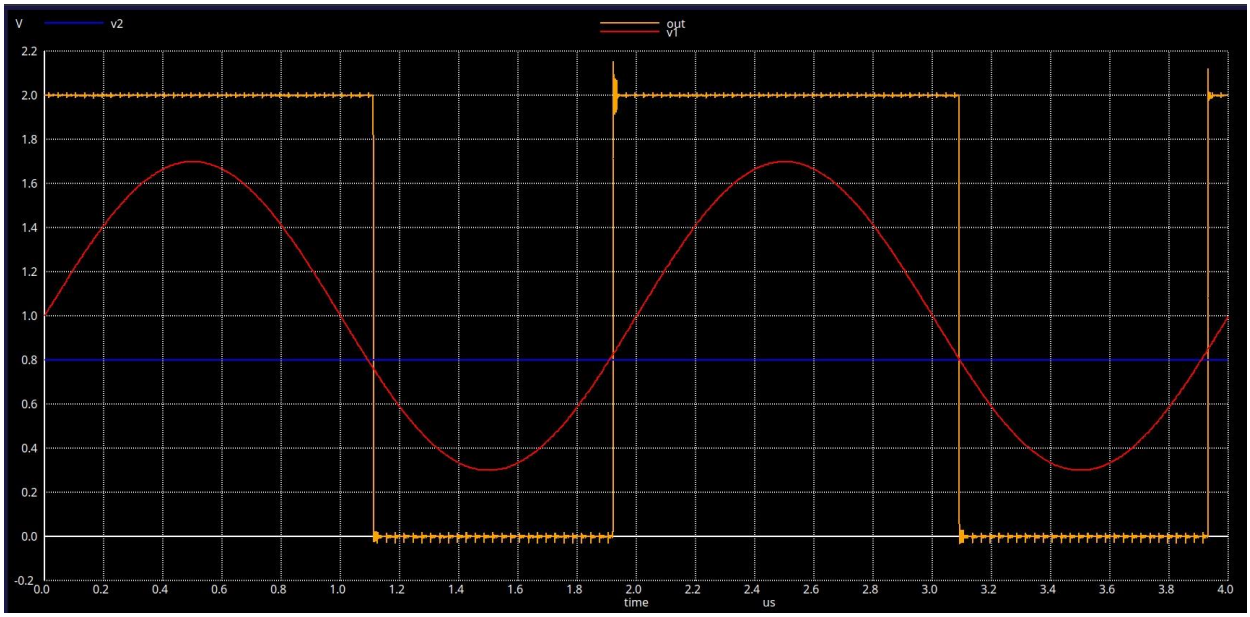



SR Latch

## Simulation Result:




## Conclusion:

The Strong-ARM Latch is a superior solution for high-speed dynamic comparison, achieving excellent performance by resolving the fundamental trade-off between speed and static power consumption. While the total decision delay is governed by the logarithmic time constant of the regenerative phase, the circuit's inherent sensitivity and full-swing output make it a highly valuable and widely adopted component in modern integrated circuits, particularly for demanding applications like high-speed Analog-to-Digital Converters (ADCs).

https://github.com/Harsshit-G/Strong-Arm-Latch-Comparator.git