BK7238 Datasheet

DS-BK7238-E08 V1.4

2023/4/28

Contents

1. Features

Wi-Fi

- IEEE 802.11 b/g/n 1x1 compliant
- Supports 20 MHz channel
- STBC supported
- Working mode STA, AP, Direct
- Concurrent AP + STA
- TX power up to +19 dBm
- RX sensitivity -99 dBm

Bluetooth Low Energy

- Bluetooth 5.2
- Bluetooth Low Energy (LE), 1 Mbps, 2 Mbps, and long range (125 kbps and 500 kbps)
- Advertising extensions
- Bluetooth direction finding: Angle of Arrival (AoA) and Angle of Departure (AoD)
- Supports an antenna array with up to sixteen antennae for precise indoor positioning
- Integrated Bluetooth LE/WLAN coexistence (PTA)

Core and Memory

- 32-bit MCU at up to 160 MHz
- SiP Flash options: 1 MB, 2 MB or none (depending on package)
- 288 KB RAM
- 4-byte eFuse
- UART/JTAG for download and debug

Clock Management

- External oscillator: 26 MHz crystal oscillator (X26M)
- Internal oscillator: 26 ~ 160 MHz digitally controlled oscillator (DCO), 32 kHz ring oscillator (ROSC)
- 480 MHz DPLL

Power Management

- 2.7 to 3.6 V VBAT supply

- On-chip power-on reset (POR) and brown-out detector (BOD)
- Embedded LDO regulators
- Low power consumption:
  - Active mode RX: 30 mA
  - Normal standby mode: 300 µA
  - Low voltage standby mode: 75 µA
  - Shutdown mode: 0.5 µA

Peripherals

- GPIOs: 19 in QFN32 (BK7238QN40), 19 in QFN32 (BK7238QN32), 9 in QFN20 (BK7238QN20)
- 1x SPI
- 2x UART: 1 with Flash download support
- 1x I2C
- 1x general-purpose DMA controller (GDMA) with 6 channels
- 6x 32-bit PWM channel
- 10-bit SAR ADC, up to 6 channels
- 6x general-purpose 32-bit timer/counter
- 1x watchdog timer
- 1x real-time counter (RTC)
- 1x temperature sensor
- 1x true random number generator (TRNG)

Packaging

- QFN40 package, 5 x 5 mm
- QFN32 package, 4 x 4 mm
- QFN20 package, 3 x 3 mm

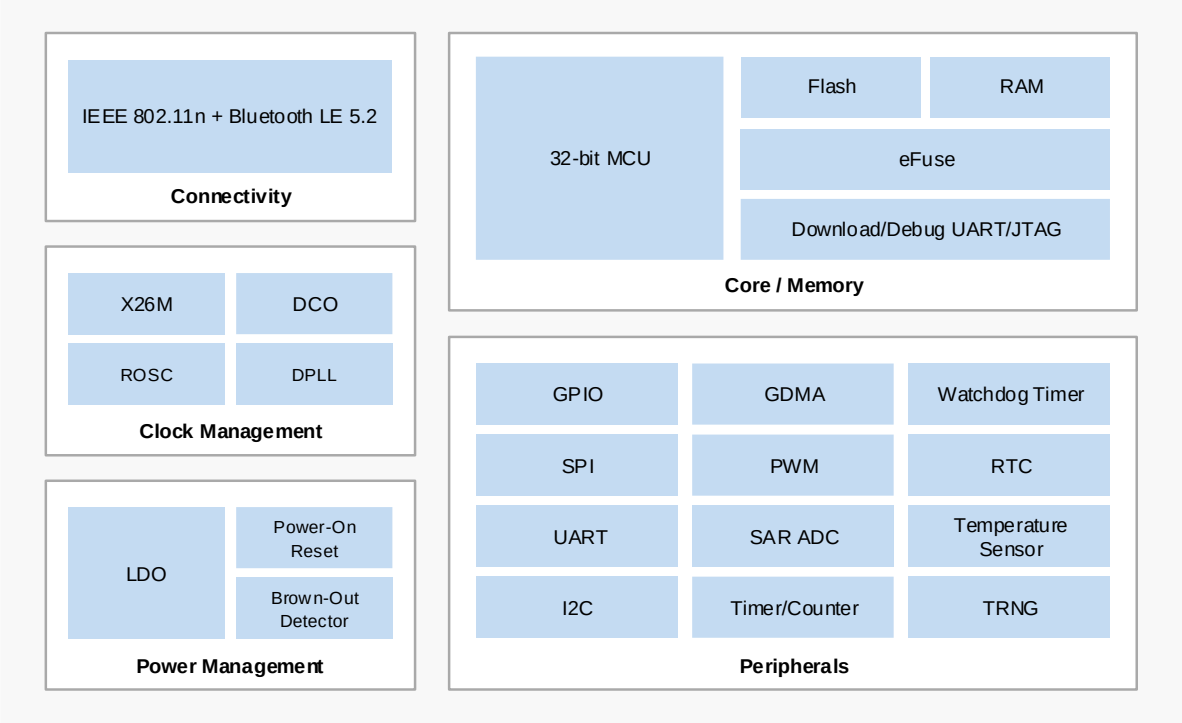
2. Overview

The BK7238 is a highly-integrated single-chip Wi-Fi 802.11n and Bluetooth Low Energy (LE) 5.2 combo solution designed for applications that require low power and compact size. The integration of a powerful 32-bit MCU and comprehensive set of peripherals and interfaces makes the BK7238 ideal for advanced Internet of Things (IoT) applications.

Using advanced design techniques and process technology, the BK7238 delivers high integration and minimal power consumption in an extremely small package for smart lighting, smart home, indoor positioning, and other complex IoT applications.

Figure 2-1 shows the general block diagram of BK7238.

Figure 2-1 BK7238 Block Diagram



The BK7238 devices are offered in several packages. The set of included peripherals varies depending on package. Table 2-1 shows the list of peripherals available on each part number.

Table 2-1 Device Options and Features

Feature	BK7238QN40	BK7238QN32	BK7238QN20
Flash	-	1 MB or 2 MB	1 MB or 2 MB
GPIO	19	19	9

Feature		BK7238QN40	BK7238QN32	BK7238QN20
SPI	Master/Slave	1	1	-
UART		2	2	2
I2C	Master/Slave	1	1	1
GDMA		Yes	Yes	Yes
PWM	PWM0 ~ 5	6	6	5
SAR ADC	10 bits	1	1	1
	Number of channels	6	6	4
Timer	General-purpose timer/counter	6	6	6
	Watchdog timer	1	1	1
	Low-power timer	1	1	1
Temperature sensor		1	1	1
TRNG		Yes	Yes	Yes
Package		5 x 5 mm QFN40	4 x 4 mm QFN32	3 x 3 mm QFN20
Operating voltage		2.7 to 3.6 V		

3. Pin Description

The BK7238 provides WLAN and Bluetooth LE functionality in several packages ranging from 20 pins to 40 pins.

3.1 BK7238QN40 Pin Description

Figure 3-1 shows the pin assignments of the 5 x 5 mm, 40-pin QFN package for BK7238QN40.

Figure 3-1 QFN40 Pin Assignments of BK7238QN40

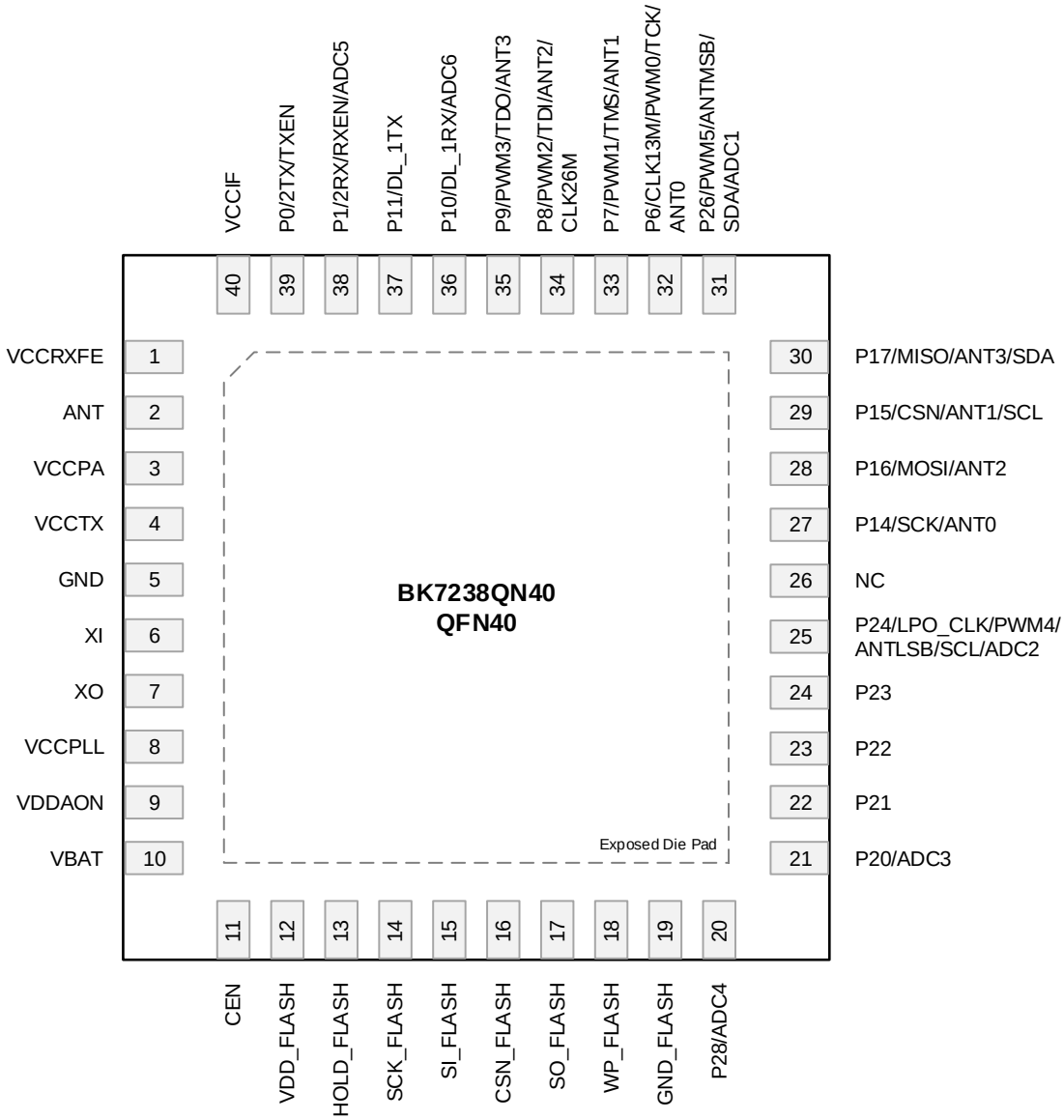


Table 3-1 shows the pin descriptions of BK7238QN40.

Table 3-1 QFN40 Pin Descriptions of BK7238QN40

Pin #	Name	I/O	Type	Description
1	VCCRXFE	-	Analog input	RF receiver power supply
2	ANT	-	RF	2.4 GHz RF signal port
3	VCCPA	-	Analog input	RF PA power supply
4	VCCTX	-	Analog input	RF transmitter power supply
5	GND	-	GND	Ground
6	XI	-	Analog input	26 MHz crystal input
7	XO	-	Analog output	26 MHz crystal output
8	VCCPLL	-	Analog input	RF PLL power supply
9	VDDAON	-	Analog output	Always ON LDO output
10	VBAT	-	Analog input	Chip power supply
11	CEN	-	Analog input	Chip enable, active high
12	VDD_FLASH	-	Analog output	External flash power supply
13	HOLD_FLASH	-	Digital input	External flash hold input
14	SCK_FLASH	-	Digital input	External flash clock input
15	SI_FLASH	-	Digital input	External flash data input
16	CSN_FLASH	-	Digital input	External flash chip select input
17	SO_FLASH	-	Digital output	External flash data output
18	WP_FLASH	-	Digital input	External flash write protect
19	GND_FLASH	-	GND	Ground
20	P28/ADC4	I/O	Digital/Analog	• GPIO28 • ADC4
21	P20/ADC3	I/O	Digital/Analog	• GPIO20 • ADC3
22	P21	I/O	Digital	GPIO21
23	P22	I/O	Digital	GPIO22
24	P23	I/O	Digital	GPIO23

Pin #	Name	I/O	Type	Description
25	P24/LPO_CLK/PWM4/ANTLSB /SCL/ADC2	I/O	Digital/Analog	• GPIO24 • 32 kHz clock output • PWM4 (differential with PWM5) • Bluetooth LE antenna selection (LSB) • I2C: SCL • ADC2
26	NC	-	NC	No connect
27	P14/SCK/ANT0	I/O	Digital	• GPIO14 • SPI: SCK • Bluetooth LE antenna selection 0
28	P16/MOSI/ANT2	I/O	Digital	• GPIO16 • SPI: MOSI • Bluetooth LE antenna selection 2
29	P15/CSN/ANT1/SCL	I/O	Digital	• GPIO15 • SPI: CSN • Bluetooth LE antenna selection 1 • I2C: SCL
30	P17/MISO/ANT3/SDA	I/O	Digital	• GPIO17 • SPI: MISO • Bluetooth LE antenna selection 3 • I2C: SDA
31	P26/PWM5/ANTMSB/SDA/AD C1	I/O	Digital/Analog	• GPIO26 • PWM5 (differential with PWM4) • Bluetooth LE antenna selection (MSB) • I2C: SDA • ADC1
32	P6/CLK13M/PWM0/TCK/ANT0	I/O	Digital	• GPIO6 • 13 MHz clock output (X26M divide by 1/2/4/8) • PWM0 (differential with PWM1) • JTAG: TCK • Bluetooth LE antenna selection 0

Pin #	Name	I/O	Type	Description
33	P7/PWM1/TMS/ANT1	I/O	Digital	• GPIO7 • PWM1 (differential with PWM0) • JTAG: TMS • Bluetooth LE antenna selection 1
34	P8/PWM2/TDI/ANT2/CLK26M	I/O	Digital	• GPIO8 • PWM2 (differential with PWM3) • JTAG: TDI • Bluetooth LE antenna selection 2 • 26 MHz clock output
35	P9/PWM3/TDO/ANT3	I/O	Digital	• GPIO9 • PWM3 (differential with PWM2) • JTAG: TDO • Bluetooth LE antenna selection 3
36	P10/DL_1RX/ADC6	I/O	Digital/Analog	• GPIO10 • UART1: RX (Flash download support) • ADC6
37	P11/DL_1TX	I/O	Digital	• GPIO11 • UART1: TX (Flash download support)
38	P1/2RX/RXEN/ADC5	I/O	Digital/Analog	• GPIO1 • UART2: RX • RX enable • ADC5
39	P0/2TX/TXEN	I/O	Digital	• GPIO0 • UART2: TX • TX enable
40	VCCIF	-	Analog input	IF power supply
Die pad	GND_SLUG	-	GND	Ground

3.2 BK7238QN32 Pin Description

Figure 3-2 shows the pin assignments of the 4 x 4 mm, 32-pin QFN package for BK7238QN32.

Figure 3-2 QFN32 Pin Assignments of BK7238QN32

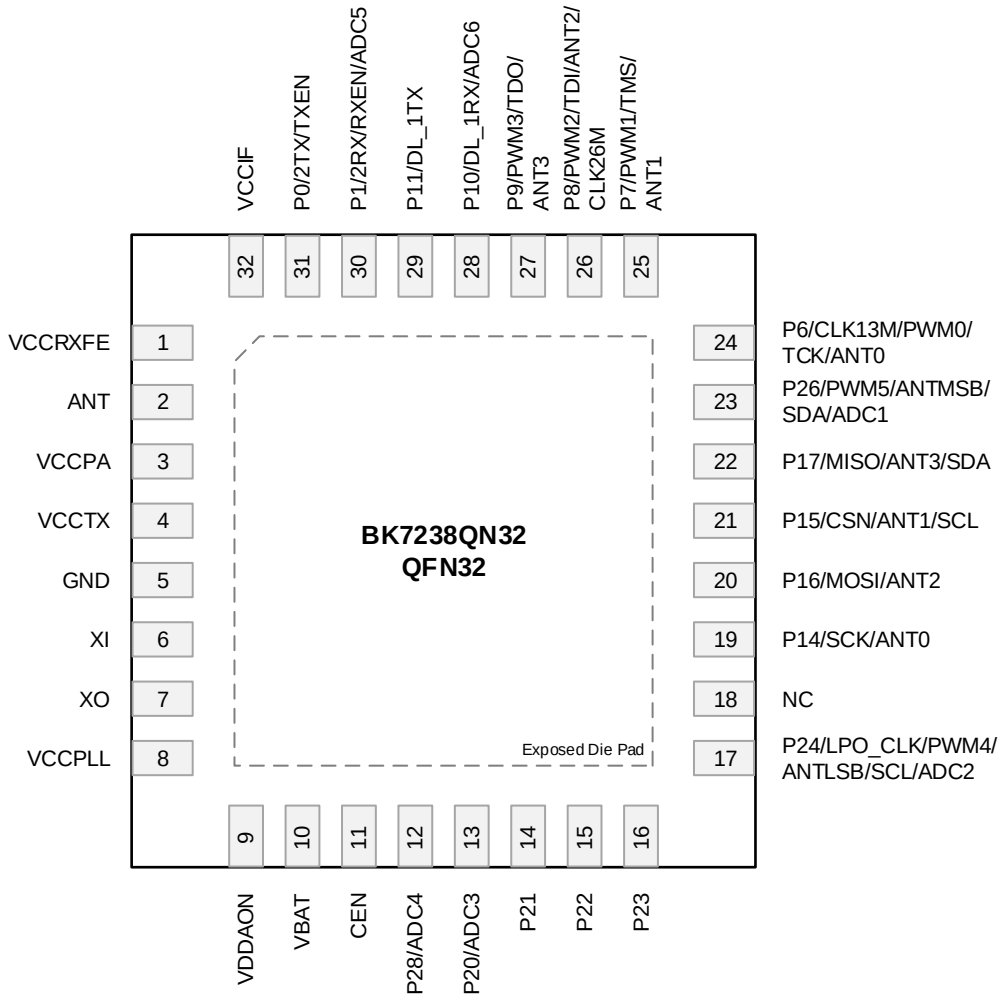


Table 3-2 shows the pin descriptions of BK7238QN32.

Table 3-2 QFN32 Pin Descriptions of BK7238QN32

Pin #	Name	I/O	Type	Description
1	VCCRXFE	-	Analog input	RF receiver power supply
2	ANT	-	RF	2.4 GHz RF signal port
3	VCCPA	-	Analog input	RF PA power supply
4	VCCTX	-	Analog input	RF Transmitter power supply
5	GND	-	GND	Ground
6	XI	-	Analog input	26 MHz crystal input
7	XO	-	Analog output	26 MHz crystal output

Pin #	Name	I/O	Type	Description
8	VCCPLL	-	Analog input	RF PLL power supply
9	VDDAON	-	Analog output	Always ON LDO output
10	VBAT	-	Analog input	Chip power supply
11	CEN	-	Analog input	Chip enable, active high
12	P28/ADC4	I/O	Digital/Analog	• GPIO28 • ADC4
13	P20/ADC3	I/O	Digital/Analog	• GPIO20 • ADC3
14	P21	I/O	Digital	GPIO21
15	P22	I/O	Digital	GPIO22
16	P23	I/O	Digital	GPIO23
17	P24/LPO_CLK/PWM4/ANTLSB /SCL/ADC2	I/O	Digital/Analog	• GPIO24 • 32 kHz clock output • PWM4 (differential with PWM5) • Bluetooth LE antenna selection (LSB) • I2C: SCL • ADC2
18	NC	-	NC	No connect
19	P14/SCK/ANT0	I/O	Digital	• GPIO14 • SPI: SCK • Bluetooth LE antenna selection 0
20	P16/MOSI/ANT2	I/O	Digital	• GPIO16 • SPI: MOSI • Bluetooth LE antenna selection 2
21	P15/CSN/ANT1/SCL	I/O	Digital	• GPIO15 • SPI: CSN • Bluetooth LE antenna selection 1 • I2C: SCL
22	P17/MISO/ANT3/SDA	I/O	Digital	• GPIO17 • SPI: MISO • Bluetooth LE antenna selection 3

Pin #	Name	I/O	Type	Description
				• I2C: SDA
23	P26/PWM5/ANTMSB/SDA/ADC1	I/O	Digital/Analog	• GPIO26 • PWM5 (differential with PWM4) • Bluetooth LE antenna selection (MSB) • I2C: SDA • ADC1
24	P6/CLK13M/PWM0/TCK/ANT0	I/O	Digital	• GPIO6 • 13 MHz clock output (X26M divide by 1/2/4/8) • PWM0 (differential with PWM1) • JTAG: TCK • Bluetooth LE antenna selection 0
25	P7/PWM1/TMS/ANT1	I/O	Digital	• GPIO7 • PWM1 (differential with PWM0) • JTAG: TMS • Bluetooth LE antenna selection 1
26	P8/PWM2/TDI/ANT2/CLK26M	I/O	Digital	• GPIO8 • PWM2 (differential with PWM3) • JTAG: TDI • Bluetooth LE antenna selection 2 • 26 MHz clock output
27	P9/PWM3/TDO/ANT3	I/O	Digital	• GPIO9 • PWM3 (differential with PWM2) • JTAG: TDO • Bluetooth LE antenna selection 3
28	P10/DL_1RX/ADC6	I/O	Digital/Analog	• GPIO10 • UART1: RX (Flash download support) • ADC6
29	P11/DL_1TX	I/O	Digital	• GPIO11 • UART1: TX (Flash download support)
30	P1/2RX/RXEN/ADC5	I/O	Digital/Analog	• GPIO1 • UART2: RX

Pin #	Name	I/O	Type	Description
				• RX enable • ADC5
31	P0/2TX/TXEN	I/O	Digital	• GPIO0 • UART2: TX • TX enable
32	VCCIF	-	Analog input	IF power supply
Die pad	GND_SLUG	-	GND	Ground

3.3 BK7238QN20 Pin Description

Figure 3-3 shows the pin assignments of the 3 x 3 mm, 20-pin QFN package for BK7238QN20.

Figure 3-3 QFN20 Pin Assignments of BK7238QN20

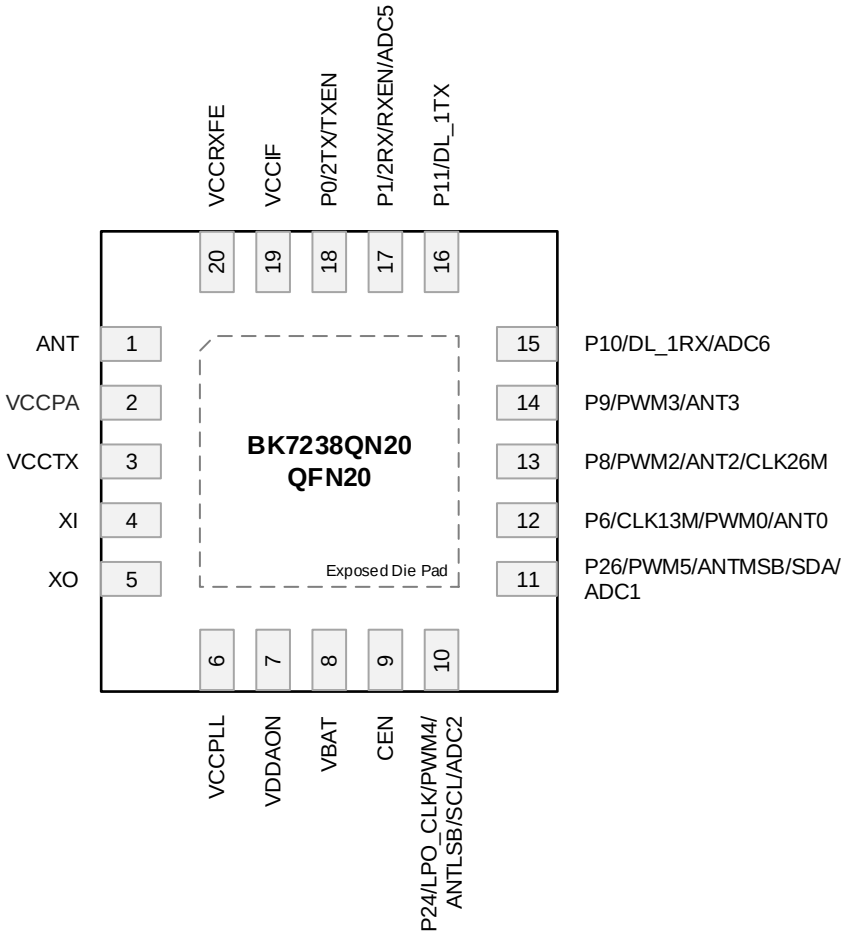


Table 3-3 shows the pin descriptions of BK7238QN20.

Table 3-3 QFN20 Pin Descriptions of BK7238QN20

Pin #	Name	I/O	Type	Description
1	ANT	-	RF	2.4 GHz RF signal port
2	VCCPA	-	Analog input	RF PA power supply
3	VCCTX	-	Analog input	RF Transmitter power supply
4	XI	-	Analog input	26 MHz crystal input
5	XO	-	Analog output	26 MHz crystal output
6	VCCPLL	-	Analog input	RF PLL power supply
7	VDDAON	-	Analog output	Always ON digital LDO output
8	VBAT	-	Analog input	Chip power supply
9	CEN	-	Analog input	Chip enable, active high
10	P24/LPO_CLK/PWM4/ANTLSB /SCL/ADC2	I/O	Digital/Analog	• GPIO24 • 32 kHz clock output • PWM4 (differential with PWM5) • Bluetooth LE antenna selection (LSB) • I2C: SCL • ADC2
11	P26/PWM5/ANTMSB/SDA/ ADC1	I/O	Digital/Analog	• GPIO26 • PWM5 (differential with PWM4) • Bluetooth LE antenna selection (MSB) • I2C: SDA • ADC1
12	P6/CLK13M/PWM0/ANT0	I/O	Digital	• GPIO6 • 13 MHz clock output (X26M divided by 1/2/4/8) • PWM0 • Bluetooth LE antenna selection 0
13	P8/PWM2/ANT2/CLK26M	I/O	Digital	• GPIO8 • PWM2 (differential with PWM3) • Bluetooth LE antenna selection 2

Pin #	Name	I/O	Type	Description
				• 26 MHz clock output
14	P9/PWM3/ANT3	I/O	Digital	• GPIO9 • PWM3 (differential with PWM2) • Bluetooth LE antenna selection 3
15	P10/DL_1RX/ADC6	I/O	Digital/Analog	• GPIO10 • UART1: RX (Flash download support) • ADC6
16	P11/DL_1TX	I/O	Digital	• GPIO11 • UART1: TX (Flash download support)
17	P1/2RX/RXEN/ADC5	I/O	Digital/Analog	• GPIO1 • UART2: RX • RX enable • ADC5
18	P0/2TX/TXEN	I/O	Digital	• GPIO0 • UART2: TX • TX enable
19	VCCIF	-	Analog input	IF power supply
20	VCCRXFE	-	Analog input	RF receiver power supply
Die pad	GND_SLUG	-	GND	Ground

4. Functional Description

4.1 Modes of Operation

The BK7238 supports four low power modes except active mode, namely shutdown mode, deep sleep mode, low voltage standby mode and normal standby mode, where shutdown mode has the lowest power consumption.

Shutdown Mode – In this mode, all circuits are turned off. A high level on the CEN pin will take the system to active mode.

Deep Sleep Mode – In this mode all circuits are powered down except GPIO and always on logic. Any GPIO edge transition or RTC timeout event can power up the system again. The retention registers can keep their contents at this mode.

Low Voltage Standby Mode – In this mode, the MCU and all digital logic stop their clocks, and their power supply decreases to a much lower retention voltage, thus the current can be much lower. In this mode, only GPIOs and the RTC timer can resume the system to active mode with normal voltage.

Normal Standby Mode – In this mode, the MCU stops running and all peripheral interrupts can resume the MCU.

Active Mode – Normal operating mode where the MCU is active and all the peripherals are available.

4.2 WLAN/Bluetooth Transceiver

The BK7238 integrates a high-performance WLAN/Bluetooth transceiver. The incorporated low noise amplifier (LNA) amplifies the single-ended input and transforms the amplified signal into a differential output for better noise and linearity trade-off. On the transmit side, the differential output of the power amplifier (PA) is combined and transformed to a single-ended output using the same on-chip balun, thus enabling only one ANT pin connection to the antenna for both transmit and receive operations. By configuring GPIO0 and GPIO1 as TXEN and RXEN functions to control external PA and LNA, the system can achieve a longer communication distance. The frequency synthesizer is fully integrated, eliminating the need for any external components.

4.3 Bluetooth LE and WLAN Coexistence

The built-in packet traffic arbitration (PTA) ensures stable Bluetooth LE and Wi-Fi dual connectivity and enables efficient sharing of over-the-air resources.

4.4 Crystal Oscillator

The BK7238 contains an integrated crystal oscillator driver circuit to drive the external 26 MHz crystal.

The 26 MHz crystal oscillator provides the reference frequency for the frequency synthesizer and can also be selected as the reference clock for internal PLLs. The startup time of the clock signal is about one milliseconds.

If an external reference clock is used, the clock input should be applied to the XI pin. Care must be taken not to overdrive the XI input with a voltage above 1.05 V.

4.5 Power-Up Sequence

Figure 4-1 shows the power-up sequence of BK7238.

Figure 4-1 BK7238 Power-Up Sequence

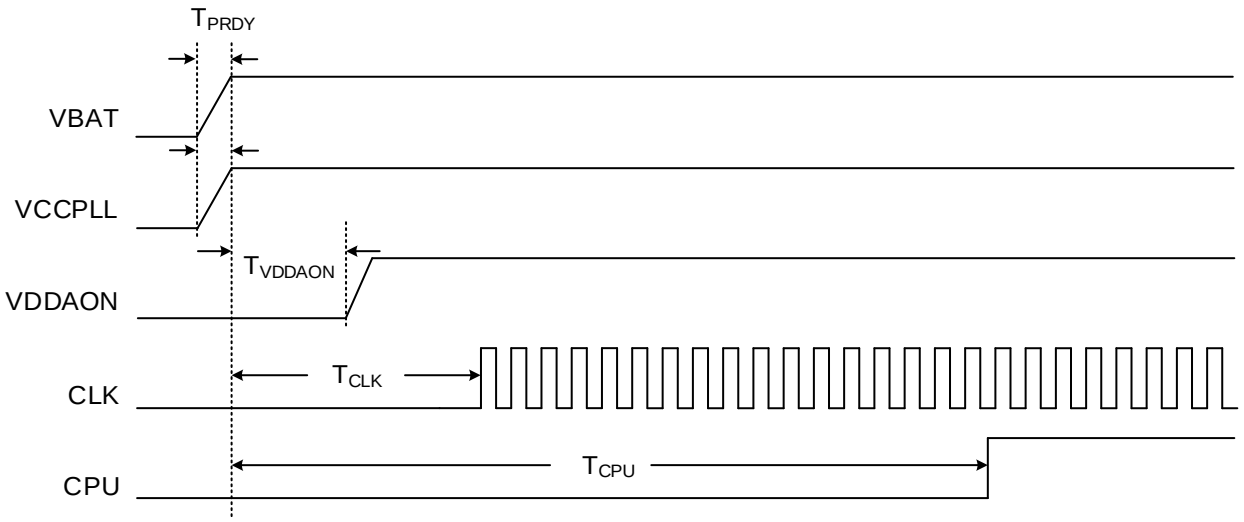


Table 4-1 Timing Parameters of BK7238 Power-Up Sequence

Parameter	Description	Min.	Typ.	Max.	Unit
T_{PRDY}	VBAT ready time	-	0.5	1.5	ms
T_{VDDAON}	Always ON digital LDO output ready time	-	0.5	1.5	ms
T_{CLK}	26 MHz clock stable time	-	3	5	ms
T_{CPU}	Application ready time	60	70	-	ms

4.6 Clock

The system has several root clock signals: X26M, DCO, D32K, ROSC and DPLL.

- X26M: High frequency 26 MHz crystal oscillator

- DCO: Internal high frequency digitally controlled oscillator, 26 MHz to 160 MHz, about ±2% variation after calibration. The startup time of the clock signal is about a few microseconds.
- D32K: 32 kHz clock signal derived from X26M
- ROSC: 32 kHz internal low frequency ring oscillator, about ±2% variation after calibration
- DPLL: High speed 480 MHz PLL clock

The clock selection options for MCU and peripherals are listed as follows.

Table 4-2 Clock Selection

MCU and Peripherals	X26M	DCO	DPLL	LPO_CLK[a]
MCU	√	√	√	√
FLASH controller	√	√	√	
SPI	√	√		
UART1	√	√		
UART2	√	√		
I2C	√	√		
PWM	√	√		√
SAR ADC	√	√		
Timer1	√			
Timer2				√
Watchdog timer				√
RTC				√

a. The low power clock (LPO_CLK) can be derived from D32K or ROSC.

The BK7238 also features the clock output capability to output clock signals for external components.

- The LPO_CLK and X26M clock can be output to GPIOs for general purpose.
- The clock derived from X26M (divide by 1/2/4/8) can be output to GPIOs for general purpose.

4.7 Reset

A reset can be triggered by the following sources: Power-on reset, brown-out reset, watchdog reset, software reset, and wakeup from shutdown mode or deep sleep mode.

System power on and watchdog reset have the same reset effect on major blocks except always on logic that any of them can reset the whole chip to initial status. The always on logic has one 32-bit timer and 16-bit retention registers, which can only be reset to initial value by system power on reset. The watchdog reset can also reset the 32-bit timer of the always on logic.

Wakeup from either shutdown mode or deep sleep mode will power on digital from power down mode, which will trigger the whole system reset procedure.

4.8 GPIO

The BK7238 has up to 19 GPIOs. Each can be configured as either input or output. Most GPIOs have alternate functions.

All GPIO pins can wake up the internal MCU from low-voltage standby mode. In low-voltage standby mode, any level change on the set GPIO will trigger the wakeup procedure.

4.9 SPI

The BK7238 integrates a SPI interface that can operate in master or slave mode. The SPI interface allows a clock frequency up to 30 MHz in master mode and 20 MHz in slave mode. The SPI interface supports a configurable 8-bit or 16-bit data width. The SPI interface supports 4-wire and 3-wire mode (without CSN pin), a 64-depth RX FIFO and a 64-depth TX FIFO with DMA capabilities.

The receive data can be latched on either rising edge or falling edge of a clock signal. The transmit data can be set by MSB or LSB first.

4.10 UART

The BK7238 includes two Universal Asynchronous Receiver/Transmitter (UART) interfaces, which offer full-duplex, asynchronous serial communication at a baud rate up to 6 Mbps. They support 5/6/7/8 bits data, and even, odd or none parity check. The stop bit can be either 1 bit or 2 bits. UART1 supports Flash download.

4.11 I2C

I2C is a popular inter-IC interface that requires only two bus lines, the serial data line (SDA) and the serial clock line (SCL). The BK7238 embeds a I2C interface, which could act as Master mode or Slave mode. It supports standard (up to 100 kbps) and fast (up to 400 kbps) modes with 7-bit addressing. If low level on SCL or bus idle duration is greater than a programmable threshold, it will generate interrupt to MCU.

4.12 GDMA

The BK7238 has a general-purpose DMA controller (GDMA) with six DMA channels to unload CPU activity. The six channels are shared by peripherals that have DMA capabilities.

The GDMA controller can perform single block transfers and repeated block transfers. Data width for destination and source can be configured as 8 bits (byte), 16 bits (half-word) or 32 bits (word). It allows peripheral to memory, memory to memory, and memory to peripheral data transfers at a high speed.

The peripherals with DMA capabilities on the BK7238 includes UART1, UART2, and SPI.

4.13 PWM

The BK7238 has six 32-bit PWM channels, labeled PWM0 ~ 5 (Timer mode supported). Each PWM channel has three modes: Timer mode, PWM mode, and Capture mode. Each mode of each channel is multiplexed with 32-bit counting. The PWM running clock can be either high speed clock or low power clock. Each PWM runs independently with its own duty cycle.

The main features of the PWM module are listed here:

- Fixed PWM base frequency with programmable 1 ~ 256 prescaler
- The counter increases in one direction and continues counting from 0 automatically when it overflows to the maximum value.
- Each channel can be individually enabled, and the mode of each channel can be individually configured.
- Capable of continuous counting between two rising edges, two falling edges or dual edges in Capture mode
- Configurable PWM period and duty-cycle for each PWM channel
- Real-time count value can be read in Timer mode.

4.13.1 Timer Mode

In Timer mode, the counter is enabled and incrementally counted, and an interrupt is generated when the specified cycle value is reached. Counting restarts from 0.

If the software refreshes the count cycle value during the counting process, the new count cycle value is used as the count cycle. If the current count value exceeds the new count cycle value, it immediately goes back to 0 and starts counting again.

The counter resets to 0 immediately if Enable = 0. If Stop = 1, the counter stops incrementing and remains its current state, and continues counting after Stop = 0.

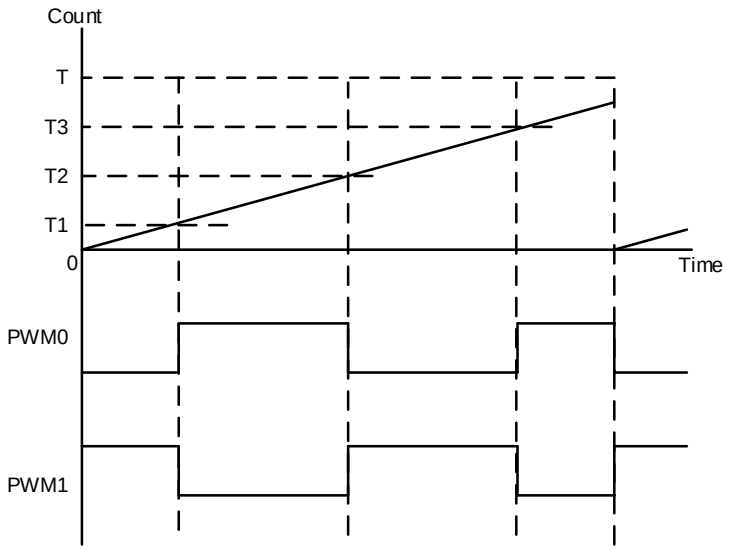
The current count value of the counter can be read in real time.

4.13.2 PWM Mode

In PWM mode, the PWM waveform start level can be configured as 0 or 1. The waveform timing is configured with four parameters.

- Waveform period T (1~2^32)
- The first level inversion time T1 (0~2^32-1, 0 - no inversion)
- The second level inversion time T2 (0~2^32-1, 0 - no inversion)
- The third level inversion time T3 (0~2^32-1, 0 - no inversion)

The six PWM channels can be configured as three pairs, and their start up time is aligned when the adjacent two channels are in paired mode (At this point, the waveform period must be configured to the same value).



As shown in the above figure, PWM0 and PWM1 have opposite start levels, share same waveform parameters, and are in paired mode.

In PWM mode, no interrupts are generated.

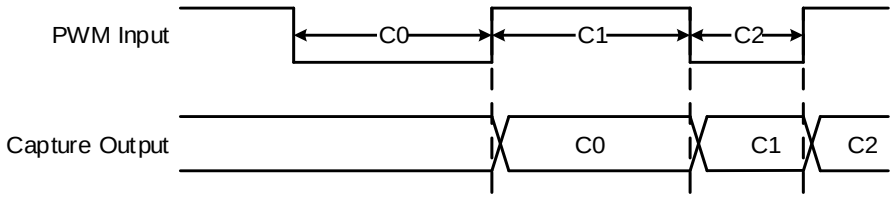
During operation, any updates to the configuration parameters will take no effect until the next time the counter starts from 0 again.

4.13.3 Capture Mode

Capture mode, which uses the operating clock to count the time between input signal edges, has the following three modes of edges:

- Rising edge: between two rising edges
- Falling edge: between two falling edges

- Dual edge: between any two edges



The figure above shows the Capture result between dual edges.

Each time there is an update to the Capture output, an interrupt is generated. The software must read out the Capture result before the next update, otherwise the Capture result will be overwritten by the new result.

4.14 General-Purpose SAR ADC

The BK7238 embeds a 10-bit general-purpose SAR ADC with programmable sampling clock ranging from 5 kHz to 26 MHz. The 10-bit resolution ADC can be configured to 12 ~ 14 bits.

The ADC supports up to six external input channels. It can operate in one-shot mode or continuous mode. The ADC supports full scale input range (0 V to VBAT) or from 0 to 3.6 V.

Table 4-3 SAR ADC Input Channel

Channel Number	Detected Voltage	Description
0	VBAT	Monitor battery voltage (VBAT)
1	ADC1	GPIO26 voltage
2	ADC2	GPIO24 voltage
3	ADC3	GPIO20 voltage
4	ADC4	GPIO28 voltage
5	ADC5	GPIO1 voltage
6	ADC6	GPIO10 voltage
7	Temperature sensor	Temperature sensor output voltage

4.15 Timers

The BK7238 includes six general-purpose timers, a watchdog timer and a real-time counter (RTC).

There are two groups of general-purpose timers, Timer1 and Timer2, and each group has three 32-bit timers. Timer1 (fast) uses 26 MHz clock as the main clock, and Timer2 (slow) uses D32K or ROSC as main clock. Each group has three 32-bit counters with a 4-bit pre-divider.

The watchdog timer runs on a 1 kHz clock derived from D32K or ROSC and has a maximum programmable period of up to 65.536 (2^16/1 kHz) seconds.

The RTC runs on ROSC. It is used for low-power timing and it can keep running even when the system is in low-voltage standby.

4.16 Temperature Sensor

The BK7238 integrates an on-chip temperature sensor. The temperature sensor can measure on-chip temperature over -40 to +125 °C with an accuracy of ±5 °C. The digital results can be read by the ADC.

Usually the software initiates calibration of a specific module based on the temperature value, narrowing the difference in chip performance at different temperatures. The host can also read the on-chip temperature and decide whether to reduce the transmit power or suspend operation at high temperatures.

4.17 True Random Number Generator (TRNG)

The random number generator module generates true, nondeterministic random numbers based on thermal noise for the purpose of creating keys, initialization vectors and nonces needed for cryptographic operations.

5. Electrical Characteristics

Note: Values currently listed in this section are preliminary measurements and are subject to change.

5.1 Absolute Maximum Ratings

Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. Exposure to absolute-maximum-rated conditions for prolonged periods may affect the reliability of the device.

Parameter	Description	Min.	Max.	Unit
VBAT	Battery regulator supply voltage	-0.3	3.6	V
P_{RX}	RX input power	-	10	dBm
T_{STR}	Storage temperature range	-55	150	℃

5.2 ESD Ratings

Parameter	Description	Test Condition	Value	Unit
ESD HBM	Electrostatic discharge voltage (human body model), per ANSI/ESDA/JEDEC JS-001-2017	ANT pin	±2000	V
		VCCPA/VCCTX/XI pins	±3000	V
		Other pins	±4000	V
ESD CDM	Electrostatic discharge voltage (charge device model), per ANSI/ESDA/JEDEC JS-002-2018	All pins	±1000	V

5.3 Recommended Operating Conditions

Parameter	Description	Min.	Typ.	Max.	Unit
VBAT	Battery/regulator supply voltage	2.7	-	3.6	V
VCCIF	Supply voltage for IF	2.7	-	3.6	V
VCCRXFE	Supply voltage for RX	2.7	-	3.6	V
VCCPA	Supply voltage for PA	2.7	-	3.6	V
VCCTX	Supply voltage for TX	2.7	-	3.6	V

Parameter	Description	Min.	Typ.	Max.	Unit
VCCPLL	Supply voltage for RF PLL	2.7	-	3.6	V
VDDAON	Always ON digital LDO output voltage	0.5	0.9	1.0	V
VDD_FLASH	Supply voltage for external Flash	2.7	-	3.6	V

5.4 Digital LDO

Parameter	Description	Min.	Typ.	Max.	Unit
VDDAON	Always ON LDO digital output voltage	0.5	0.9	1.0	V
Load Current	-	-	-	50	mA

5.5 Crystal and Reference Clock

Parameter	Description	Min.	Typ.	Max.	Unit
Frequency	Crystal and reference frequency	-	26	-	MHz
Tolerance	Crystal and reference frequency tolerance	-10	-	+10	ppm
XI Pin	Input voltage range for reference clock input	-0.3	-	1.05	V

5.6 Current Consumption

Measured with T = 25 °C, VBAT = 3.0 V unless otherwise stated.

Parameter	Condition	Min.	Typ.	Max.	Unit
Active Mode					
RX current	11 Mbps DSSS	-	30	-	mA
	54 Mbps OFDM	-	33	-	mA
	MCS7, HT20	-	33	-	mA
TX current	11 Mbps DSSS @ 17 dBm	-	265	-	mA
	54 Mbps OFDM @ 15 dBm	-	230	-	mA
	MCS7, HT20 @ 14 dBm	-	220	-	mA

Parameter	Condition	Min.	Typ.	Max.	Unit
Standby Mode					
Normal standby	-	-	300	-	µA
Low voltage standby	-	-	75	-	µA
Deep Sleep Mode					
Deep sleep	-	-	10	-	µA
Shutdown Mode					
Shutdown	-	-	0.5	-	µA

5.7 WLAN RF Characteristics - Receiver

Measured with T = 25 °C, VBAT = 3.0 V unless otherwise stated.

Parameter	Condition	Min.	Typ.	Max.	Unit
General					
Frequency range	-	2412	-	2484	MHz
Sensitivity					
Sensitivity - IEEE 802.11b	1 Mbps DSSS	-	-99	-	dBm
	2 Mbps DSSS	-	-96	-	dBm
	5.5 Mbps DSSS	-	-94	-	dBm
	11 Mbps DSSS	-	-90	-	dBm
Sensitivity - IEEE 802.11g (10% PER for 1024 octet PSDU)	6 Mbps OFDM	-	-92	-	dBm
	9 Mbps OFDM	-	-92	-	dBm
	12 Mbps OFDM	-	-91	-	dBm
	18 Mbps OFDM	-	-89	-	dBm
	24 Mbps OFDM	-	-86	-	dBm
	36 Mbps OFDM	-	-82	-	dBm
	48 Mbps OFDM	-	-78	-	dBm
	54 Mbps OFDM	-	-76	-	dBm
Sensitivity - IEEE 802.11n, 20 MHz	MCS0	-	-92	-	dBm

Parameter	Condition		Min.	Typ.	Max.	Unit
(10% PER for 4096 octet PSDU)	MCS1		-	-90	-	dBm
	MCS2		-	-87	-	dBm
	MCS3		-	-84	-	dBm
	MCS4		-	-81	-	dBm
	MCS5		-	-77	-	dBm
	MCS6		-	-75	-	dBm
	MCS7		-	-74	-	dBm
Maximum Receive Level						
Maximum receive level @ 2.4 GHz	1, 2 Mbps (8% PER, 1024 octets)		-	-	10	dBm
	5.5, 11 Mbps (8% PER, 1024 octets)		-	-	10	dBm
	6 ~54 Mbps (10% PER, 1024 octets)		-	-	5	dBm
	MCS0~7 (10% PER, 4096 octets)		-	-	2	dBm
Adjacent Channel Rejection						
Adjacent channel rejection - IEEE 802.11b	1 Mbps DSSS	-74 dBm	-	45	-	dB
	2 Mbps DSSS	-74 dBm	-	45	-	dB
	5.5 Mbps DSSS	-70 dBm	-	40	-	dB
	11 Mbps DSSS	-70 dBm	-	40	-	dB
Adjacent channel rejection - IEEE 802.11g	6 Mbps OFDM	-79 dBm	-	37	-	dB
	54 Mbps OFDM	-62 dBm	-	28	-	dB
Adjacent channel rejection - IEEE 802.11n	MCS0	-79 dBm	-	35	-	dB
	MCS7	-61 dBm	-	22	-	dB

5.8 WLAN RF Characteristics - Transmitter

Measured with T = 25 °C, VBAT = 3.0 V unless otherwise stated.

Parameter	Condition		Min.	Typ.	Max.	Unit
General						
Frequency range	-		2412	-	2484	MHz
TX power						
TX power - IEEE 802.11b (EVM compliant)	1 Mbps DSSS		-	19	-	dBm
	11 Mbps DSSS		-	19	-	dBm
TX power - IEEE 802.11g (EVM compliant)	6 Mbps OFDM		-	20	-	dBm
	54 Mbps OFDM		-	17	-	dBm
TX power - IEEE 802.11n (EVM compliant)	MCS0		-	19	-	dBm
	MCS7		-	16	-	dBm
Harmonic Level						
Harmonic level (at maximum output power)	4.8~5.0 GHz	2nd harmonic	-	-	-45	dBm
	7.2~7.5 GHz	3rd harmonic	-	-	-50	dBm
General Spurs						
General spurs (at maximum output power)	1~18 GHz		-	-	-45	dBm

5.9 Bluetooth LE RF Characteristics - Receiver

Measured with T = 25 °C, VBAT = 3.0 V unless otherwise stated.

Parameter	Condition	Min.	Typ.	Max.	Unit
General					
Frequency range	-	2402	-	2480	MHz
Data rate	Bluetooth LE 1 Mbps, 2 Mbps, 125 kbps and 500 kbps				
Bluetooth LE 1 Mbps					
Sensitivity	30.8% PER	-	-98	-	dBm
Maximum input level	30.8% PER	0	-	-	dBm

Parameter	Condition	Min.	Typ.	Max.	Unit
Out-of-band blocking	30-2000 MHz	-10	-	-	dBm
Out-of-band blocking	2003-2399 MHz	-20	-	-	dBm
Out-of-band blocking	2484-2997 MHz	-10	-	-	dBm
Out-of-band blocking	3000 MHz-12.75 GHz	-10	-	-	dBm

5.10 Bluetooth LE RF Characteristics - Transmitter

Measured with T = 25 °C, VBAT = 3.0 V unless otherwise stated.

Parameter	Condition	Min.	Typ.	Max.	Unit
General					
Frequency range	-	2402	-	2480	MHz
TX Power					
TX power	-	6	8	10	dBm
Bluetooth LE 1 Mbps					
Modulation Characteristics					
Δf1avg	-	-	250	-	kHz
Δf2max	-	-	230	-	kHz
Δf2avg/Δf1avg	-	-	0.9	-	-
Carrier Frequency Offset and Drift					
Max $\lvert f_n \rvert$ $n = 0, 1, 2, 3 \ldots k$	-	-	2.0	-	kHz
Max $\lvert f_0 - f_n \rvert$ $n = 2, 3, 4 \ldots k$	-	-	1.5	-	kHz
$\lvert f_1 - f_0 \rvert$	-	-	0.5	-	kHz
Max $\lvert f_n - f_{n-5} \rvert$ $n = 6, 7, 8 \ldots k$	-	-	1.3	-	kHz/50 μs

5.11 SAR ADC Characteristics

Measured with T = 25 °C, VBAT = 3.0 V unless otherwise stated.

Parameter	Condition	Min.	Typ.	Max.	Unit
Conversion clock	-	-	-	26	MHz
Conversion time	-	-	16	-	Cycle
VREF	-	-	0.9	-	V
Resolution	-	-	10	-	Bits
Input voltage range	-	0	-	ADC_VREF*4	V
Input impedance	-	-	Infinite	-	kΩ
Input capacitance (Cs)	-	-	1	-	pF
DNL	-	-	1	-	Bits
SNDR	-	-	57.5	-	dB
$T_{STARTUP}$	-	-	32	-	Cycle
Current consumption	With buffer	-	200	-	μA

6. Package Information

6.1 QFN40 5 x 5 mm Package

Figure 6-1 QFN40 5 x 5 mm Package Outline

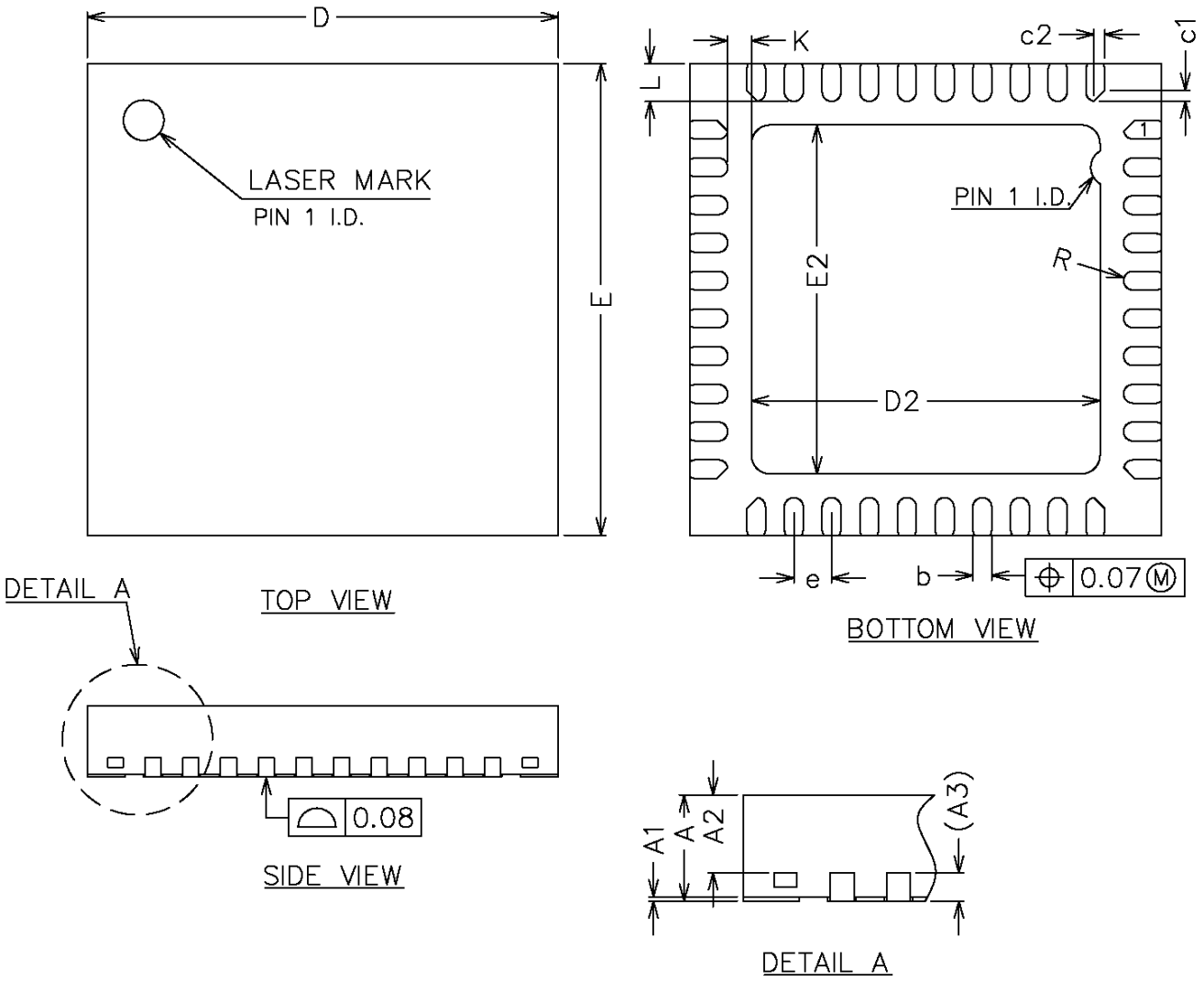


Table 6-1 QFN40 Package Dimensions

Symbol	Dimensions in Millimeters		
	Min.	Nom.	Max.
A	0.70	0.75	0.80
A1	0.00	0.02	0.05
A2	0.50	0.55	0.60
A3	0.20 REF		
b	0.15	0.20	0.25
D	4.90	5.00	5.10
E	4.90	5.00	5.10
D2	3.60	3.70	3.80
E2	3.60	3.70	3.80
e	0.35	0.40	0.45
K	0.20	-	-
L	0.35	0.40	0.45
R	0.075	-	-
c1	-	0.12	-
c2	-	0.12	-

6.2 QFN32 4 x 4 mm Package

Figure 6-2 QFN32 4 x 4 mm Package Outline

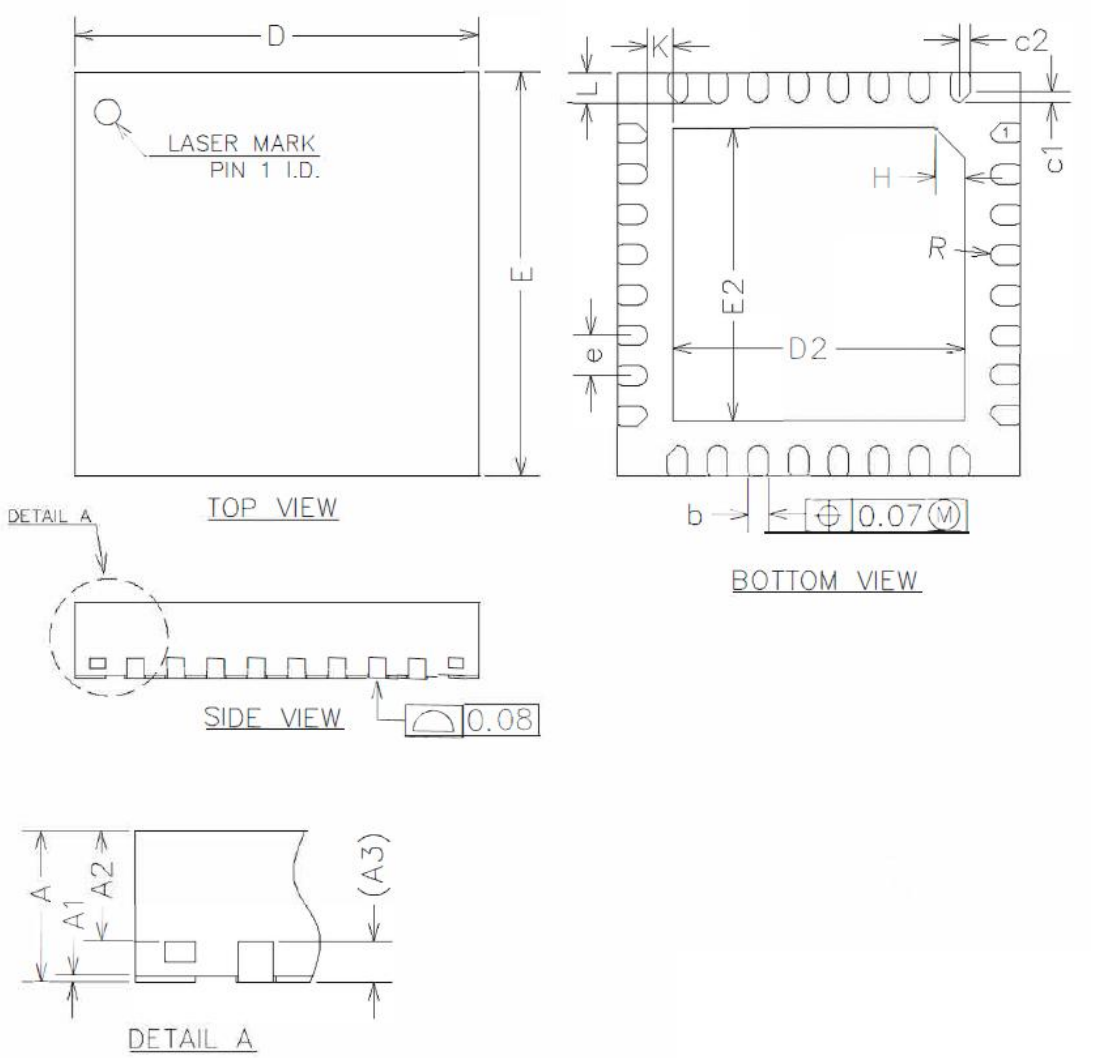


Table 6-2 QFN32 Package Dimensions

Symbol	Dimensions in Millimeters		
	Min.	Nom.	Max.
A	0.70	0.75	0.80
A1	0.00	0.02	0.05
A2	0.50	0.55	0.60
A3	0.20 REF		

Symbol	Dimensions in Millimeters		
	Min.	Nom.	Max.
b	0.15	0.20	0.25
D	3.90	4.00	4.10
E	3.90	4.00	4.10
D2	2.80	2.90	3.00
E2	2.80	2.90	3.00
e	0.30	0.40	0.50
H	0.30 REF		
K	0.25 REF		
L	0.25	0.30	0.35
R	0.09	-	-
c1	-	0.10	-
c2	-	0.10	-

6.3 QFN20 3 x 3 mm Package

Figure 6-3 QFN20 3 x 3 mm Package Outline

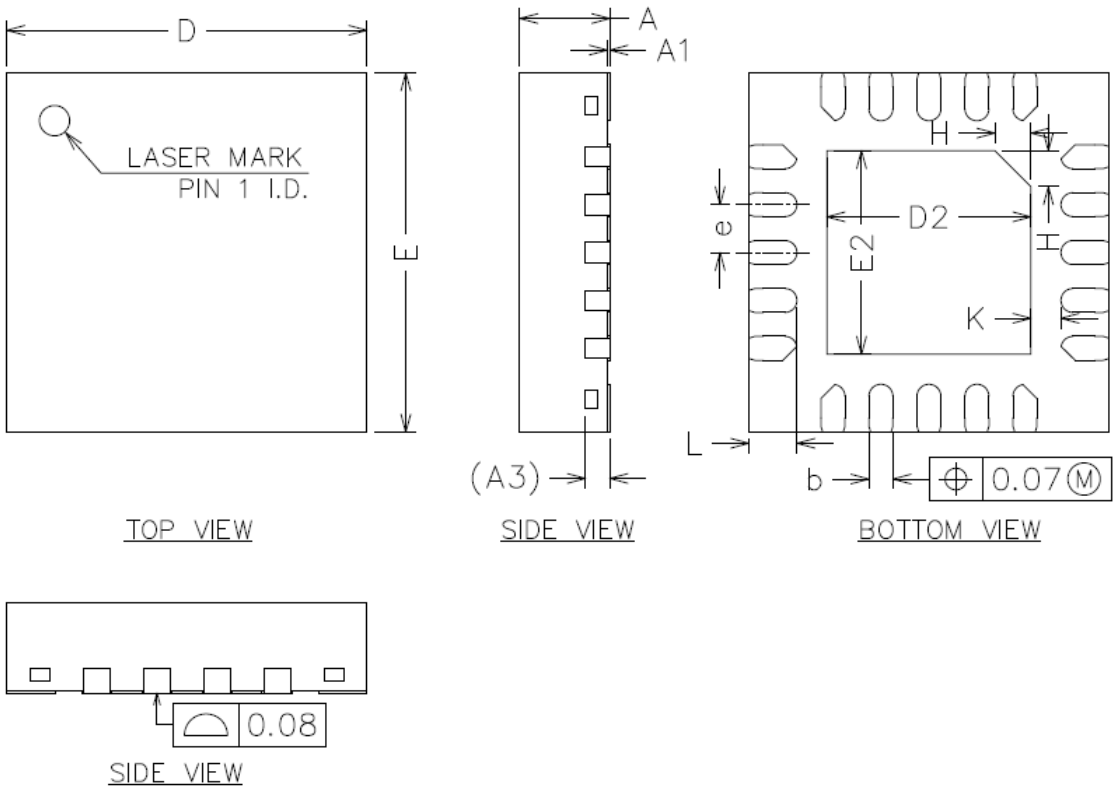


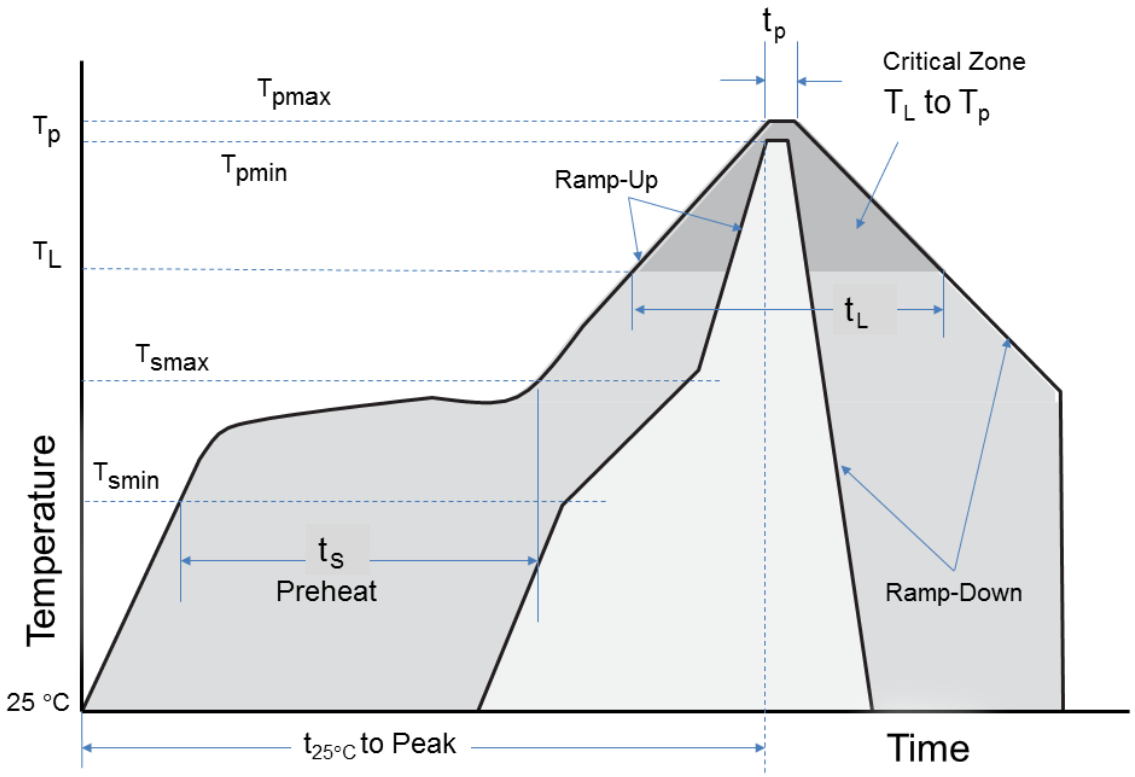
Table 6-3 QFN20 Package Dimensions

Symbol	Dimensions in Millimeters		
	Min.	Nom.	Max.
A	0.70	0.75	0.80
A1	0.00	0.02	0.05
A3	0.20 REF		
b	0.15	0.20	0.25
D	2.95	3.00	3.05
E	2.95	3.00	3.05
D2	1.65	1.70	1.75
E2	1.65	1.70	1.75

Symbol	Dimensions in Millimeters		
	Min.	Nom.	Max.
e	0.30	0.40	0.50
H	0.30 REF		
K	0.15	-	-
L	0.35	0.40	0.45

7. Reflow Soldering Profile

Figure 7-1 Reflow Soldering Profile



Profile Feature		Specification
Average ramp-up rate (T_{smax} to T_p)		3 ℃/s max.
Preheat	Temperature min. (T_{smin})	150 ℃
	Temperature max. (T_{smax})	200 ℃
	Time (t_s)	60 s to 180 s
Time maintained above	Temperature (T_L)	217 ℃
	Time (t_L)	60 s to 150 s
Peak/classification temperature (T_p)		260 ℃
Time within 5 ℃ of actual peak temperature (t_p)		20 s to 40 s
Ramp-down rate		6 ℃/s max.

Profile Feature	Specification
Time 25 ℃ to peak temperature	8 minutes max.

RoHS Compliant

The product does not contain lead, mercury, cadmium, hexavalent chromium, PBB&PBDE content in accordance with directive 2002/95/EC (RoHS).

ESD Sensitivity

Integrated circuits are ESD sensitive and can be damaged by static electricity. Proper ESD techniques should be used when handling these devices.

Moisture Sensitivity Level

The product is qualified to moisture sensitivity level MSL3 in accordance with IPC/JEDEC J-STD-020.

8. Ordering Information

Figure 8-1 Part Number Scheme

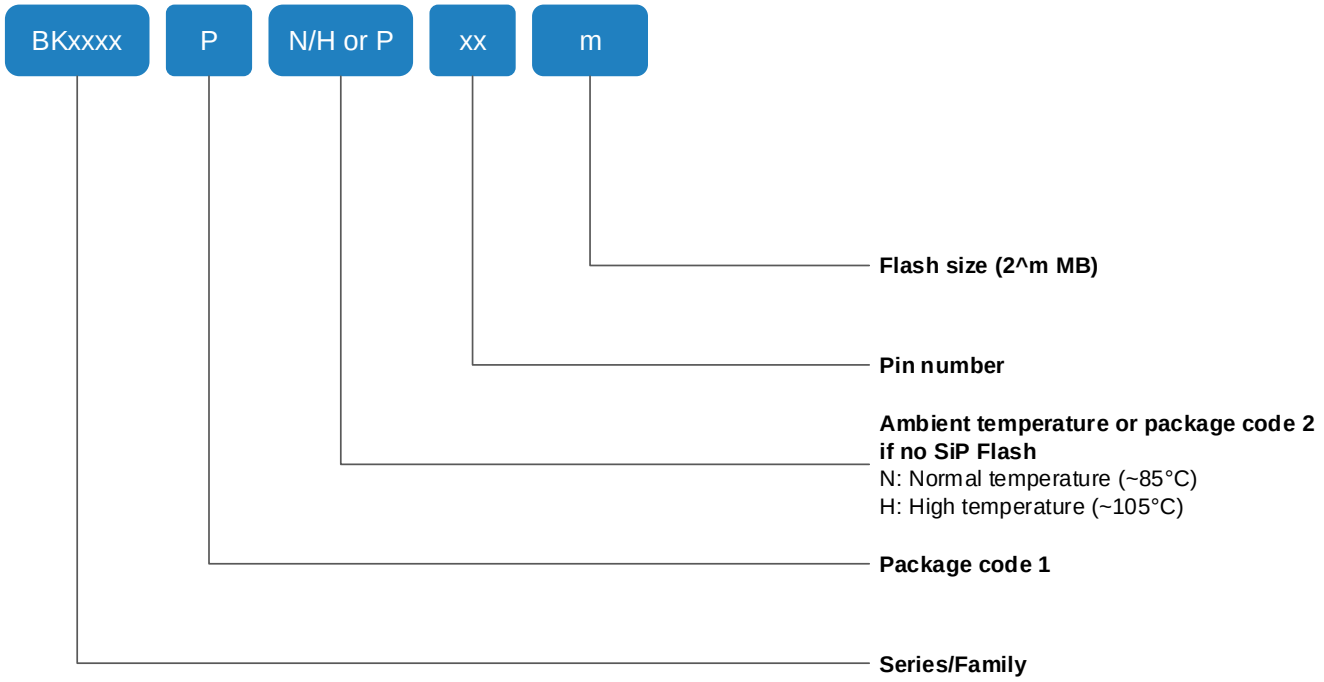


Table 8-1 Ordering Information

Ordering Code	Package	SiP[a] Flash	Ambient Temp	Packing	Minimum Ordering Qty (MOQ)
BK7238QN40	5 mm x 5 mm QFN40	-	-40 to +105 ℃	Tape and Reel	3000
BK7238QH320	4 mm x 4 mm QFN32	1 MB	-40 to +105 ℃	Tape and Reel	3000
BK7238QH200	3 mm x 3 mm QFN20	1 MB	-40 to +105 ℃	Tape and Reel	3000
BK7238QN321	4 mm x 4 mm QFN32	2 MB	-40 to +85 ℃	Tape and Reel	3000
BK7238QH321	4 mm x 4 mm QFN32	2 MB	-40 to +105 ℃	Tape and Reel	3000
BK7238QN201	3 mm x 3 mm QFN20	2 MB	-40 to +85 ℃	Tape and Reel	3000
BK7238QH201	3 mm x 3 mm QFN20	2 MB	-40 to +105 ℃	Tape and Reel	3000

a. A system in a package (SiP) refers to Flash enclosed in the package.

Revision History

Version	Date	Description
0.1	2021/11/2	Initial release. First version of the preliminary specification.
0.2	2022/2/18	Added documentation for QFN32 package and general wording update: • Added and updated features in Section 1 Features • Updated Figure 2-1 and added Table 2-1 in Section 2 Overview • Added Section 3.2 BK7238QN32 Pin Description • Changed the pin name of pin 7 in Section 3.3 BK7238QN20 Pin Description • Added deep sleep mode to Section 4.1 Modes of Operation • Added clock selection for SPI, I2C to Table 4-2 in Section 4.6 Clock • Updated Section 4.7 Reset • Updated GPIO number in Section 4.8 GPIO • Added Section 4.9 SPI, Section 4.11 I2C, Section 4.12 GDMA • Updated PWM channel number in Section 4.13 PWM • Updated the configurable resolution of SRA ADC and Table 4-3 in Section 4.14 General-Purpose SAR ADC • Changed the parameter VDDDIG to VDDAON in Section 5.3 Recommended Operating Conditions • Added parameter deep sleep current to Section 5.6 Current Consumption • Added Section 6.2 QFN32 4 x 4 mm Package • Added QFN32 ordering info to Table 8-1 in Section 8 Ordering Information
0.3	2022/7/7	• Corrected RAM size and removed Cache in Section 1 Features • Removed Cache from Figure 2-1 in Section 2 Overview • Added documentation for QFN40 package • Updated Operating temperature • Corrected IO mapping for ADC channels in Section 3 Pin Description • Added measurement conditions for RF characteristics and SAR ADC characteristics in Section 5 Electrical Characteristics • Added Section 7 Reflow Soldering Profile
1.0	2022/10/24	• Updated Wi-Fi TX power and RX sensitivity in Section 1 Features • Added 2 MB Flash option for QFN32 and QFN20 packages • Replaced low-power timer with real-time counter (RTC) • Added Section 5.2 ESD Ratings

Version	Date	Description
		• Added active mode TX current and deep sleep current to Section 5.6 Current Consumption • Updated and added RF data in Section 5.7 to Section 5.10 • Updated SAR ADC characteristics table in Section 5.11 SAR ADC Characteristics
1.1	2023/2/20	• Updated Table 2-1 for BK7238QN20 in Section 2 Overview • Updated pin assignments of QFN20 package (BK7238QN20) • Updated storage temperature range in Section 5.1 Absolute Maximum Ratings
1.2	2023/3/6	Added Section 4.5 Power-Up Sequence
1.3	2023/3/31	Updated Section 8 Ordering Information
1.4	2023/4/28	Updated ESD ratings in Section 5.2 ESD Ratings

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