Matt Hartnett

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SKILLS

- **Digital Design:** SystemVerilog RTL, Vivado, DSP, High Speed Interfaces, Tcl, VHDL, Quartus, Libero
- **Digital Verification:** SystemVerilog TB, Cocotb, Verilator, xsim, Modelsim
- **Circuit Design and Analysis:** LTSpice, Advanced Design System, Soldering, Solidworks Electrical, DipTrace, Eagle
- **Software Development:** Python, C++, C, Java
- **Linux Development:** Ubuntu, Fedora, Buildroot, Yocto, PetaLinux
- **Embedded Programming:** Embedded C, Codasip, Arduino, Raspberry Pi
- **Web Development:** HTML, CSS, Javascript, PHP, SQL
- **Software Systems:** Git, CI/CD, Matlab, Simulink Real-time, OpenCV, SVN
- **Debugging:** Simulation with Testbenches, Hardware with Logic Analyzers, Scopes, and other tools
- **Project Management Tools:** Agile PLM, Confluence, DOORS NG, OpenText MBPM

EXPERIENCE

Embedded Systems Engineer - FIRST RF 10/2024–Present
Boulder, CO

- Architected and implemented the full FPGA/HDL stack for a production RADAR system, owning design from module-level RTL to system integration. Included high speed interfaces, on-chip processing, and device to device synchronization.
- Delivered a new DSP pipeline that increased usable bandwidth 4×, improved SNR by ~20 dB, reduced logic utilization, and lowered end-to-end latency; modeled algorithms in Python/NumPy and verified with exhaustive testbenches.
- Engineered a cycle-accurate, latency-constrained data path to meet strict RADAR timeline requirements; performed both simulation-based and on-hardware validation in partnership with embedded/software teams.
- Modernized the internal HDL build system, enabling Verilator + cocotb flows; authored FIRST RF's first cocotb testbenches and led full team adoption.

Electrical Engineer II - Laboratory for Atmospheric and Space Physics 06/2022–10/2024
Boulder, CO

- Operated as the lead of electronic ground support equipment (EGSE) for NASA's Libera mission, including the design and implementation of several test systems; designs included integration of COTS equipment, custom PCBs, and FPGA logic.
- Developed test racks from scratch: specifying, procuring, and assembling IT hardware, writing hardware control firmware, designing interface harnesses, and authoring control software to enable long-duration, mission-critical testing and integration.
- Served as the cognizant EGSE engineer, owning multiple projects from concept through qualification; including rigorous design reviews and compliance processes, and multi-team coordination to ensure delivery-readiness and long-term mission support.

Electrical Engineering Intern - Laboratory for Atmospheric and Space Physics 01/2021–06/2022
Boulder, CO

- Wrote low-level, hardware interface flight software for the SPRITE cubesat mission.
- Developed an FPGA solution to test the scientific instrument on the ground.
- Wrote an image compression algorithm that reduced the scientific data to 1/10th.

Teaching Assistant - Circuits 1 for Engineers 08/2021–12/2021
Boulder, CO

- Provided support to students in lab and in office hours.
- Graded lab reports and created answer keys.
- Developed midterm questions and helped course organization.

IT Technician - Leeds School of Business 01/2020–01/2021
Boulder, CO

- Installed and configured hardware and software for workstations and classrooms.
- Communicated technical information through emails and phone calls.

Robotics Research Assistant - Advanced Robotics Perception Group 09/2019–05/2020
Boulder, CO

- Worked with a large team building a complex navigation robot.
- Used OpenCV for object detection and identification, specifically heat signatures of human dummies, phones, and vents with >80% accuracy.

EDUCATION

MSEE, Embedded Systems Engineering - University of Colorado, Boulder 08/2023–Present
Boulder, CO

BS, Electrical and Computer Engineering - University of Colorado, Boulder 08/2019–05/2022
Boulder, CO

PROJECTS

Skyler Phased Array RADAR

- Designed the end-to-end DSP chain and datapath (filtering, decimation/interpolation, mixing, 1 Gb/s Ethernet framing), then implemented cycle-accurate RTL with thorough TB coverage.
- Built a layered verification strategy (SystemVerilog TB + cocotb with Verilator) to catch interface, timing, and algorithmic defects early; mirrored tests on hardware for parity and end product verification.
- Drove cross-functional integration and bring-up with embedded and application software, closing timing on high utilization designs while meeting RADAR timeline constraints.

Libera SSIM

- Led the design of an advanced, high reliability test fixture used to validate the performance of the Libera instrument.
- Created a test rack to simulate the JPSS-3 spacecraft with 100% of interfaces accurately recreated to maximize “test as you fly” ideology.
- Integrated a precisely synchronized FPGA with <10 ns timing error.

Libera EL Lifetest

- Prepared and implemented the test bed for a 5-year pre-flight motor verification test.
- Designed a custom PCB and multiple harnesses to integrate dozens of components into a cohesive system.

Senior Design Capstone (FRANKLIN)

- Team lead for a phase-coherent remote sensing system.
- Developed FPGA-based data collection and storage.

GSE Detector Readout

- Used an FPGA to read detector data at full speed and stream over 100 Mb/s Ethernet to a PC for live readout.
- Implemented a MicroBlaze processor on a Spartan-7 FPGA to run the TCP stack in C.

3D Drone Mapping Simulation

- Autonomously mapped 3D environments in Webots.
- Planned exploration with a rapidly-exploring random tree to target unmapped areas.

5-Stage RISC-V Processor

- Built a fully functional processor in Codasip using C++, then adapted to synthesizable RTL with I/O management and off-chip RAM access.
- Achieved 100% verification coverage; designed with full ISA support and ECC memory.

REFERENCES

Dominic Doty - Software Development Engineer, Amazon - doty.dominic@gmail.com - (303) 704-8313
Jack Williams, PhD - Senior Electrical Engineer, Blue Canyon Technologies - (303) 735-8727