Matt Hartnett

Contact Information
matthew.e.hartnett@gmail.com
Github: https://github.com/hartnettmatt
LinkedIn: www.linkedin.com/in/hartnettmatt

Skills

Digital Design (SystemVerilog RTL, Vivado, DSP, tcl, VHDL, Quartus, Libero)

Digital Verification (SystemVerilog TB, Cocotb, Verilator, xsim, Modelsim)

Circuit Design and Analysis (LTSpice, Advanced Design System, Soldering, Solidworks Electrical, DipTrace, Eagle)

Software Development (Python, C++, Embedded C, Java)

Linux Development (Ubuntu, Fedora, Buildroot, Yocto, PetaLinux)

Embedded Programming (Embedded C, Codasip, Arduino, Raspberry Pi)

Web Development (HTML, CSS, Javascript, PHP, SQL)

Software Systems (Git, CI/CD, Matlab, Simulink Real-time, OpenCV, SVN)

Debugging and problem solving for all architectures listed above

Project Management Tools (Agile PLM, Confluence, DOORS NG, OpenText MBPM)

Experience

Embedded Systems Engineer / FIRST RF

10/2024 to Present, Boulder

- Architected and implemented the full FPGA/HDL stack for a production radar system, owning design from module-level RTL to system integration (SystemVerilog, Vivado).
- Delivered a new DSP pipeline that increased usable bandwidth 4×, improved SNR by ~20 dB, reduced logic utilization, and lowered end-to-end latency; modeled algorithms in Python/NumPy and verified with exhaustive testbenches.
- Engineered a cycle-accurate, latency-constrained data path to meet strict radar timeline requirements; performed both simulation-based and on-hardware validation in partnership with embedded/software teams.
- Modernized the internal HDL build system, enabling Verilator + cocotb flows; authored FIRST RF's first cocotb testbenches and led full team adoption.

Electrical Engineer II / Laboratory for Atmospheric and Space Physics

06/2022 to 10/2024, CU Boulder

- Designed high reliability test equipment for the Libera scientific mission
- Built systems from the ground up, including hardware, firmware, and software
- Operated with minimal oversight as the cognizant engineer for multiple projects

Electrical Engineering Intern / Laboratory for Atmospheric and Space Physics

01/2021 to 06/2022, CU Boulder

- Wrote low-level, hardware interface flight software for the SPRITE cubesat mission
- Developed an FPGA solution to test our scientific instrument on the ground.
- Wrote an image compression algorithm that reduced the scientific data to 1/10th

Teaching Assistant / Circuits 1 for Engineers

08/2021 to 12/2021, CU Boulder

- Provided support to students in lab and in office hours
- Graded lab reports and created answer keys
- Developed midterm questions and helped course organization

IT Technician / Leeds School of Business

01/2020 to 01/2021, CU Boulder

- Installed and configured hardware and software for workstations and classrooms.
- Communicated technical information through emails and phone calls.

Robotics Research Assistant / Advanced Robotics Perception Group

09/2019 to 05/2020, CU Boulder

- Worked with a large team building a complex navigation robot.
- Used OpenCV for object detection and identification, specifically heat signatures of human dummies, phones, and vents with >80% accuracy

Education

MSEE Embedded Systems Engineering (In Progress) / University of Colorado Boulder

08/2023 - Present, Boulder Colorado

BS Electrical and Computer Engineering / University of Colorado Boulder

08/2019 - 05/2022, Boulder Colorado

Projects

Skyler Phased Array RADAR
- Designed the end-to-end DSP chain and datapath (filtering, decimation/interpolation, mixing, 1 Gb/s ethernet framing), then implemented cycle-accurate RTL with thorough TB coverage.
- Built a layered verification strategy (SystemVerilog TB + cocotb on Verilator) to catch interface, timing, and algorithmic defects early; mirrored tests on hardware for parity.
- Drove cross-functional integration and bring-up with embedded and application software, closing timing on high utilization designs, while meeting radar timeline constraints.

Libera SSIM
- Lead the design of an advanced, high reliability test fixture utilized to validate the performance of the Libera instrument.
- Created a test rack to simulate the JPSS-3 spacecraft with 100% of interfaces accurately recreated to maximize "Test as you fly" ideology
- High reliability system that included a precisely synchronized FPGA with less than 10 nanosecond of timing error

Libera EL Lifetest
- Prepared and implemented the test bed for a 5 year long, pre-flight motor verification test
- Required a custom PCB as well as several custom harnesses in order to integrate in dozens of different components and aspects into a cohesive system

Senior Design Capstone
- Team lead for the FRANKLIN, a phase coherent remote sensing system
- Primarily developed the FPGA-based data collection and storage

GSE Detector Readout
- Utilized an FPGA to read the data from our scientific detector at full speed and then write that data over 100 Mb/s ethernet to a PC for a live readout
- Implemented a Microbaze processor on a Spartan 7 FPGA to run the TCP stack in C

3D Drone Mapping Simulation
- Utilized the Webots simulation software to autonomously map in 3D
- A drone sought out unmapped areas using a rapidly-exploring random tree

5 Stage RISC-V Processor
- A fully functional and validated processor, built in Codasip using C++ and adapted into RTL as a synthesizable core with IO management, access to off-chip RAM, and 100% verification
- Designed from the ground up to include the full ISA as well as ECC memory

Reference

Dominic Doty

Software Development Engineer, Amazon

doty.dominic@gmail.com

(303) 704-8313

Jack Williams, PhD

Senior Electrical Engineer, Blue Canyon Technologies

(303) 735-8727