Matt Hartnett

matthew.e.hartnett@gmail.com · github.com/hartnettmatt · linkedin.com/in/hartnettmatt

Skills

Digital Design: SystemVerilog RTL, Vivado, DSP, High-Speed Interfaces, Tcl, VHDL, Quartus, Libero
Verification: SystemVerilog TB, cocotb, Verilator, xsim, ModelSim
Software: Python, C++, C, Java
Linux: Ubuntu, Fedora, Buildroot, Yocto, PetaLinux
Embedded: Embedded C, Codasip, Arduino, Raspberry Pi
Systems & Tools: Git, CI/CD, MATLAB, Simulink Real-Time, OpenCV, SVN
Debug: Simulation with TBs; on-hardware with logic analyzers, scopes, and related tools
Process: Agile PLM, Confluence, DOORS NG, OpenText MBPM

Experience

Embedded Systems Engineer • **FIRST RF** 10/2024–Present
Boulder, CO

- Architected and implemented the full FPGA/HDL stack for a production RADAR system, owning design from module level RTL to system integration. Included high speed interfaces, on chip processing, and device to device synchronization.
- Delivered a new DSP pipeline that increased usable bandwidth 4×, improved SNR by ~20 dB, reduced logic utilization, and lowered end to end latency; modeled algorithms in Python/NumPy and verified with exhaustive testbenches.
- Engineered a cycle accurate, latency constrained data path to meet strict RADAR timeline requirements; performed both simulation based and on hardware validation in partnership with embedded/software teams.
- Modernized the internal HDL build system, enabling Verilator + cocotb flows; authored FIRST RF's first cocotb testbenches and led full team adoption.

Electrical Engineer II • **Laboratory for Atmospheric and Space Physics** 06/2022–10/2024
Boulder, CO

- Operated as the lead of electronic ground support equipment (EGSE) for NASA's Libera mission, including the design and implementation of several test systems; designs included integration of COTS equipment, custom PCBs, and FPGA logic.
- Developed test racks from scratch: specifying, procuring, and assembling IT hardware, writing hardware control firmware, designing interface harnesses, and authoring control software to enable long duration, mission critical testing and integration.
- Served as the cognizant EGSE engineer, owning multiple projects from concept through qualification; including rigorous design reviews and compliance processes, and multi-team coordination to ensure delivery readiness and long term mission support.

Electrical Engineering Intern • **Laboratory for Atmospheric and Space Physics** 01/2021–06/2022
Boulder, CO

- Wrote low-level, hardware interface flight software for the Command and Data Handling (C&DH) Unit on the SPRITE cubesat mission.
- Developed an FPGA-based solution to test the scientific instrument on the ground with a simple, robust interface to enable rapid verification.
- Wrote an image compression algorithm that reduced the scientific data to 1/10th of the original size, enabling the mission to meet TX requirements.

Education

MSEE, Embedded Systems Engineering • **University of Colorado Boulder** 08/2023–Present
Boulder, CO

BS, Electrical & Computer Engineering • **University of Colorado Boulder** 08/2019–05/2022
Boulder, CO

Projects

Skyler Phased Array RADAR

- Designed the end-to-end DSP chain and datapath (filtering, decimation/interpolation, mixing, 1 Gb/s Ethernet framing), then implemented cycle accurate RTL with thorough TB coverage.
- Built a layered verification strategy (SystemVerilog TB + cocotb with Verilator) to catch interface, timing, and algorithmic defects early; mirrored tests on hardware for parity and end product verification.
- Drove cross-functional integration and bring up with embedded and application software, closing timing on high utilization designs while meeting RADAR timeline constraints.

Libera SSIM

- Led the design of an advanced, high reliability test fixture used to validate the performance of the Libera instrument.
- Created a test rack to simulate the JPSS-3 spacecraft with 100% of interfaces accurately recreated to maximize "test like you fly" ideology.
- Integrated a precisely synchronized FPGA with <10 ns timing error.

Libera EL Lifetest

- Designed, implemented, and qualified the test bed for a 5 year pre-flight motor verification lifespan test.
- Engineered a custom interconnect PCB and multiple harnesses to integrate dozens of components into a cohesive system with minimal harnessing.

5-Stage RISC-V Processor

- Built a fully functional processor in Codasip using C++, then adapted to synthesizable RTL with I/O management and off chip RAM access.
- Achieved 100% verification coverage; designed with full ISA support and ECC memory.