Matt Hartnett

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Skills

Digital Design: SystemVerilog RTL, Vivado, DSP, High-Speed Interfaces, Tcl, VHDL, Quartus, Libero
Verification: SystemVerilog TB, cocotb, Verilator, xsim, ModelSim
Software: Python, C++, C, Java
Linux: Ubuntu, Fedora, Buildroot, Yocto, PetaLinux
Embedded: Embedded C, Codasip, Arduino, Raspberry Pi
Systems & Tools: Git, CI/CD, MATLAB, Simulink Real-Time, OpenCV, SVN
Debug: Simulation with TBs; on-hardware with logic analyzers, scopes, and related tools
Process: Agile PLM, Confluence, DOORS NG, OpenText MBPM

Experience

Embedded Systems Engineer · **FIRST RF** 10/2024–Present
Boulder, CO

- Architected and implemented the FPGA/HDL stack for a production RADAR system, from module-level RTL to system integration; covered high-speed interfaces, on-chip processing, and device synchronization.
- Delivered a DSP pipeline that increased usable bandwidth 4×, improved SNR by ~20 dB, reduced logic utilization, and lowered end-to-end latency; modeled in Python/NumPy and verified with exhaustive testbenches.
- Engineered a cycle-accurate, latency-constrained data path to meet strict RADAR timing; validated via simulation and on-hardware with embedded/software teams.
- Modernized HDL build flows (Verilator + cocotb); authored FIRST RF's first cocotb testbenches and led team adoption.

Electrical Engineer II · **Laboratory for Atmospheric and Space Physics** 06/2022–10/2024
Boulder, CO

- Led electronic ground support equipment (EGSE) for NASA's Libera mission; designed test systems integrating COTS equipment, custom PCBs, and FPGA logic.
- Built test racks end-to-end: specified/procured IT hardware, wrote control firmware, designed interface harnesses, and authored control software for long-duration, mission-critical testing.
- Owned projects from concept through qualification, navigating reviews and compliance, coordinating across teams for delivery readiness and long-term mission support.

Electrical Engineering Intern · **Laboratory for Atmospheric and Space Physics** 01/2021–06/2022
Boulder, CO

- Wrote low-level hardware-interface flight software for the Command & Data Handling (C&DH) unit on the SPRITE CubeSat mission.
- Developed an FPGA-based ground test solution with a simple, robust interface for rapid instrument verification.
- Implemented an image compression algorithm reducing data volume to ~10% of original, enabling TX requirements.

Education

MSEE, Embedded Systems Engineering · **University of Colorado Boulder** 08/2023–Present
Boulder, CO

BS, Electrical & Computer Engineering · **University of Colorado Boulder** 08/2019–05/2022
Boulder, CO

Projects

Skyler Phased Array RADAR

- Designed end-to-end DSP chain and datapath (filtering, decim/interp, mixing, 1 Gb/s Ethernet framing); implemented cycle-accurate RTL with thorough TB coverage.
- Built layered verification (SystemVerilog TB + cocotb/Verilator) to catch interface, timing, and algorithmic defects early; mirrored tests on hardware for parity and product validation.
- Drove cross-functional bring-up with embedded/app software; closed timing on high-utilization designs within RADAR constraints.

Libera SSIM

- Led design of a high-reliability test fixture to validate Libera instrument performance.
- Created a rack that simulated JPSS-3 spacecraft with complete interface replication to support "test as you fly."
- Integrated a precisely synchronized FPGA with <10 ns timing error.

Libera EL Lifetest

- Designed, implemented, and qualified the testbed for a five-year pre-flight motor verification lifespan test.
- Designed a custom interconnect PCB and harnesses to integrate dozens of components into a cohesive system.

5-Stage RISC-V Processor

- Built a functional processor in Codasip (C++), then adapted to synthesizable RTL with I/O management and off-chip RAM access.
- Achieved 100% verification coverage; full ISA support and ECC memory.