

# Illustration of the Hardware Simulator

October 22, 2024

# Syntax and Semantics

There are two main aspects in describing a formal language (e.g. programming language, hardware description language, ...)

- **Syntax:** What is an **allowed** program in the language?
  - ★ This is specified by a grammar
  - ★ The first assignment is about the syntax of HDL<sub>0</sub>
    - ▶ Actually no knowledge of hardware really needed here...
- **Semantics:** What does an allowed program **mean**?
  - ★ One way to define it: by an interpreter program for the language.
  - ★ We will do this in the second assignment for HDL<sub>0</sub>

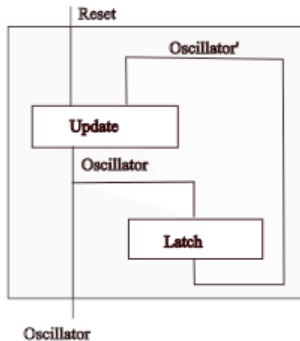
Since us humans like to have an intuitive feel for the language we are working with, we illustrate the interpreter on HDL<sub>0</sub> on the hello-world example in the following.

```

hardware: helloworld
inputs: Reset
outputs: Oscillator
latches: Oscillator
updates:
Oscillator = /Oscillator' /Reset
siminputs:
Reset=0000100

```

State of the Simulator



Clock cycle	1	2	3	4	5	6	7	
Reset	0	0	0	0	1	0	0	Input Signals
Oscillator'								Internal Signals
Oscillator								Output Signals

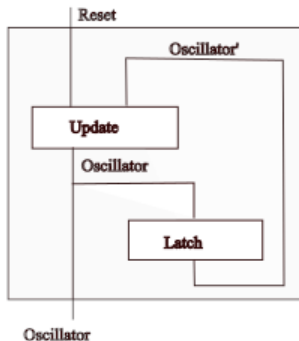
Initially, we are given the value of the input signals. (See simulate)

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Clock cycle	1	2	3	4	5	6	7	
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Oscillator'	0							Internal Signals
Oscillator								Output Signals

On the first time point, all latches output 0

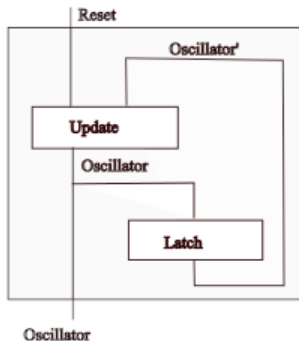
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State of the Simulator

Clock cycle	1	2	3	4	5	6	7	
Reset	0	0	0	0	1	0	0	Input Signals
Oscillator'	0							Internal Signals
Oscillator	1							Output Signals



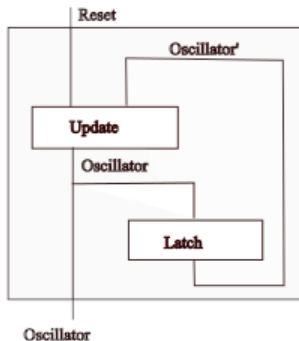
The value of all other signals is computed according to update

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State of the Simulator



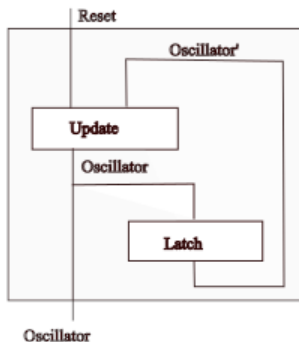
Clock cycle	1	2	3	4	5	6	7	
Reset	0	0	0	0	1	0	0	Input Signals
Oscillator'	0							Internal Signals
Oscillator	1							Output Signals

Proceed to the next clock cycle.

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State of the Simulator

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Clock cycle	1	2	3	4	5	6	7	
Reset	0	0	0	0	1	0	0	Input Signals
Oscillator'	0	1						Internal Signals
Oscillator	1							Output Signals

latches' outputs are set to the value of their inputs from last cycle.

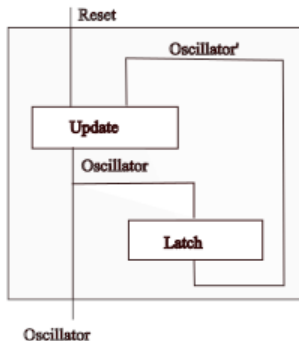
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Oscillator'	0	1						Internal Signals
Oscillator	1	0						Output Signals



All the other signals computed according to update again

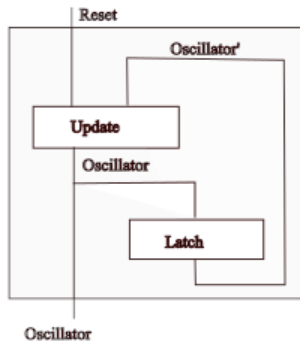


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Oscillator	1	0						Output Signals

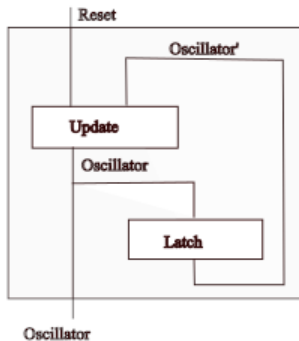
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Oscillator	1	0	1					Output Signals

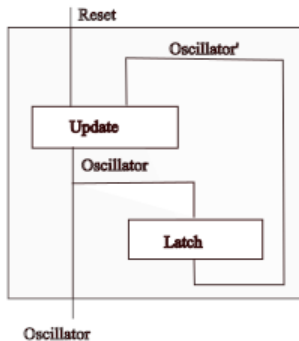
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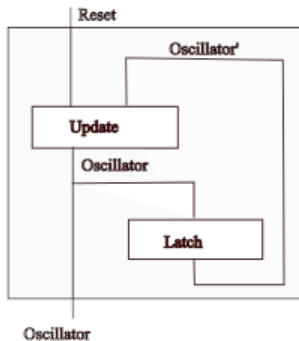
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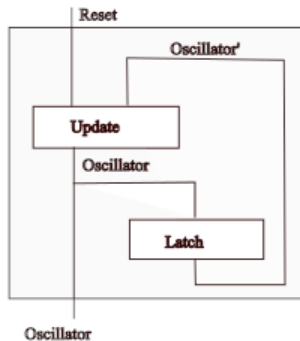
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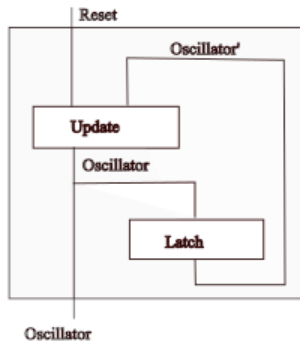
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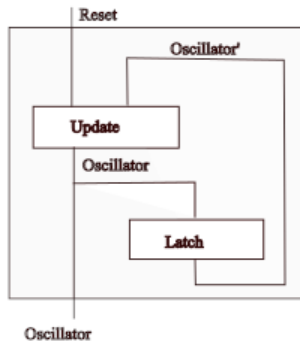
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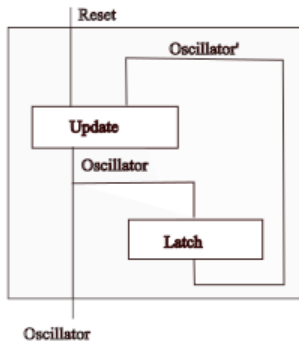
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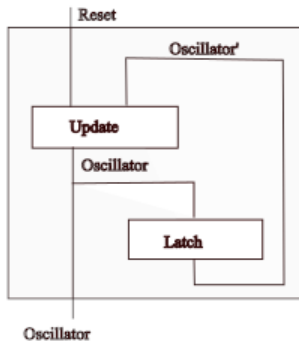
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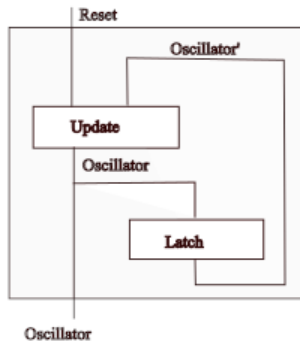
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