Goal

In this lab, you are going to modify the CPU caches in the RISC-V CPU simulator. Lab 1 is composed of two parts. Each part is separate, and you should prepare and submit the source codes respectively.

In task 1, you are asked to modify the three-level CPU cache to be a three-level exclusive Cache with different write policies.

In task 2, you are going to enhance the default LRU cache replacement policy.

You also need to verify the correctness of your implementation and upload a comprehensive and readable summary report in PDF format to ShanghaiTech Pan.

Lab 1 will take **6 points** overall for CS211 in Fall 2022.

The due date for Lab 1

23:59:59, 18th October, 2022. Any submission past the deadline shall not receive any points for this lab.

Deliverable

1. A report in English of your design, implementation, test, etc. In a nutshell, it shall include everything that makes a self-contained practice. (**1 point**)
2. Source code for task 1 with git commit history: the compressed file which contains source code with comments, related test programs, etc. (**2.5 points**)
3. Source code for task 2 with git commit history: the compressed file which contains source code with comments, related test programs, etc. (**2.5 points**)

All of them shall be submitted on ShanghaiTech Cloud Driver (Campus Network Only or via VPN). The submission link is as follows.

Submission Link: http://pan.shanghaitech.edu.cn/cloudservice/outerLink/decode?c3Vnb24xNjY0MjA0MjEzOTE5c3Vnb24=

The task of Lab 1

Task 1

The cache inclusion policy plays an important role in the cache hierarchy. Exclusive policy increases the effective amount of caching and has been adopted in many commercial products.

In this task, you are asked to modify the three-level CPU cache to be a three-level **exclusive** cache hierarchy with **two** different write policies (i.e., write-allocate + write-back, and write-allocate + write-through).

You shall use test cases to quantitatively justify the correctness and efficacy of your implementations.

What you need to do is:

1. Modify the three-level CPU cache to be a three-level **exclusive** cache hierarchy with **write-allocate + write-back** policies.
2. Modify the three-level CPU cache to be a three-level **exclusive** cache hierarchy with **write-allocate + write-through** policies.
3. Design your test methods and cases, and use your test cases to quantitatively justify the correctness and efficacy of your implementations.
4. Depict your exclusive caching algorithm and explain how to deal with different write policies using exclusive cache hierarchy in your report.
5. Prepare a comprehensive and readable report in PDF form.

Task 2

Replacement policy is another significant design decision of the CPU cache. Traditional LRU policy may work not well in some cases. Many researchers have devoted themselves to improving cache replacement.

In this task, you are going to enhance the default LRU cache replacement policy of the simulator.

What you need to do is:

1. Read the paper titled "Sampling Dead Block Prediction for Last-Level Caches". (You can access from the link: https://ieeexplore.ieee.org/document/5695535 or Resources in Piazza.)
2. Figure out how the sampling dead block prediction (SDBP) proposed in the paper works on sampling program counters (PCs) to determine when a cache block is likely to be dead.
3. Implement this SDBP algorithm in the simulator and use it to enhance the default LRU cache replacement policy of the simulator for the last-level caches.
4. Use programs (`test/ackermann.c`, `test/matrixmulti.c`, `test/quicksort.c`) to quantitatively justify that your implementation is effective and efficient, and also you can write test your own programs to test your implementation.
5. Quantitatively compare your policy with the original LRU already included in the simulator by running different test programs.
6. In your report, you must include experimental results (such as miss rate and hit rate) of evaluating your replacement policy against the original LRU, and analyze results and observations systematically.
7. Prepare a comprehensive and readable report in PDF form.

Note: You shall use the original default cache inclusion policy rather than the one you implement in task 1.

Ref:

Should you have any further questions or problems, please contact TAs (Jiang Qisheng and Hu Yanpeng).