

# **Introduction to CMOS VLSI Design**

## **Lecture 3: CMOS Transistor Theory**

### **Outline**

- ☐ Introduction
- ☐ MOS Capacitor
- ☐ nMOS I-V Characteristics
- ☐ pMOS I-V Characteristics
- ☐ Gate and Diffusion Capacitance
- ☐ Pass Transistors
- ☐ RC Delay Models

# Introduction

- ❑ So far, we have treated transistors as ideal switches
- ❑ An ON transistor passes a finite amount of current
  - Depends on terminal voltages
  - Derive current-voltage (I-V) relationships
- ❑ Transistor gate, source, drain all have capacitance
  - $I = C (\Delta V / \Delta t) \rightarrow \Delta t = (C / I) \Delta V$
  - Capacitance and current determine speed
- ❑ Also explore what a “degraded level” really means



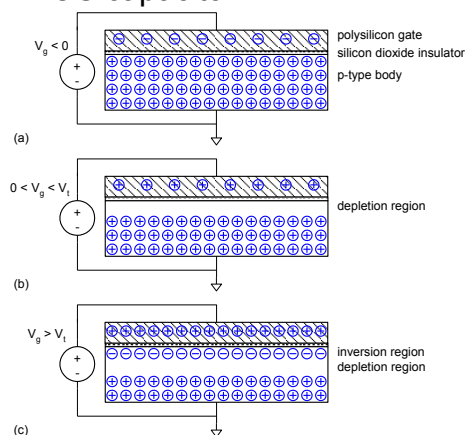
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# MOS Capacitor

- ❑ Gate and body form MOS capacitor
- ❑ Operating modes
  - Accumulation
  - Depletion
  - Inversion



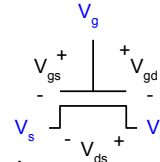
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# Terminal Voltages

- ❑ Mode of operation depends on  $V_g$ ,  $V_d$ ,  $V_s$ 
  - $V_{gs} = V_g - V_s$
  - $V_{gd} = V_g - V_d$
  - $V_{ds} = V_d - V_s = V_{gs} - V_{gd}$
- ❑ Source and drain are symmetric diffusion terminals
  - By convention, source is terminal at lower voltage
  - Hence  $V_{ds} \geq 0$
- ❑ nMOS body is grounded. First assume source is 0 too.
- ❑ Three regions of operation
  - *Cutoff*
  - *Linear*
  - *Saturation*



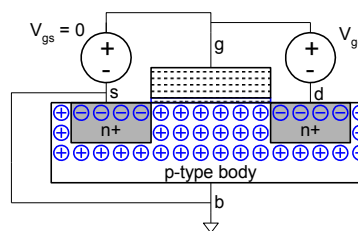
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# nMOS Cutoff

- ❑ No channel
- ❑  $I_{ds} = 0$



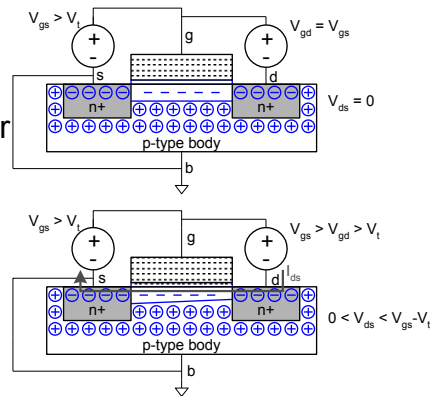
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## nMOS Linear

- ☐ Channel forms
- ☐ Current flows from d to s
  - $e^-$  from s to d
- ☐  $I_{ds}$  increases with  $V_{ds}$
- ☐ Similar to linear resistor



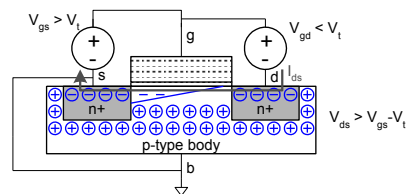
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## nMOS Saturation

- ☐ Channel pinches off
- ☐  $I_{ds}$  independent of  $V_{ds}$
- ☐ We say current saturates
- ☐ Similar to current source



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# I-V Characteristics

- ❑ In Linear region,  $I_{ds}$  depends on
  - How much charge is in the channel?
  - How fast is the charge moving?

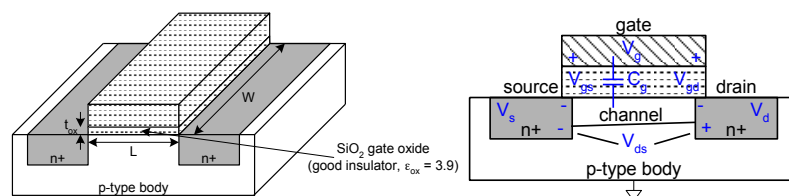
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# Channel Charge

- ❑ MOS structure looks like parallel plate capacitor while operating in inversion
  - Gate – oxide – channel
- ❑  $Q_{\text{channel}} =$



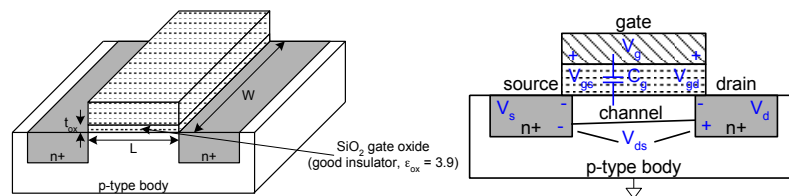
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# Channel Charge

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- ❑  $Q_{\text{channel}} = CV$
- ❑  $C =$



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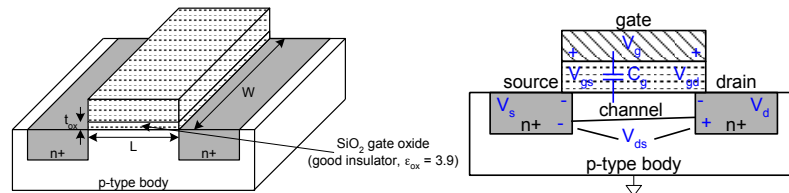
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# Channel Charge

- ❑ MOS structure looks like parallel plate capacitor while operating in inversion
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- ❑  $Q_{\text{channel}} = CV$
- ❑  $C = C_g = \epsilon_{\text{ox}} WL / t_{\text{ox}} = C_{\text{ox}} WL$
- ❑  $V =$

$$C_{\text{ox}} = \epsilon_{\text{ox}} / t_{\text{ox}}$$



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## Channel Charge

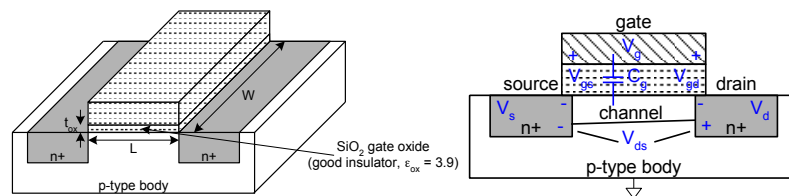
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  - Gate – oxide – channel

- ❑  $Q_{\text{channel}} = CV$

- ❑  $C = C_g = \epsilon_{\text{ox}} WL / t_{\text{ox}} = C_{\text{ox}} WL$

$$C_{\text{ox}} = \epsilon_{\text{ox}} / t_{\text{ox}}$$

- ❑  $V = V_{\text{gc}} - V_t = (V_{\text{gs}} - V_{\text{ds}}/2) - V_t$



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## Carrier velocity

- ❑ Charge is carried by e-
- ❑ Carrier velocity  $v$  proportional to lateral E-field between source and drain
- ❑  $v =$

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## Carrier velocity

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- ❑  $v = \mu E$                        $\mu$  called mobility
- ❑  $E =$

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- ❑  $E = V_{ds}/L$
- ❑ Time for carrier to cross channel:
  - $t =$



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- ❑  $E = V_{ds}/L$
- ❑ Time for carrier to cross channel:
  - $t = L / v$

## nMOS Linear I-V

- ❑ Now we know
  - How much charge  $Q_{\text{channel}}$  is in the channel
  - How much time  $t$  each carrier takes to cross

$$I_{ds} =$$

## nMOS Linear I-V

□ Now we know

- How much charge  $Q_{\text{channel}}$  is in the channel
- How much time  $t$  each carrier takes to cross

$$I_{ds} = \frac{Q_{\text{channel}}}{t}$$

$$=$$

## nMOS Linear I-V

□ Now we know

- How much charge  $Q_{\text{channel}}$  is in the channel
- How much time  $t$  each carrier takes to cross

$$I_{ds} = \frac{Q_{\text{channel}}}{t}$$

$$= \mu C_{\text{ox}} \frac{W}{L} \left( V_{gs} - V_t - \frac{V_{ds}}{2} \right) V_{ds}$$

$$= \beta \left( V_{gs} - V_t - \frac{V_{ds}}{2} \right) V_{ds} \qquad \beta = \mu C_{\text{ox}} \frac{W}{L}$$

## nMOS Saturation I-V

- ❑ If  $V_{gd} < V_t$ , channel pinches off near drain
  - When  $V_{ds} > V_{dsat} = V_{gs} - V_t$
- ❑ Now drain voltage no longer increases current

$$I_{ds} =$$

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$$I_{ds} = \beta \left( V_{gs} - V_t - \frac{V_{dsat}}{2} \right) V_{dsat}$$

$$= \frac{\beta}{2} (V_{gs} - V_t)^2$$

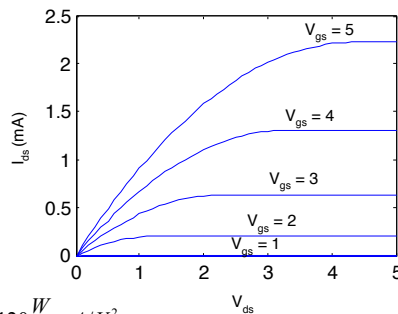
## nMOS I-V Summary

- ❑ Shockley 1<sup>st</sup> order transistor models

$$I_{ds} = \begin{cases} 0 & V_{gs} < V_t & \text{cutoff} \\ \beta \left( V_{gs} - V_t - \frac{V_{ds}}{2} \right) V_{ds} & V_{ds} < V_{dsat} & \text{linear} \\ \frac{\beta}{2} (V_{gs} - V_t)^2 & V_{ds} > V_{dsat} & \text{saturation} \end{cases}$$

## Example

- ❑ We will be using a 0.6  $\mu\text{m}$  process for your project
  - From AMI Semiconductor
  - $t_{\text{ox}} = 100 \text{ \AA}$
  - $\mu = 350 \text{ cm}^2/\text{V}\cdot\text{s}$
  - $V_t = 0.7 \text{ V}$
- ❑ Plot  $I_{\text{ds}}$  vs.  $V_{\text{ds}}$ 
  - $V_{\text{gs}} = 0, 1, 2, 3, 4, 5$
  - Use  $W/L = 4/2 \lambda$



$$\beta = \mu C_{\text{ox}} \frac{W}{L} = (350) \left( \frac{3.9 \cdot 8.85 \cdot 10^{-14}}{100 \cdot 10^{-8}} \right) \left( \frac{W}{L} \right) = 120 \frac{W}{L} \mu\text{A}/\text{V}^2$$

## pMOS I-V

- ❑ All dopings and voltages are inverted for pMOS
- ❑ Mobility  $\mu_p$  is determined by holes
  - Typically 2-3x lower than that of electrons  $\mu_n$
  - $120 \text{ cm}^2/\text{V}\cdot\text{s}$  in AMI 0.6  $\mu\text{m}$  process
- ❑ Thus pMOS must be wider to provide same current
  - In this class, assume  $\mu_n / \mu_p = 2$
  - \*\*\* plot I-V here

# Capacitance

- ❑ Any two conductors separated by an insulator have capacitance
- ❑ Gate to channel capacitor is very important
  - Creates channel charge necessary for operation
- ❑ Source and drain have capacitance to body
  - Across reverse-biased diodes
  - Called diffusion capacitance because it is associated with source/drain diffusion

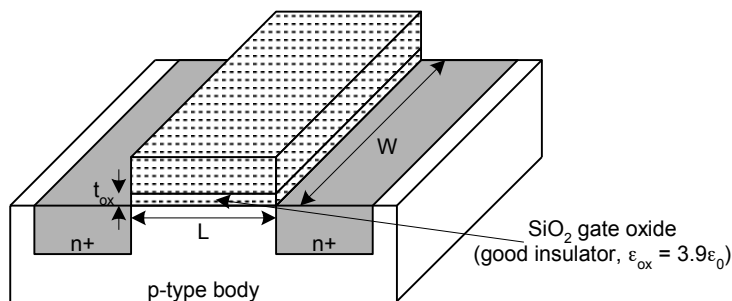
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# Gate Capacitance

- ❑ Approximate channel as connected to source
- ❑  $C_{gs} = \epsilon_{ox} WL / t_{ox} = C_{ox} WL = C_{permicron} W$
- ❑  $C_{permicron}$  is typically about 2 fF/ $\mu\text{m}$



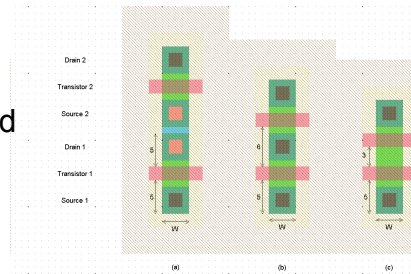
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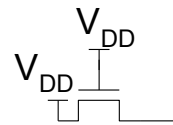
## Diffusion Capacitance

- ❑  $C_{sb}$ ,  $C_{db}$
- ❑ Undesirable, called *parasitic* capacitance
- ❑ Capacitance depends on area and perimeter
  - Use small diffusion nodes
  - Comparable to  $C_g$  for contacted diff
  - $\frac{1}{2} C_g$  for uncontacted
  - Varies with process



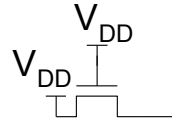
## Pass Transistors

- ❑ We have assumed source is grounded
- ❑ What if source  $> 0$ ?
  - e.g. pass transistor passing  $V_{DD}$



## Pass Transistors

- ❑ We have assumed source is grounded
- ❑ What if source  $> 0$ ?
  - e.g. pass transistor passing  $V_{DD}$
- ❑  $V_g = V_{DD}$ 
  - If  $V_s > V_{DD} - V_t$ ,  $V_{gs} < V_t$
  - Hence transistor would turn itself off
- ❑ nMOS pass transistors pull no higher than  $V_{DD} - V_{tn}$ 
  - Called a degraded “1”
  - Approach degraded value slowly (low  $I_{ds}$ )
- ❑ pMOS pass transistors pull no lower than  $V_{tp}$

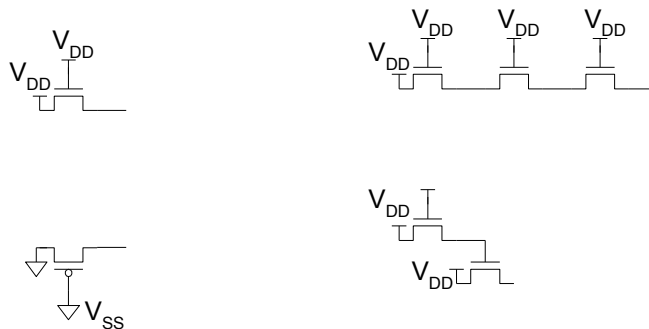


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## Pass Transistor Ckts



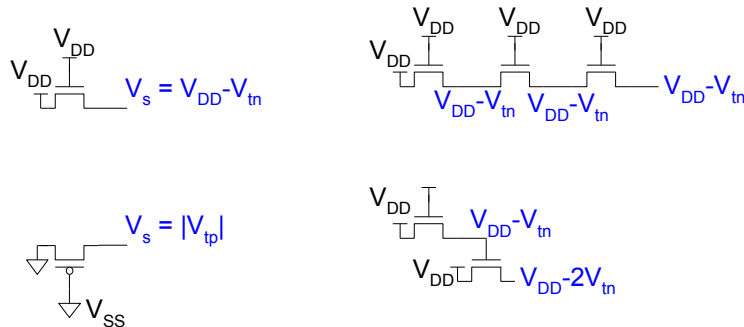
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## Pass Transistor Ckts



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## Effective Resistance

- ❑ Shockley models have limited value
  - Not accurate enough for modern transistors
  - Too complicated for much hand analysis
- ❑ Simplification: treat transistor as resistor
  - Replace  $I_{ds}(V_{ds}, V_{gs})$  with effective resistance  $R$ 
    - $I_{ds} = V_{ds}/R$
  - $R$  averaged across switching of digital gate
- ❑ Too inaccurate to predict current at any given time
  - But good enough to predict RC delay

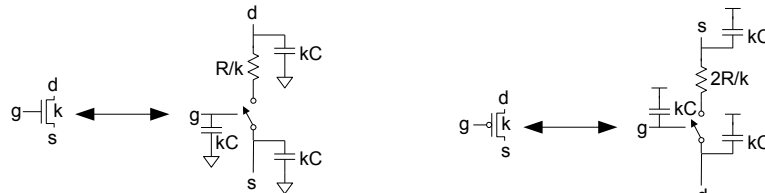
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## RC Delay Model

- ❑ Use equivalent circuits for MOS transistors
  - Ideal switch + capacitance and ON resistance
  - Unit nMOS has resistance  $R$ , capacitance  $C$
  - Unit pMOS has resistance  $2R$ , capacitance  $C$
- ❑ Capacitance proportional to width
- ❑ Resistance inversely proportional to width



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## RC Values

- ❑ Capacitance
  - $C = C_g = C_s = C_d = 2 \text{ fF}/\mu\text{m}$  of gate width
  - Values similar across many processes
- ❑ Resistance
  - $R \approx 6 \text{ K}\Omega \cdot \mu\text{m}$  in  $0.6\mu\text{m}$  process
  - Improves with shorter channel lengths
- ❑ Unit transistors
  - May refer to minimum contacted device ( $4/2 \lambda$ )
  - Or maybe  $1 \mu\text{m}$  wide device
  - Doesn't matter as long as you are consistent

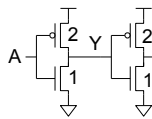
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# Inverter Delay Estimate

- Estimate the delay of a fanout-of-1 inverter



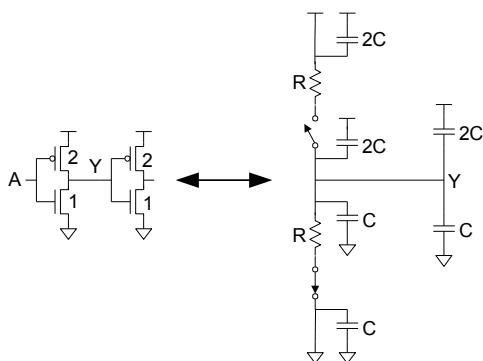
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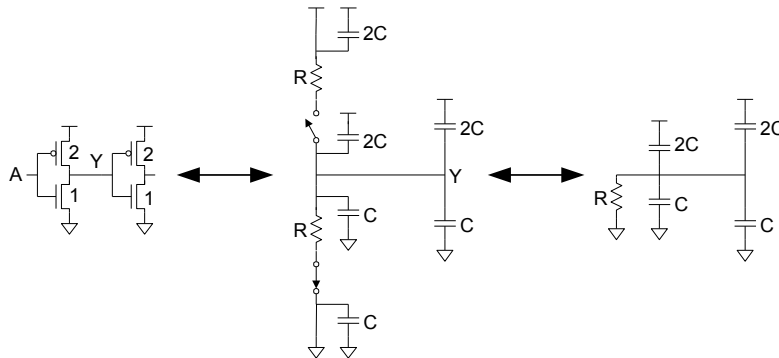
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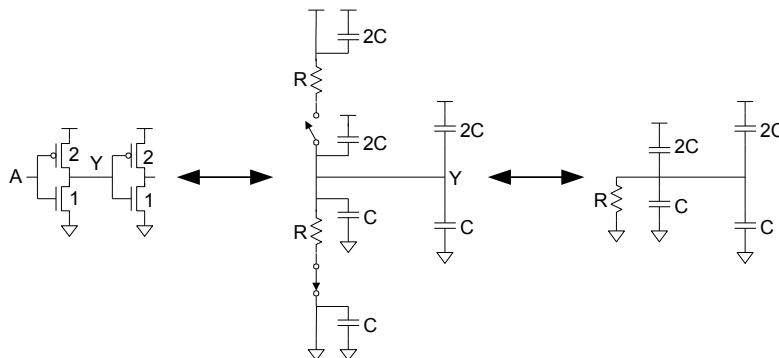
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# Inverter Delay Estimate

- Estimate the delay of a fanout-of-1 inverter



$$d = 6RC$$

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