Introduction to CMOS VLSI Design

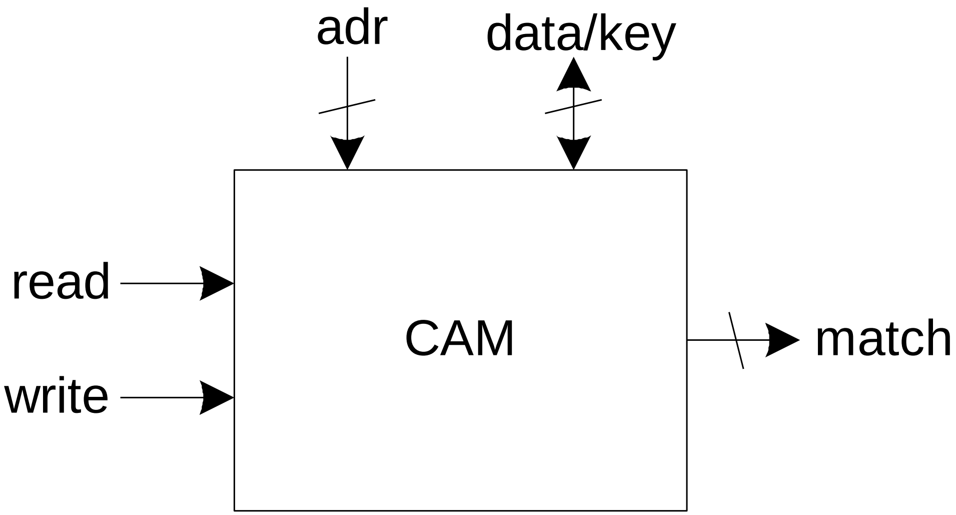
Lecture 14: CAMs, ROMs, and PLAs

Outline

- ❑ Content-Addressable Memories
- ❑ Read-Only Memories
- ❑ Programmable Logic Arrays

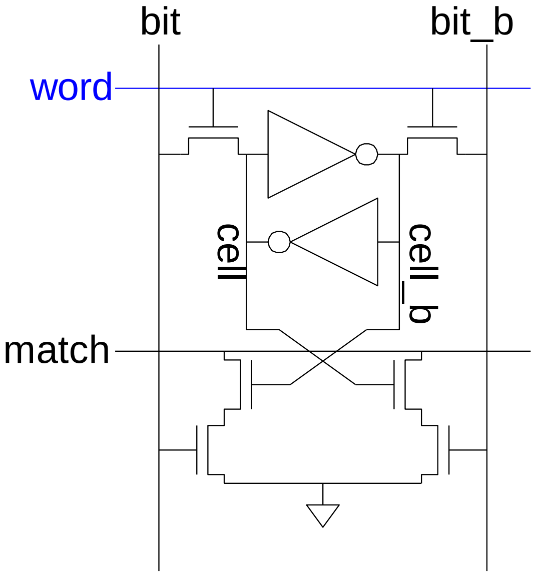
CAMs

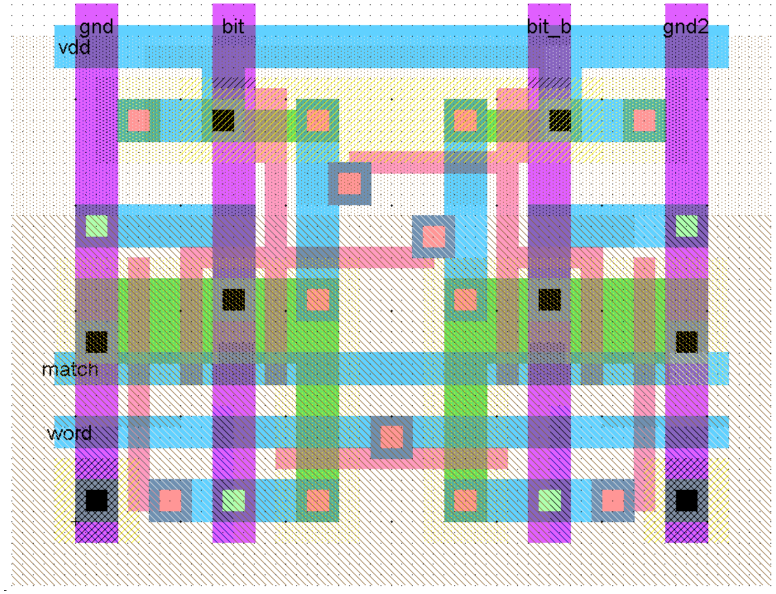
- ❑ Extension of ordinary memory (e.g. SRAM)
  - – Read and write memory as usual
  - – Also *match* to see which words contain a *key*



10T CAM Cell

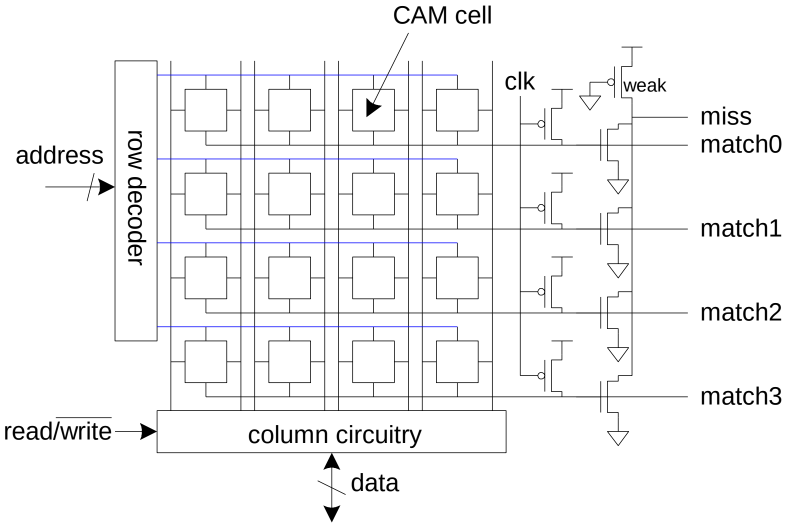
- Add four match transistors to 6T SRAM
  - 56 x 43 λ unit cell





CAM Cell Operation

- ❑ Read and write like ordinary SRAM
- ❑ For matching:
  - – Leave wordline low
  - – Precharge matchlines
  - – Place key on bitlines
  - – Matchlines evaluate
- ❑ Miss line
  - – Pseudo-nMOS NOR of match lines
  - – Goes high if no words match



Read-Only Memories

- ❑ Read-Only Memories are nonvolatile
  - – Retain their contents when power is removed
- ❑ Mask-programmed ROMs use one transistor per bit
  - – Presence or absence determines 1 or 0

ROM Example

- ❑ 4-word x 6-bit ROM
  - – Represented with dot diagram
  - – Dots indicate 1’ s in ROM

```
Word 0: 010101
Word 1: 011001
Word 2: 100101
Word 3: 101010
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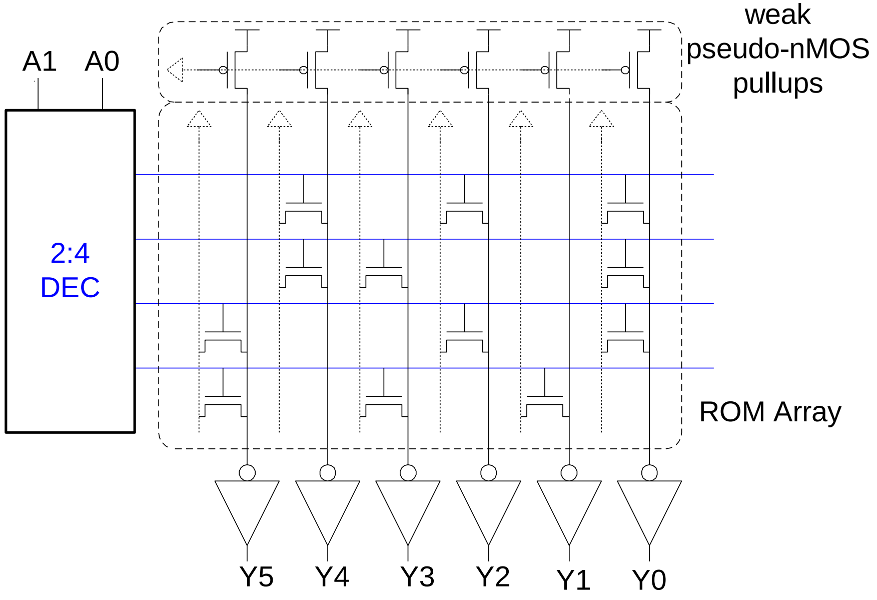
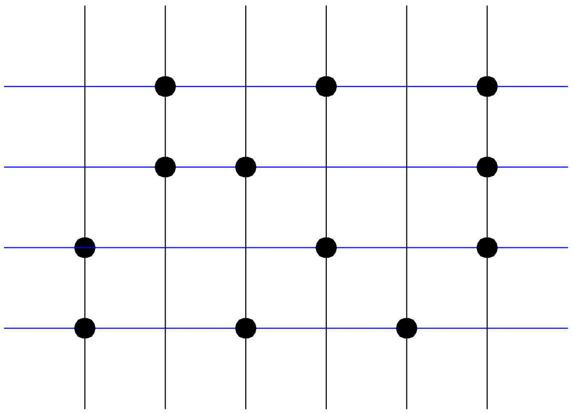
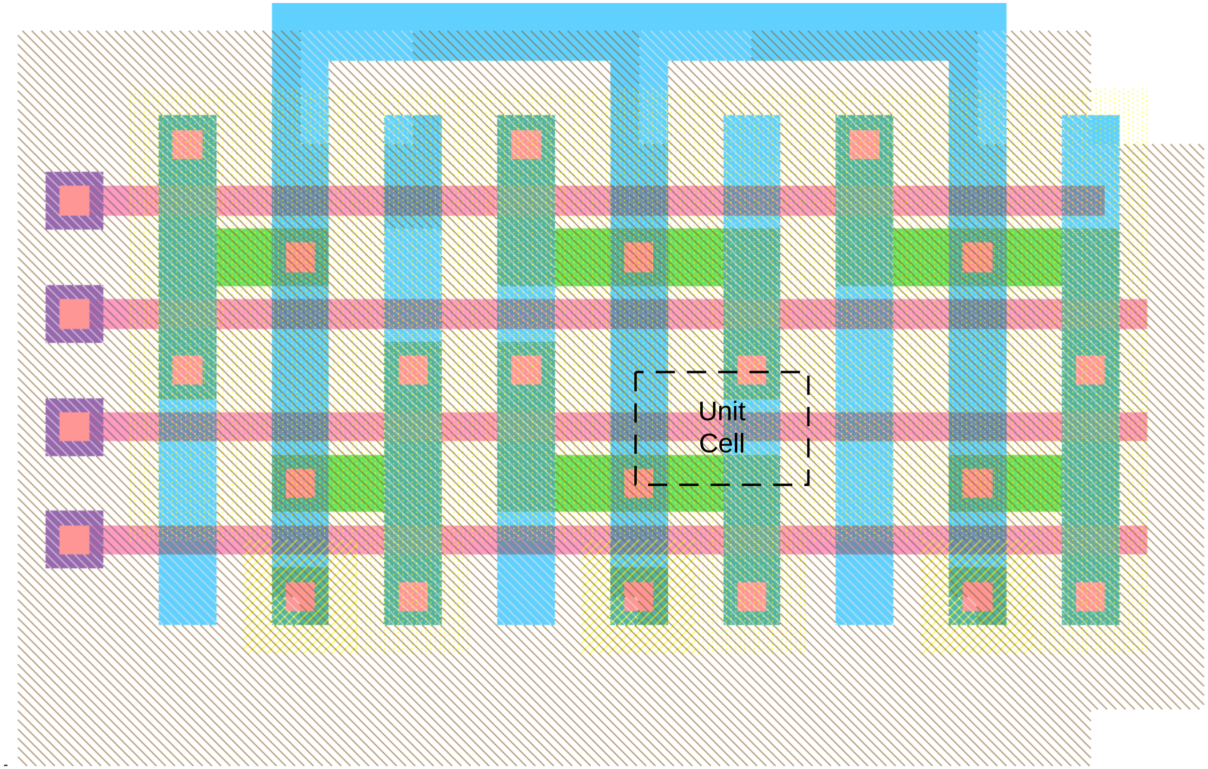




Looks like 6 4-input pseudo-nMOS NORs

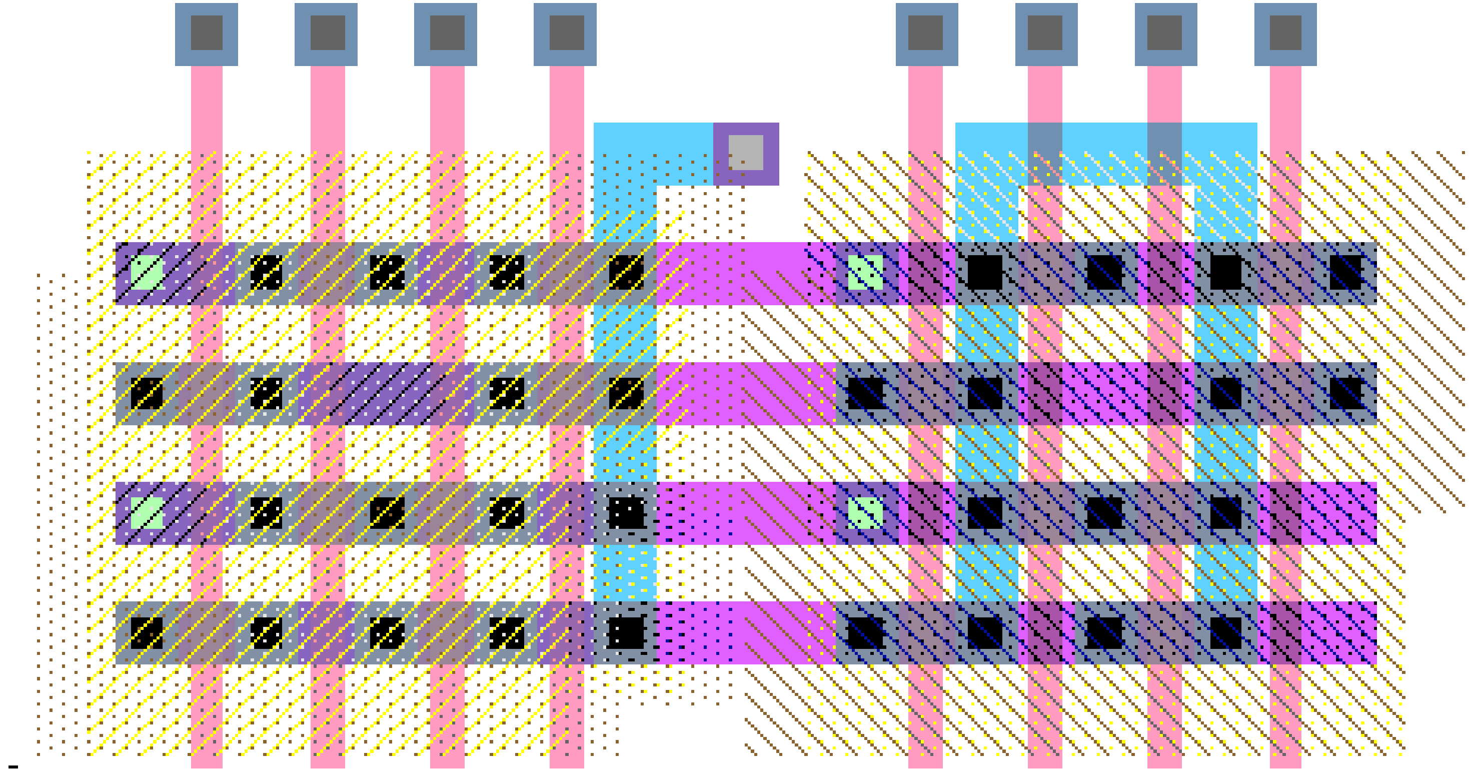
ROM Array Layout

- ❑ Unit cell is 12 x 8 λ (about 1/10 size of SRAM)

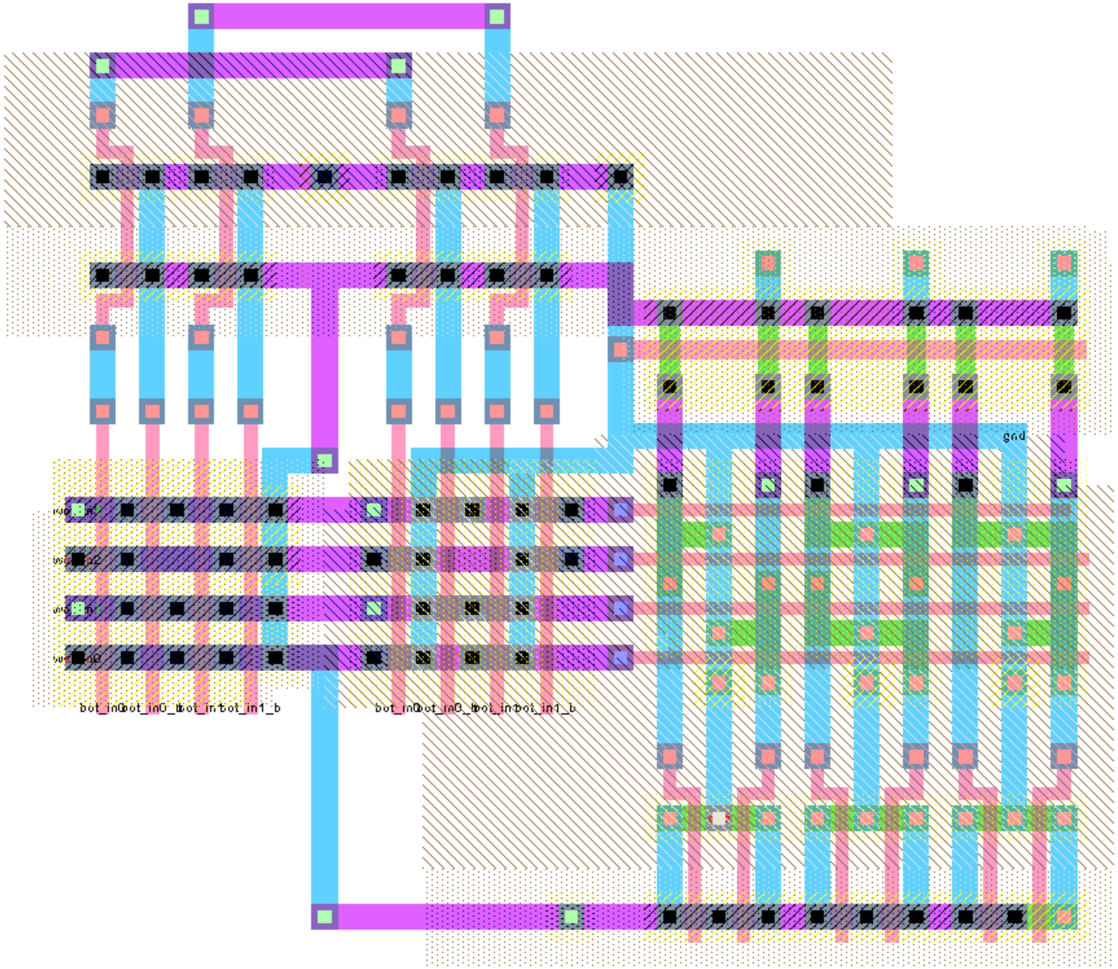


Row Decoders

- ❑ ROM row decoders must pitch-match with ROM
  - – Only a single track per word!

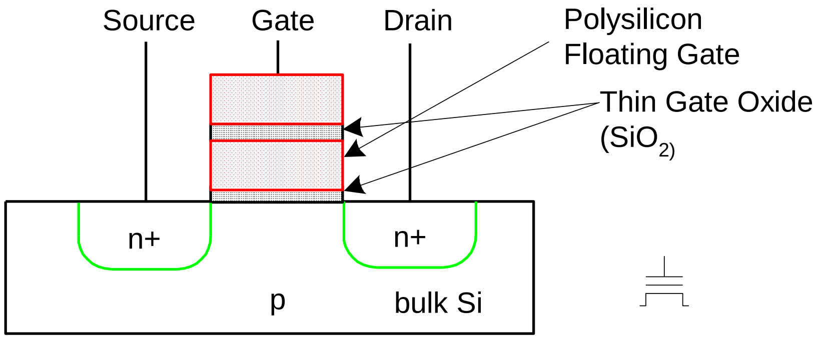


Complete ROM Layout



PROMs and EPROMs

- ❑ Programmable ROMs
  - – Build array with transistors at every site
  - – Burn out fuses to disable unwanted transistors
- ❑ Electrically Programmable ROMs
  - – Use floating gate to turn off unwanted transistors
  - – EPROM, EEPROM, Flash



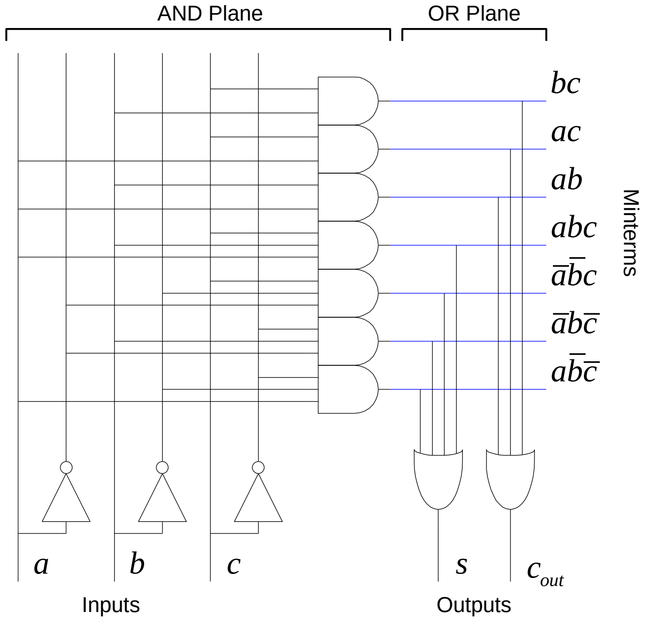
PLAs

- ❑ A *Programmable Logic Array* performs any function in sum-of-products form.
- ❑ *Literals*: inputs & complements
- ❑ *Products / Minterms*: AND of literals
- ❑ *Outputs*: OR of Minterms

- ❑ Example: Full Adder

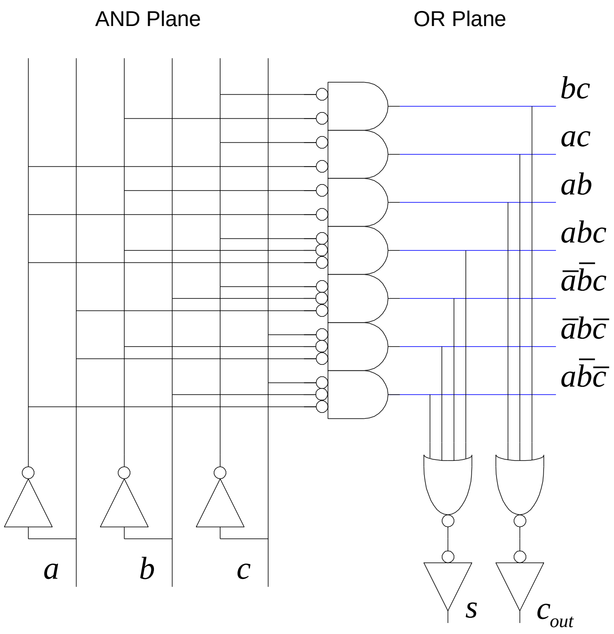
$$s = a\bar{b}\bar{c} + \bar{a}b\bar{c} + \bar{a}\bar{b}c + abc$$

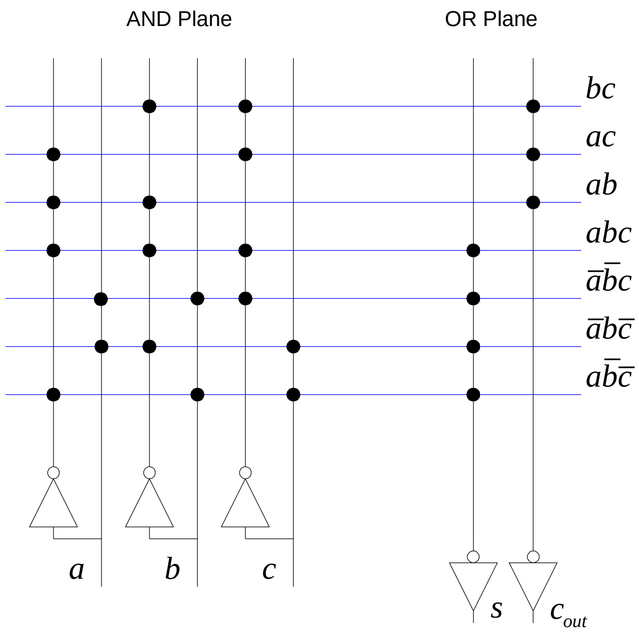
$$c_{\text{out}} = ab + bc + ac$$



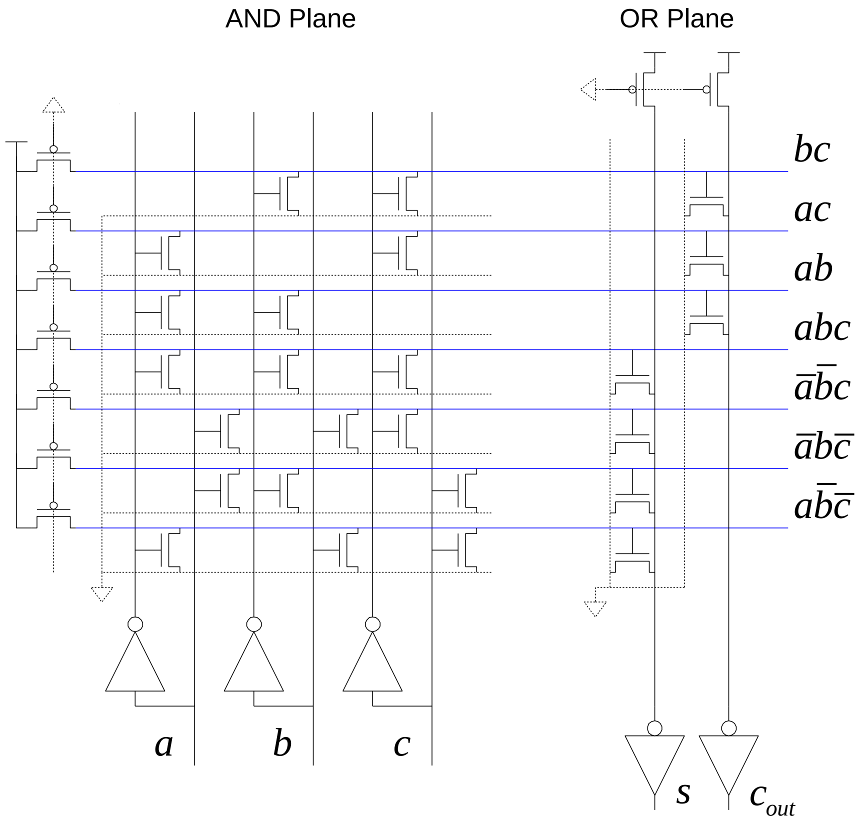
NOR-NOR PLAs

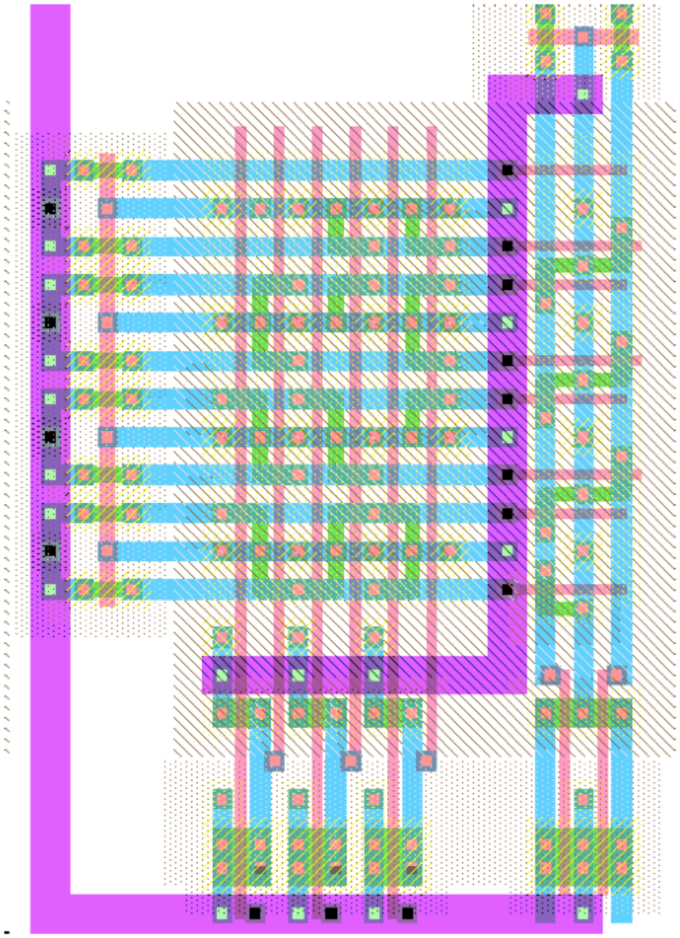
- ❑ ANDs and ORs are not very efficient in CMOS
- ❑ Dynamic or Pseudo-nMOS NORs are very efficient
- ❑ Use DeMorgan’ s Law to convert to all NORs





PLA Schematic & Layout





PLAs vs. ROMs

- The OR plane of the PLA is like the ROM array
- The AND plane of the PLA is like the ROM decoder
- PLAs are more flexible than ROMs
  - No need to have 2^n rows for n inputs
  - Only generate the minterms that are needed
  - Take advantage of logic simplification