Introduction to CMOS VLSI Design

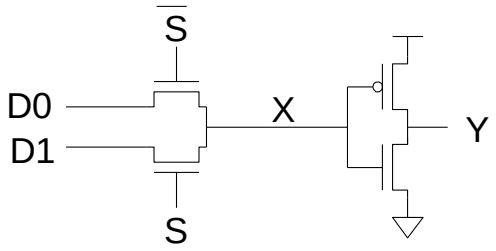
Lecture 16: Circuit Pitfalls

Outline

- Circuit Pitfalls
  - Detective puzzle
  - Given circuit and symptom, diagnose cause and recommend solution
  - All these pitfalls have caused failures in real chips
- Noise Budgets
- Reliability

Bad Circuit 1

- Circuit
  - 2:1 multiplexer



- Principle:

- Solution:

- Symptom
  - Mux works when selected D is 0 but not 1.
  - Or fails at low V_{DD}.
  - Or fails in SFSF corner.

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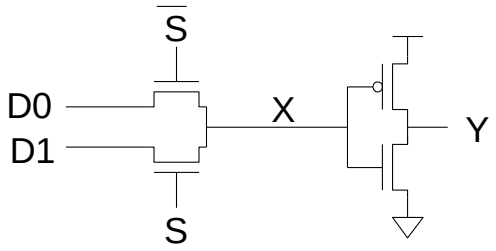

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  - Mux works when selected D is 0 but not 1.
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- Principle: Threshold drop
  - X never rises above V_{DD}-V_t
  - V_t is raised by the body effect
  - The threshold drop is most serious as V_t becomes a greater fraction of V_{DD}.
- Solution:

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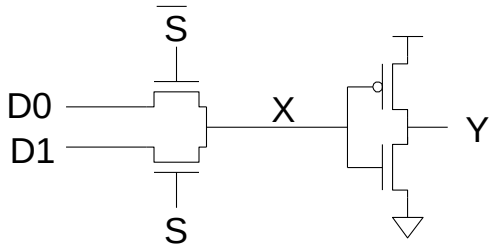

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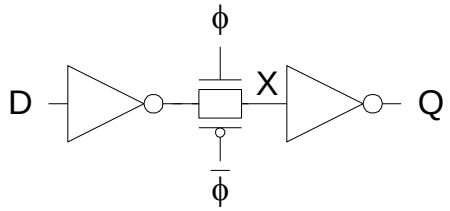
- Principle: Threshold drop
  - X never rises above V_{DD}-V_t
  - V_t is raised by the body effect
  - The threshold drop is most serious as V_t becomes a greater fraction of V_{DD}.
- Solution: Use transmission gates, not pass transistors

Bad Circuit 2

- Circuit
  - Latch



- Symptom
  - Load a 0 into Q
  - Set ϕ = 0
  - Eventually Q spontaneously flips to 1

- Principle:

- Solution:

Bad Circuit 2

- Circuit
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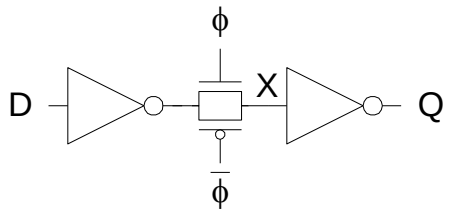

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- Principle: Leakage
  - X is a dynamic node holding value as charge on the node
  - Eventually subthreshold leakage may disturb charge
- Solution:

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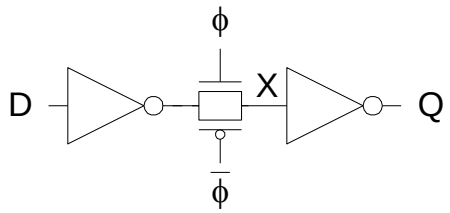

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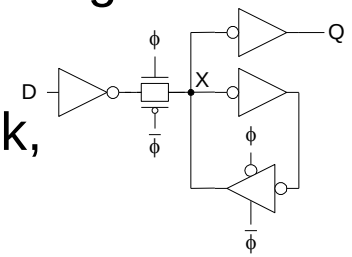
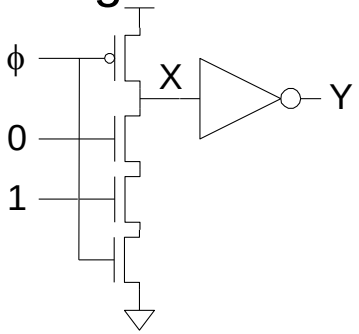
- Principle: Leakage
  - X is a dynamic node holding value as charge on the node
  - Eventually subthreshold leakage may disturb charge
- Solution: Staticize node with feedback
  - Or periodically refresh node (requires fast clock, not practical processes with big leakage)



Bad Circuit 3

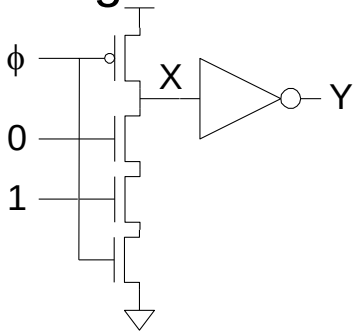
- Circuit
  - Domino AND gate



- Symptom
  - Precharge gate (Y=0)
  - Then evaluate
  - Eventually Y spontaneously flips to 1
- Principle:
- Solution:

Bad Circuit 3

- Circuit
  - Domino AND gate



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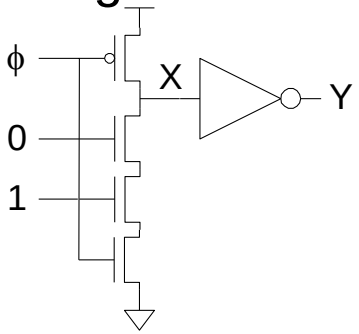

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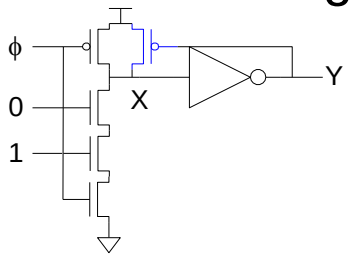
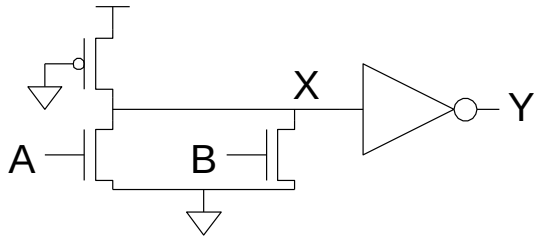
  - Then evaluate
  - Eventually Y spontaneously flips to 1
- Principle: Leakage
  - X is a dynamic node holding value as charge on the node
  - Eventually subthreshold leakage may disturb charge
- Solution: Keeper



Bad Circuit 4

- Circuit
  - Pseudo-nMOS OR



- Principle:

- Solution:

- Symptom
  - When only one input is true, Y = 0.
  - Perhaps only happens in SF corner.

Bad Circuit 4

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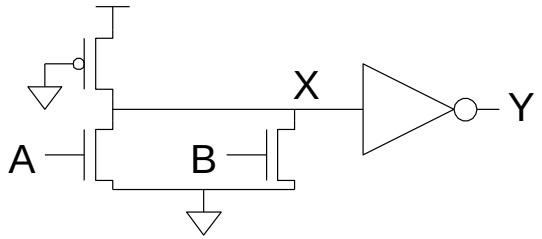
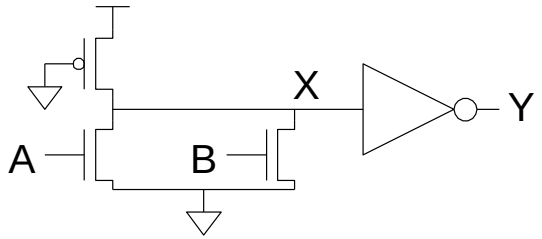


- Symptom
  - When only one input is true, Y = 0.
  - Perhaps only happens in SF corner.
- Principle: Ratio Failure
  - nMOS and pMOS fight each other.
  - If the pMOS is too strong, nMOS cannot pull X low enough.
- Solution:

Bad Circuit 4

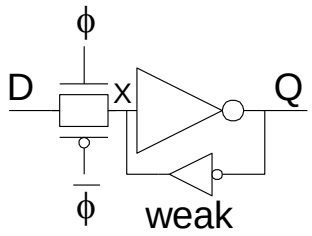
- Circuit
  - Pseudo-nMOS OR



- Symptom
  - When only one input is true, Y = 0.
  - Perhaps only happens in SF corner.
- Principle: Ratio Failure
  - nMOS and pMOS fight each other.
  - If the pMOS is too strong, nMOS cannot pull X low enough.
- Solution: Check that ratio is satisfied in all corners

Bad Circuit 5

- Circuit
  - Latch



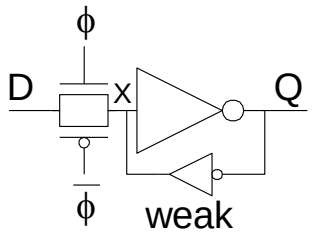
- Principle:

- Solutions:

- Symptom
  - Q stuck at 1.
  - May only happen for certain latches where input is driven by a small gate located far away.

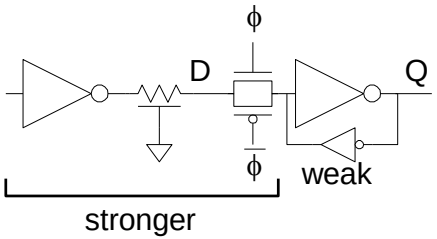
Bad Circuit 5

- Circuit
  - Latch



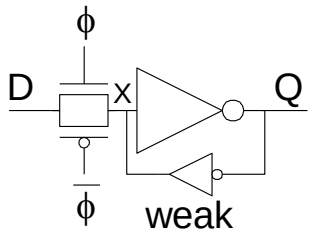
- Principle: Ratio Failure (again)
  - Series resistance of D driver, wire resistance, and tgate must be much less than weak feedback inverter.
- Solutions:

- Symptom
  - Q stuck at 1.
  - May only happen for certain latches where input is driven by a small gate located far away.



Bad Circuit 5

- Circuit
  - Latch



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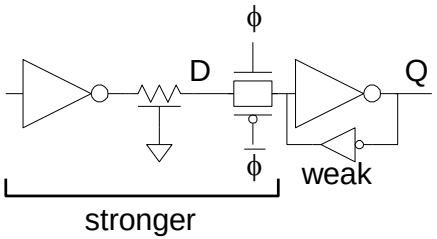
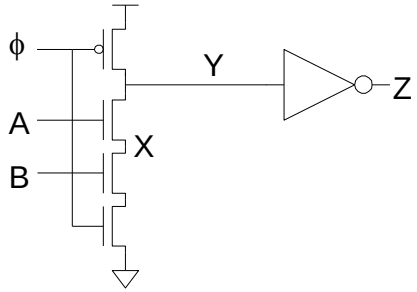


- Solutions: Check relative strengths
  - Avoid unbuffered diffusion inputs where driver is unknown

Bad Circuit 6

- Circuit
  - Domino AND gate



- Principle:

- Solutions:

- Symptom
  - Precharge gate while A = B = 0, so Z = 0
  - Set ϕ = 1
  - A rises
  - Z is observed to sometimes rise

Bad Circuit 6

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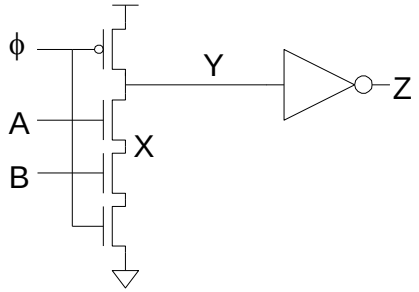
  - Domino AND gate



- Principle: Charge Sharing
  - If X was low, it shares charge with Y
- Solutions:

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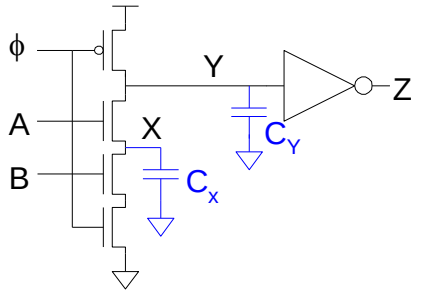

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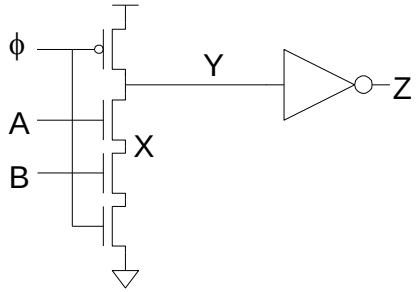

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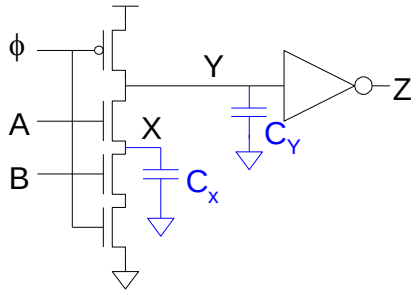
- Principle: Charge Sharing
  - If X was low, it shares charge with Y
- Solutions: Limit charge sharing

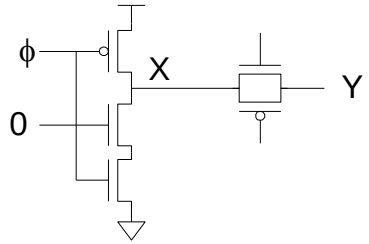
$$V_x = V_Y = \frac{C_Y}{C_x + C_Y} V_{DD}$$

  - Safe if $C_Y >> C_X$
  - Or precharge node X too



Bad Circuit 7

- Circuit
  - Dynamic gate + latch



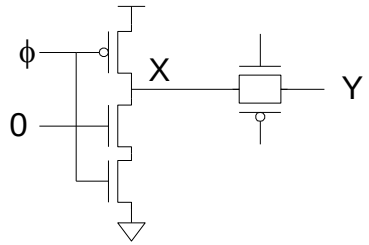
- Principle:

- Solution:

- Symptom
  - Precharge gate while transmission gate latch is opaque
  - Evaluate
  - When latch becomes transparent, X falls

Bad Circuit 7

- Circuit
  - Dynamic gate + latch



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  - Evaluate
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- Principle: Charge Sharing
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- Solution:

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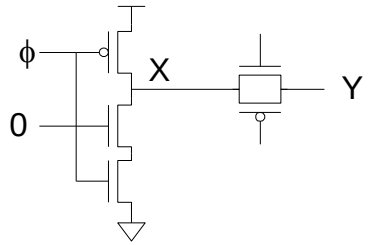
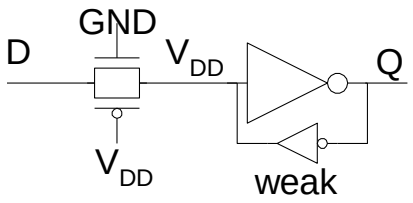


- Symptom
  - Precharge gate while transmission gate latch is opaque
  - Evaluate
  - When latch becomes transparent, X falls
- Principle: Charge Sharing
  - If Y was low, it shares charge with X
- Solution: Buffer dynamic nodes before driving transmission gate

Bad Circuit 8

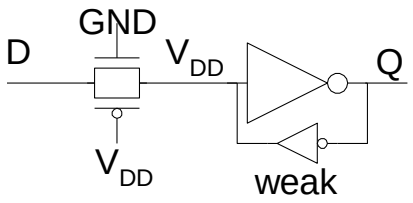
- Circuit
  - Latch



- Symptom
  - Q changes while latch is opaque
  - Especially if D comes from a far-away driver
- Principle:
- Solution:

Bad Circuit 8

- Circuit
  - Latch



- Symptom
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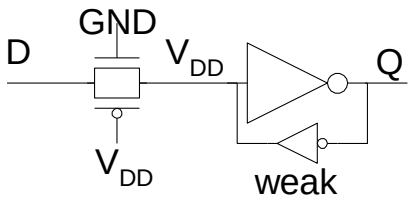
- Principle: Diffusion Input Noise Sensitivity
  - If $D < -V_t$, transmission gate turns on
  - Most likely because of power supply noise or coupling on D
- Solution:

Bad Circuit 8

- Circuit
  - Latch



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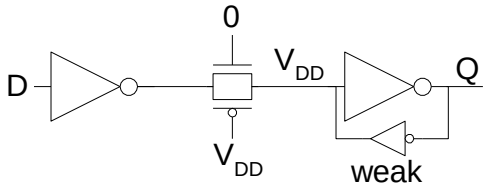
- Solution: Buffer D locally

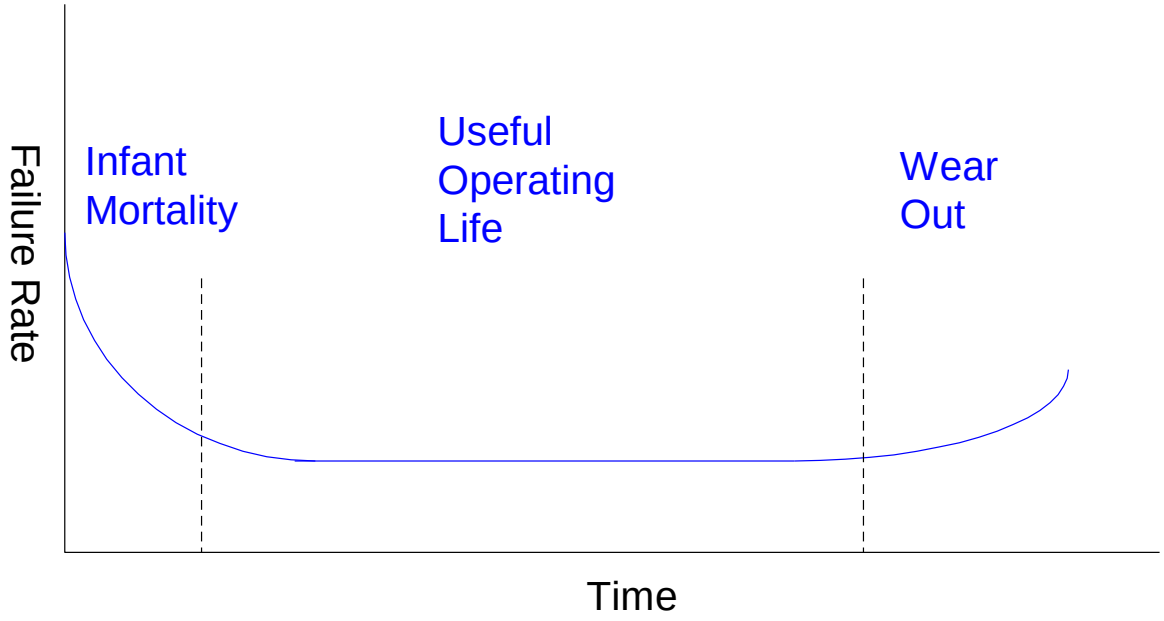


Noise

- Sources
  - Power supply noise / ground bounce
  - Capacitive coupling
  - Charge sharing
  - Leakage
  - Noise feedthrough
- Consequences
  - Increased delay (for noise to settle out)
  - Or incorrect computations

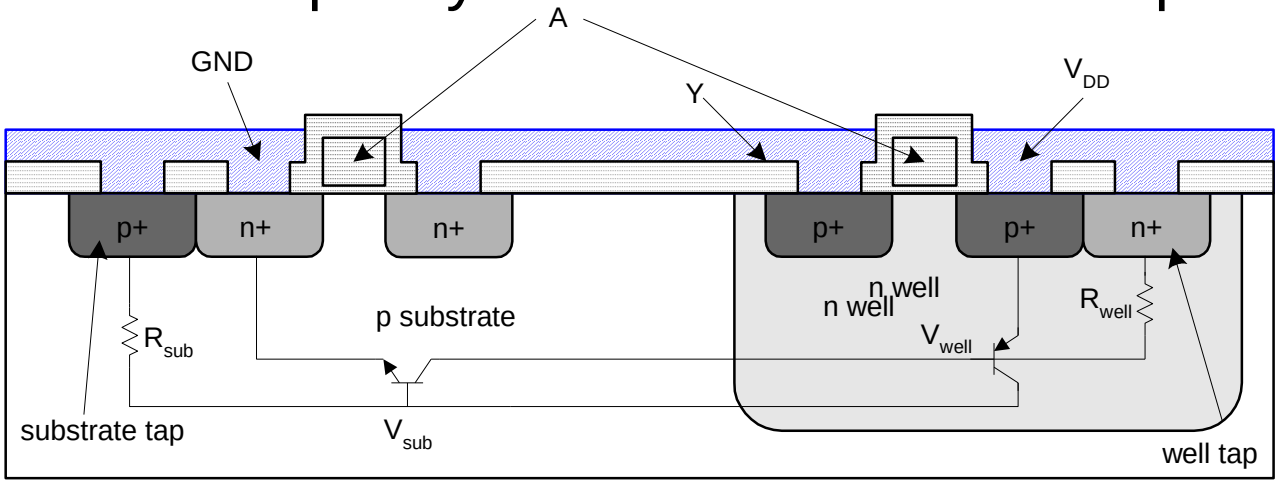
Reliability

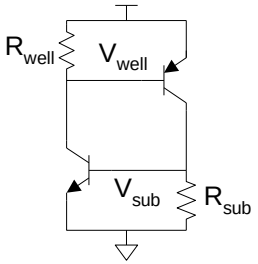
- Hard Errors
- Soft Errors



Latchup

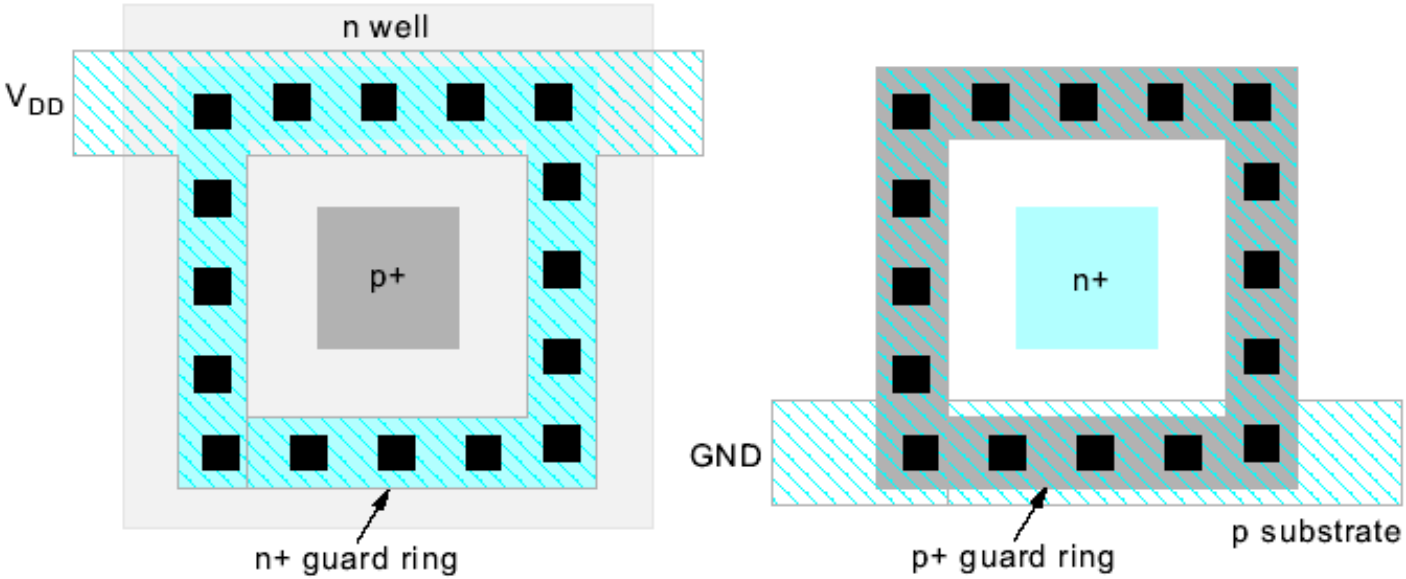
- Latchup: positive feedback leading to V_{DD} – GND short
  - Major problem for 1970's CMOS processes before it was well understood
- Avoid by minimizing resistance of body to GND / V_{DD}
  - Use plenty of substrate and well taps





Guard Rings

- Latchup risk greatest when diffusion-to-substrate diodes could become forward-biased
- Surround sensitive region with guard ring to collect injected charge



Soft Errors

- In 1970's, DRAMs were observed to occasionally flip bits for no apparent reason
  - Ultimately linked to alpha particles and cosmic rays
- Collisions with particles create electron-hole pairs in substrate
  - These carriers are collected on dynamic nodes, disturbing the voltage
- Minimize soft errors by having plenty of charge on dynamic nodes
- Tolerate errors through ECC, redundancy