

# **Introduction to CMOS VLSI Design**

## **Lecture 6: Wires**

### **Outline**

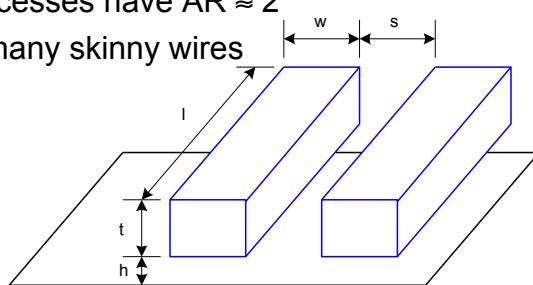
- Introduction
- Wire Resistance
- Wire Capacitance
- Wire RC Delay
- Crosstalk
- Wire Engineering
- Repeaters

# Introduction

- ❑ Chips are mostly made of wires called *interconnect*
  - In stick diagram, wires set size
  - Transistors are little things under the wires
  - Many layers of wires
- ❑ Wires are as important as transistors
  - Speed
  - Power
  - Noise
- ❑ Alternating layers run orthogonally

# Wire Geometry

- ❑ Pitch =  $w + s$
- ❑ Aspect ratio:  $AR = t/w$ 
  - Old processes had  $AR \ll 1$
  - Modern processes have  $AR \approx 2$ 
    - Pack in many skinny wires



## Layer Stack

- AMI 0.6  $\mu\text{m}$  process has 3 metal layers
- Modern processes use 6-10+ metal layers
- Example:
  - Intel 180 nm process
  - M1: thin, narrow ( $< 3\lambda$ )
    - High density cells
  - M2-M4: thicker
    - For longer wires
  - M5-M6: thickest
    - For  $V_{DD}$ , GND, clk

Layer	T (nm)	W (nm)	S (nm)	AR	
6	1720	860	860	2.0	
	1000				
5	1600	800	800	2.0	
	1000				
4	1080	540	540	2.0	
	700				
3	700	320	320	2.2	
	700				
2	700	320	320	2.2	
	700				
1	480	250	250	1.9	
	800				

Substrate

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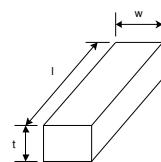
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## Wire Resistance

- $\rho$  = resistivity ( $\Omega \cdot \text{m}$ )

$$R =$$



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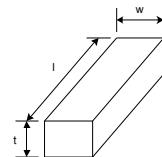
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# Wire Resistance

- ❑  $\rho = \text{resistivity } (\Omega \cdot \text{m})$

$$R = \frac{\rho}{t} \frac{l}{w}$$

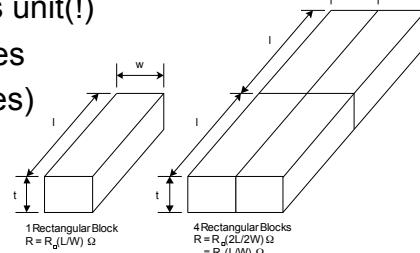


# Wire Resistance

- ❑  $\rho = \text{resistivity } (\Omega \cdot \text{m})$

$$R = \frac{\rho}{t} \frac{l}{w} = R_{\square} \frac{l}{w}$$

- ❑  $R_{\square} = \text{sheet resistance } (\Omega/\square)$ 
  - $\square$  is a dimensionless unit(!)
- ❑ Count number of squares
  - $R = R_{\square} * (\# \text{ of squares})$



## Choice of Metals

- ❑ Until 180 nm generation, most wires were aluminum
- ❑ Modern processes often use copper
  - Cu atoms diffuse into silicon and damage FETs
  - Must be surrounded by a diffusion barrier

Metal	Bulk resistivity ( $\mu\Omega^*cm$ )
Silver (Ag)	1.6
Copper (Cu)	1.7
Gold (Au)	2.2
Aluminum (Al)	2.8
Tungsten (W)	5.3
Molybdenum (Mo)	5.3

## Sheet Resistance

- ❑ Typical sheet resistances in 180 nm process

Layer	Sheet Resistance ( $\Omega/\square$ )
Diffusion (silicided)	3-10
Diffusion (no silicide)	50-200
Polysilicon (silicided)	3-10
Polysilicon (no silicide)	50-400
Metal1	0.08
Metal2	0.05
Metal3	0.05
Metal4	0.03
Metal5	0.02
Metal6	0.02

## Contacts Resistance

- Contacts and vias also have 2-20  $\Omega$
- Use many contacts for lower R
  - Many small contacts for current crowding around periphery



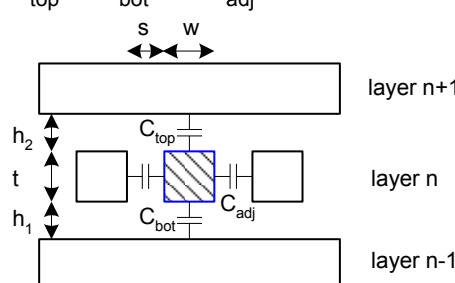
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## Wire Capacitance

- Wire has capacitance per unit length
  - To neighbors
  - To layers above and below
- $C_{\text{total}} = C_{\text{top}} + C_{\text{bot}} + 2C_{\text{adj}}$



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## Capacitance Trends

- Parallel plate equation:  $C = \epsilon A/d$ 
  - Wires are not parallel plates, but obey trends
  - Increasing area ( $W, t$ ) increases capacitance
  - Increasing distance ( $s, h$ ) decreases capacitance
- Dielectric constant
  - $\epsilon = k\epsilon_0$
- $\epsilon_0 = 8.85 \times 10^{-14} \text{ F/cm}$
- $k = 3.9$  for  $\text{SiO}_2$
- Processes are starting to use low- $k$  dielectrics
  - $k \approx 3$  (or less) as dielectrics use air pockets

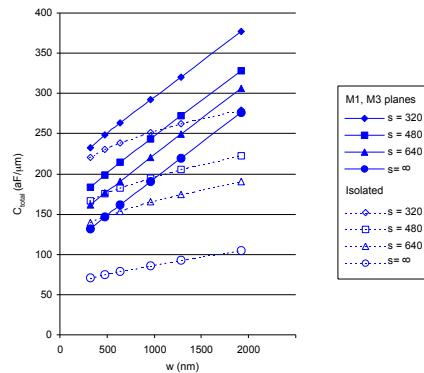
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## M2 Capacitance Data

- Typical wires have  $\sim 0.2 \text{ fF}/\mu\text{m}$ 
  - Compare to  $2 \text{ fF}/\mu\text{m}$  for gate capacitance



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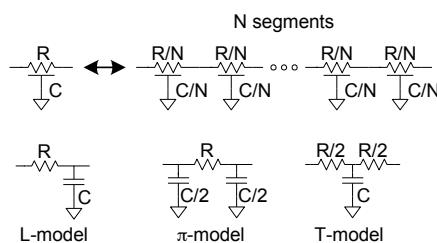
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## Diffusion & Polysilicon

- Diffusion capacitance is very high (about  $2 \text{ fF}/\mu\text{m}$ )
  - Comparable to gate capacitance
  - Diffusion also has high resistance
  - Avoid using diffusion *runners* for wires!
- Polysilicon has lower C but high R
  - Use for transistor gates
  - Occasionally for very short wires between gates

## Lumped Element Models

- Wires are a distributed system
  - Approximate with lumped element models



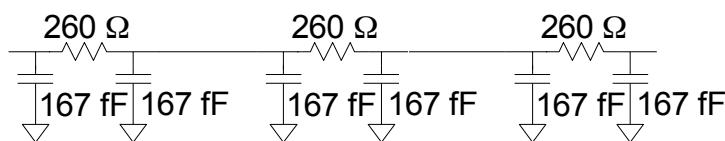
- 3-segment  $\pi$ -model is accurate to 3% in simulation
- L-model needs 100 segments for same accuracy!
- Use single segment  $\pi$ -model for Elmore delay

## Example

- ❑ Metal2 wire in 180 nm process
  - 5 mm long
  - 0.32  $\mu\text{m}$  wide
- ❑ Construct a 3-segment  $\pi$ -model
  - $R_{\square} =$
  - $C_{\text{permicron}} =$

## Example

- ❑ Metal2 wire in 180 nm process
  - 5 mm long
  - 0.32  $\mu\text{m}$  wide
- ❑ Construct a 3-segment  $\pi$ -model
  - $R_{\square} = 0.05 \Omega/\square \Rightarrow R = 781 \Omega$
  - $C_{\text{permicron}} = 0.2 \text{ fF}/\mu\text{m} \Rightarrow C = 1 \text{ pF}$



## Wire RC Delay

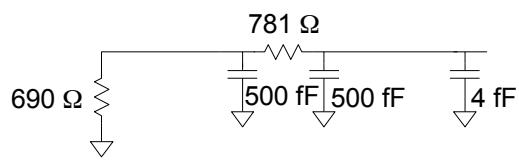
- ❑ Estimate the delay of a 10x inverter driving a 2x inverter at the end of the 5mm wire from the previous example.
  - $R = 2.5 \text{ k}\Omega \cdot \mu\text{m}$  for gates
  - Unit inverter: 0.36  $\mu\text{m}$  nMOS, 0.72  $\mu\text{m}$  pMOS

$$- t_{pd} =$$

## Wire RC Delay

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  - Unit inverter: 0.36  $\mu\text{m}$  nMOS, 0.72  $\mu\text{m}$  pMOS

$$- t_{pd} = 1.1 \text{ ns}$$

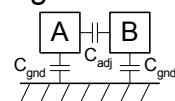


## Crosstalk

- ❑ A capacitor does not like to change its voltage instantaneously.
- ❑ A wire has high capacitance to its neighbor.
  - When the neighbor switches from 1-> 0 or 0->1, the wire tends to switch too.
  - Called capacitive *coupling* or *crosstalk*.
- ❑ Crosstalk effects
  - Noise on nonswitching wires
  - Increased delay on switching wires

## Crosstalk Delay

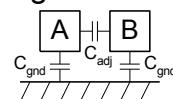
- ❑ Assume layers above and below on average are quiet
  - Second terminal of capacitor can be ignored
  - Model as  $C_{\text{gnd}} = C_{\text{top}} + C_{\text{bot}}$
- ❑ Effective  $C_{\text{adj}}$  depends on behavior of neighbors
  - *Miller effect*



B	$\Delta V$	$C_{\text{eff(A)}}$	MCF
Constant			
Switching with A			
Switching opposite A			

## Crosstalk Delay

- ❑ Assume layers above and below on average are quiet
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  - *Miller effect*



B	$\Delta V$	$C_{\text{eff(A)}}$	MCF
Constant	$V_{\text{DD}}$	$C_{\text{gnd}} + C_{\text{adj}}$	1
Switching with A	0	$C_{\text{gnd}}$	0
Switching opposite A	$2V_{\text{DD}}$	$C_{\text{gnd}} + 2 C_{\text{adj}}$	2

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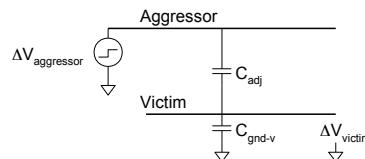
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## Crosstalk Noise

- ❑ Crosstalk causes noise on nonswitching wires
- ❑ If victim is floating:
  - model as capacitive voltage divider

$$\Delta V_{\text{victim}} = \frac{C_{\text{adj}}}{C_{\text{gnd-v}} + C_{\text{adj}}} \Delta V_{\text{aggressor}}$$



6: Wires

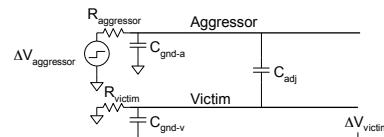
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## Driven Victims

- Usually victim is driven by a gate that fights noise
  - Noise depends on relative resistances
  - Victim driver is in linear region, agg. in saturation
  - If sizes are same,  $R_{\text{aggressor}} = 2-4 \times R_{\text{victim}}$

$$\Delta V_{\text{victim}} = \frac{C_{\text{adj}}}{C_{\text{gnd-v}} + C_{\text{adj}}} \frac{1}{1+k} \Delta V_{\text{aggressor}}$$



$$k = \frac{\tau_{\text{aggressor}}}{\tau_{\text{victim}}} = \frac{R_{\text{aggressor}} (C_{\text{gnd-a}} + C_{\text{adj}})}{R_{\text{victim}} (C_{\text{gnd-v}} + C_{\text{adj}})}$$

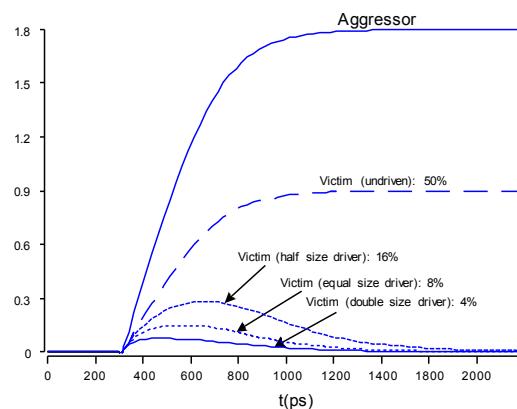
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## Coupling Waveforms

- Simulated coupling for  $C_{\text{adj}} = C_{\text{victim}}$



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## Noise Implications

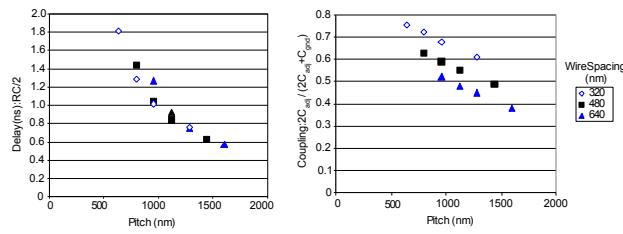
- ❑ So what if we have noise?
- ❑ If the noise is less than the noise margin, nothing happens
- ❑ Static CMOS logic will eventually settle to correct output even if disturbed by large noise spikes
  - But glitches cause extra delay
  - Also cause extra power from false transitions
- ❑ Dynamic logic never recovers from glitches
- ❑ Memories and other sensitive circuits also can produce the wrong answer

## Wire Engineering

- ❑ Goal: achieve delay, area, power goals with acceptable noise
- ❑ Degrees of freedom:

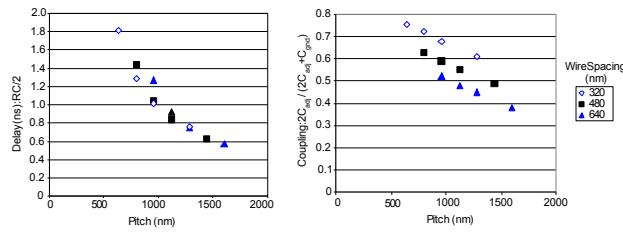
# Wire Engineering

- ❑ Goal: achieve delay, area, power goals with acceptable noise
- ❑ Degrees of freedom:
  - Width
  - Spacing



# Wire Engineering

- ❑ Goal: achieve delay, area, power goals with acceptable noise
- ❑ Degrees of freedom:
  - Width
  - Spacing
  - Layer

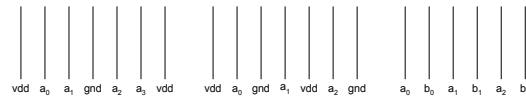
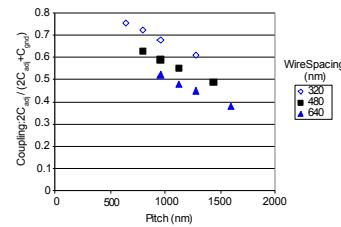
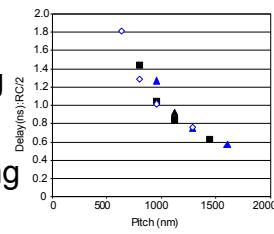


# Wire Engineering

- ❑ Goal: achieve delay, area, power goals with acceptable noise

- ❑ Degrees of freedom:

- Width
- Spacing
- Layer
- Shielding



6: Wires

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# Repeaters

- ❑ R and C are proportional to  $l$
- ❑ RC delay is proportional to  $l^2$ 
  - Unacceptably great for long wires

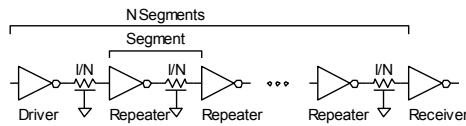
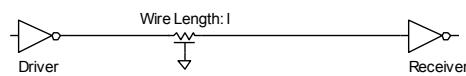
6: Wires

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## Repeaters

- ❑ R and C are proportional to  $l$
- ❑ RC delay is proportional to  $l^2$ 
  - Unacceptably great for long wires
- ❑ Break long wires into N shorter segments
  - Drive each one with an inverter or buffer



6: Wires

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## Repeater Design

- ❑ How many repeaters should we use?
- ❑ How large should each one be?
- ❑ Equivalent Circuit
  - Wire length  $l/N$ 
    - Wire Capacitance  $C_w * l/N$ , Resistance  $R_w * l/N$
    - Inverter width W (nMOS = W, pMOS = 2W)
      - Gate Capacitance  $C' * W$ , Resistance  $R/W$

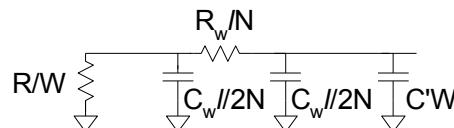
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## Repeater Design

- ❑ How many repeaters should we use?
- ❑ How large should each one be?
- ❑ Equivalent Circuit
  - Wire length  $l$ 
    - Wire Capacitance  $C_w * l$ , Resistance  $R_w * l$
  - Inverter width  $W$  (nMOS =  $W$ , pMOS =  $2W$ )
    - Gate Capacitance  $C' * W$ , Resistance  $R/W$



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## Repeater Results

- ❑ Write equation for Elmore Delay
  - Differentiate with respect to  $W$  and  $N$
  - Set equal to 0, solve

$$\frac{l}{N} = \sqrt{\frac{2RC'}{R_w C_w}}$$

$$\frac{t_{pd}}{l} = (2 + \sqrt{2}) \sqrt{RC'R_w C_w} \quad \begin{matrix} \sim 60-80 \text{ ps/mm} \\ \text{in 180 nm process} \end{matrix}$$

$$W = \sqrt{\frac{RC_w}{R_w C'}}$$

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