Computer-Aided VLSI System Design
Homework 5 Report

Due Tuesday, Dec. 3, 13:59

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Student Name:葉冠宏

APR Results

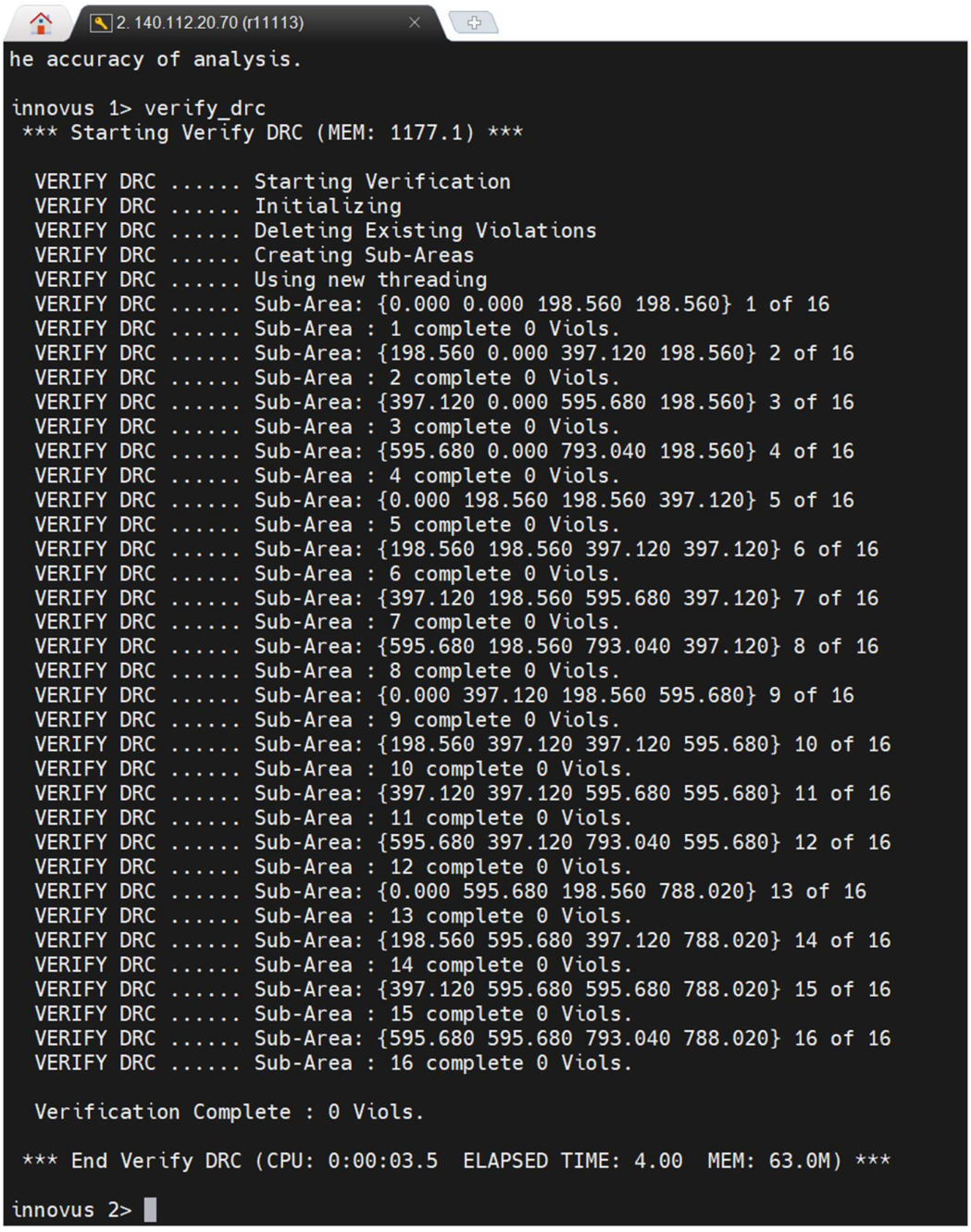
1. Fill in the blanks below.

Design Stage	Description	Value
P&R	Number of DRC violations (ex: 0) (Verify -> Verify Geometry…)	0
	Number of LVS violations (ex: 0) (Verify -> Verify Connectivity…)	0
	Die Area (um^2)	624931.38
	Core Area (um^2)	397055.81
Post-layout Simulation	Clock Period for Post-layout Simulation (ex. 10ns)	15.18ns
Follow your design in HW3? (If not, specify student ID of the designer or 'from TA')		Yes

Questions and Discussion

1. Attach the snapshot of CCOpt Clock Tree Debugger result (5%).

2. Attach the snapshot of DRC and LVS checking after routing. (5%)



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innovus 2> VERIFY_CONNECTIVITY use new engine.

******** Start: VERIFY CONNECTIVITY ********
Start Time: Fri Nov 29 13:49:49 2024

Design Name: core
Database Units: 2000
Design Boundary: (0.0000, 0.0000) (793.0400, 788.0200)
Error Limit = 1000; Warning Limit = 50
Check all nets
**** 13:49:49 **** Processed 5000 nets.
**** 13:49:50 **** Processed 10000 nets.

Begin Summary
  Found no problems or warnings.
End Summary

End Time: Fri Nov 29 13:49:50 2024
Time Elapsed: 0:00:01.0

******** End: VERIFY CONNECTIVITY ********
  Verification Complete : 0 Viols.  0 Wrngs.
  (CPU Time: 0:00:01.4  MEM: 25.000M)

innovus 2>
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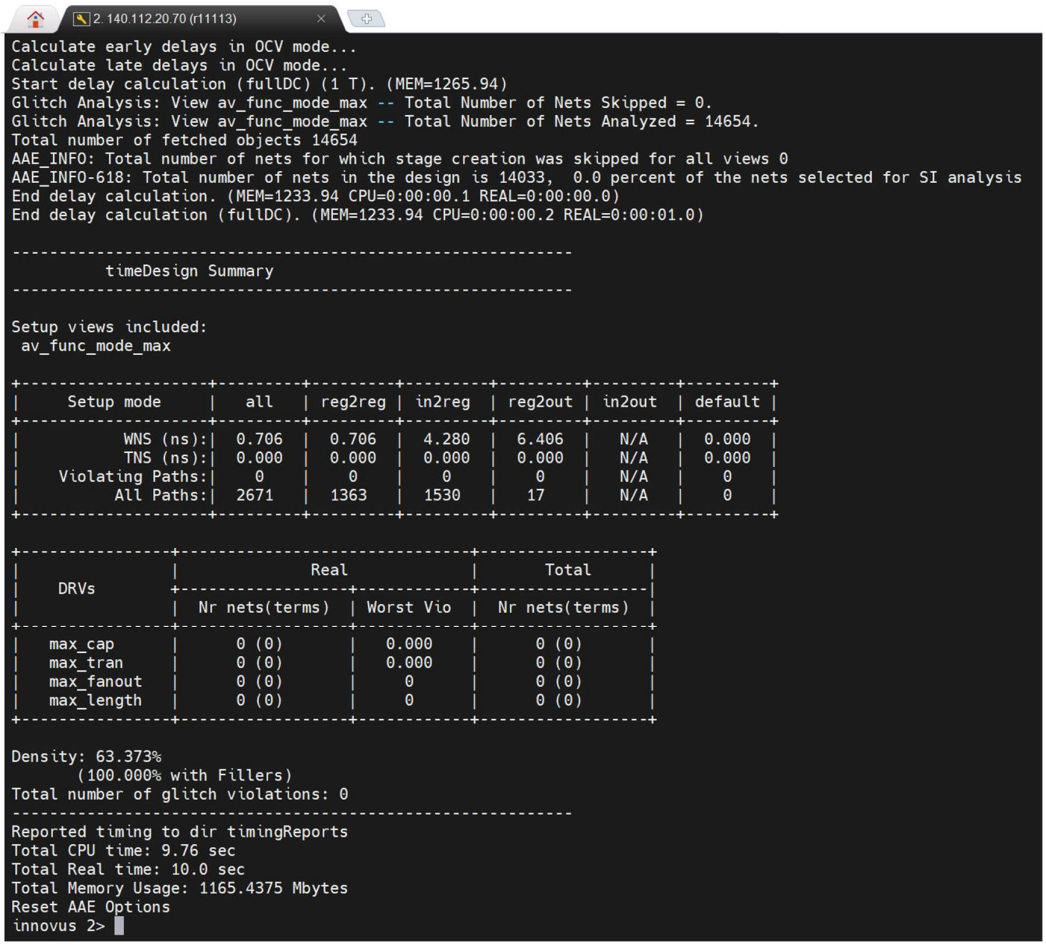
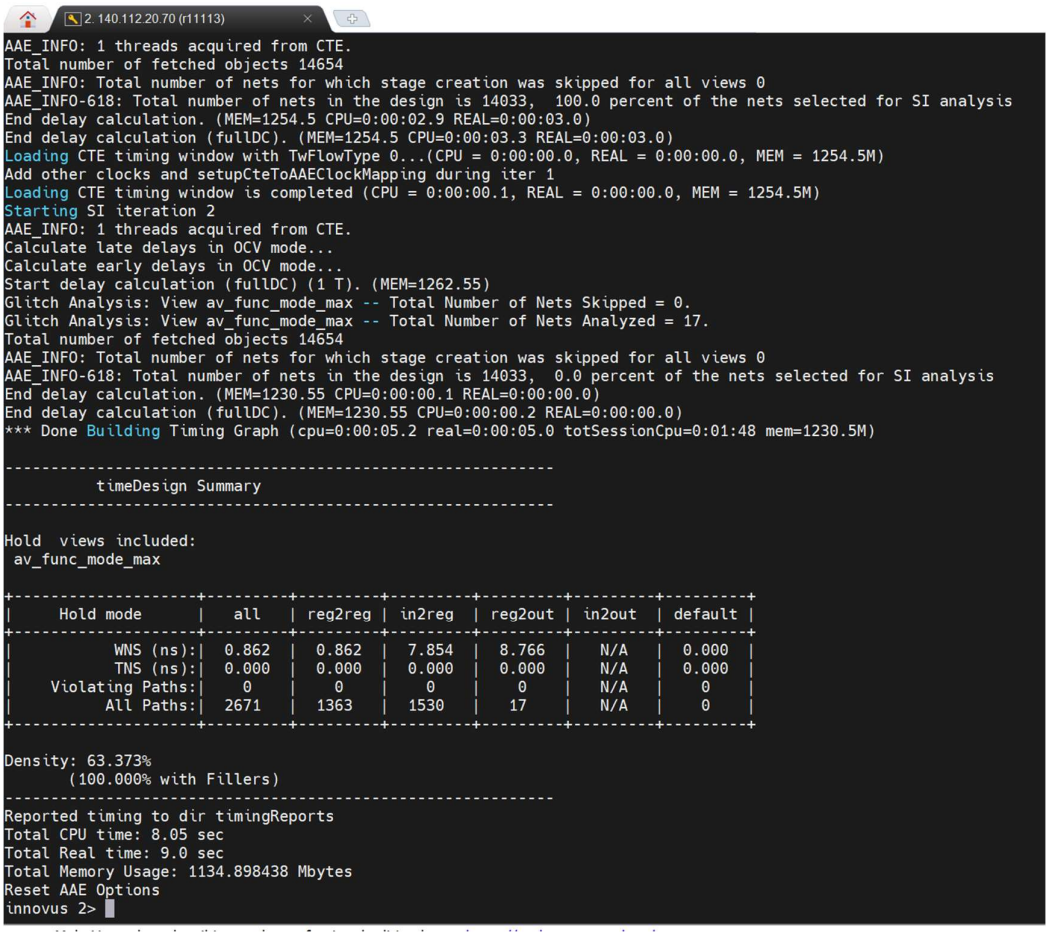
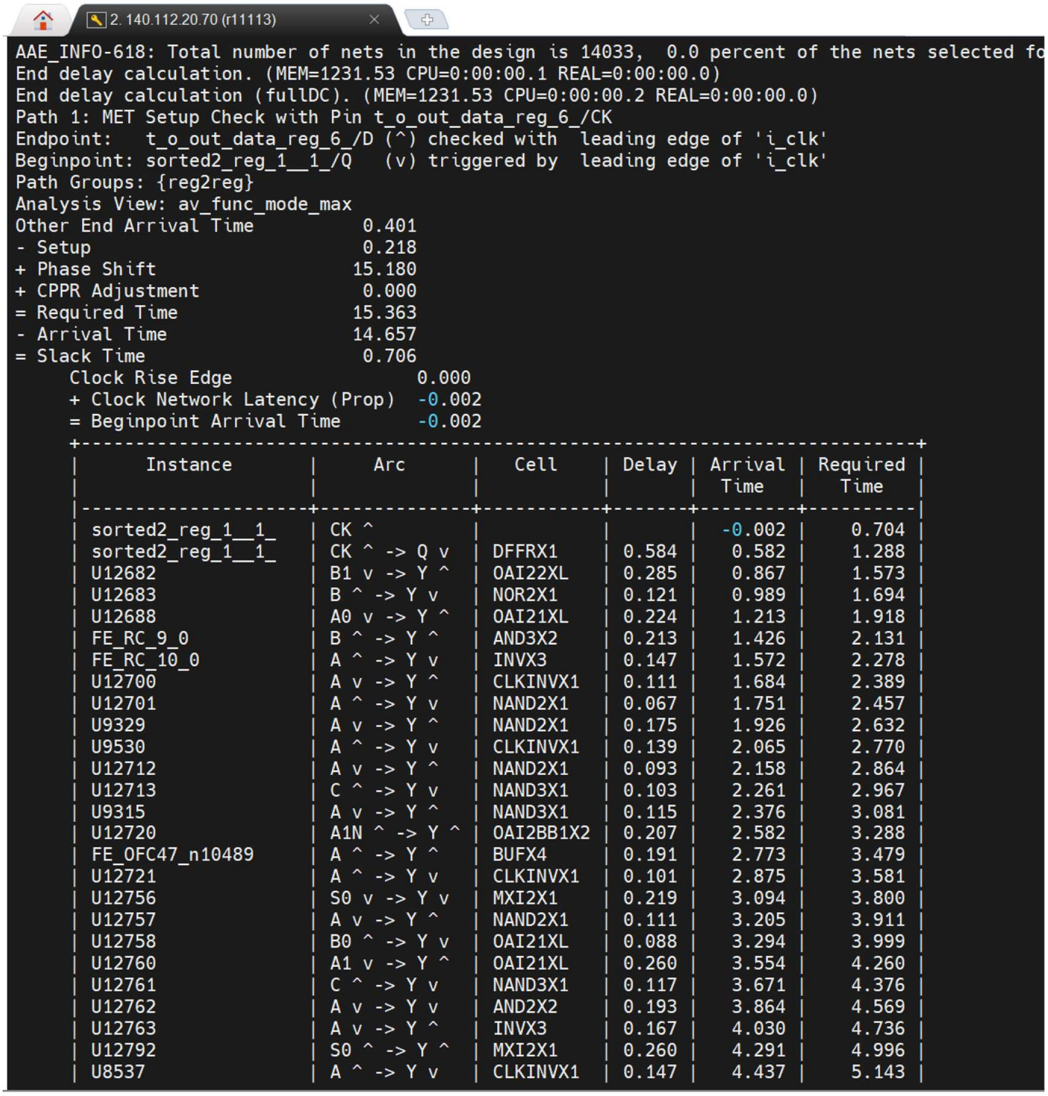
3. Attach the snapshot of the timing report for **setup time and hold time** with no timing violation (post-route). (5%)




2. 140.112.20.70 (r11113)
AAE_INFO: 1 threads acquired from CTE.
Total number of fetched objects 14654
AAE_INFO: Total number of nets for which stage creation was skipped for all views 0
AAE_INFO-618: Total number of nets in the design is 14033, 100.0 percent of the nets selected for SI analysis
End delay calculation. (MEM=1254.5 CPU=0:00:02.9 REAL=0:00:03.0)
End delay calculation (fullDC). (MEM=1254.5 CPU=0:00:03.3 REAL=0:00:03.0)
Loading CTE timing window with TwFlowType 0...(CPU = 0:00:00.0, REAL = 0:00:00.0, MEM = 1254.5M)
Add other clocks and setupCteToAAEClockMapping during iter 1
Loading CTE timing window is completed (CPU = 0:00:00.1, REAL = 0:00:00.0, MEM = 1254.5M)
Starting SI iteration 2
AAE_INFO: 1 threads acquired from CTE.
Calculate late delays in OCV mode...
Calculate early delays in OCV mode...
Start delay calculation (fullDC) (1 T). (MEM=1262.55)
Glitch Analysis: View av_func_mode_max -- Total Number of Nets Skipped = 0.
Glitch Analysis: View av_func_mode_max -- Total Number of Nets Analyzed = 17.
Total number of fetched objects 14654
AAE_INFO: Total number of nets for which stage creation was skipped for all views 0
AAE_INFO-618: Total number of nets in the design is 14033, 0.0 percent of the nets selected for SI analysis
End delay calculation. (MEM=1230.55 CPU=0:00:00.1 REAL=0:00:00.0)
End delay calculation (fullDC). (MEM=1230.55 CPU=0:00:00.2 REAL=0:00:00.0)
*** Done Building Timing Graph (cpu=0:00:05.2 real=0:00:05.0 totSessionCpu=0:01:48 mem=1230.5M)
timeDesign Summary
Hold views included:
av_func_mode_max
Hold mode | all | reg2reg | in2reg | reg2out | in2out | default
WNS (ns): | 0.862 | 0.862 | 7.854 | 8.766 | N/A | 0.000
TNS (ns): | 0.000 | 0.000 | 0.000 | 0.000 | N/A | 0.000
Violating Paths: | 0 | 0 | 0 | 0 | N/A | 0
All Paths: | 2671 | 1363 | 1530 | 17 | N/A | 0
Density: 63.373%
(100.000% with Fillers)
Reported timing to dir timingReports
Total CPU time: 8.05 sec
Total Real time: 9.0 sec
Total Memory Usage: 1134.898438 Mbytes
Reset AAE Options
innovus 2>

4. Show the critical path after post-route optimization. What is the path type? (10%)
   (The slack of the critical path should match the smallest slack in the timing report)



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2. 140.112.20.70 (r11113)
AAE_INFO-618: Total number of nets in the design is 14033,  0.0 percent of the nets selected fo
End delay calculation. (MEM=1231.53 CPU=0:00:00.1 REAL=0:00:00.0)
End delay calculation (fullDC). (MEM=1231.53 CPU=0:00:00.2 REAL=0:00:00.0)
Path 1: MET Setup Check with Pin t_o_out_data_reg_6_/CK
Endpoint:   t_o_out_data_reg_6_/D (^) checked with  leading edge of 'i_clk'
Beginpoint: sorted2_reg_1__1_/Q   (v) triggered by  leading edge of 'i_clk'
Path Groups: {reg2reg}
Analysis View: av_func_mode_max
Other End Arrival Time          0.401
- Setup                         0.218
+ Phase Shift                  15.180
+ CPPR Adjustment               0.000
= Required Time                15.363
- Arrival Time                 14.657
= Slack Time                    0.706
     Clock Rise Edge                0.000
     + Clock Network Latency (Prop)  -0.002
     = Beginpoint Arrival Time       -0.002
     +-------------------------------------------------------------------------------+
     |      Instance       |     Arc      |   Cell    | Delay | Arrival | Required |
     |                     |              |           |       |  Time   |   Time   |
     |---------------------+--------------+-----------+-------+---------+----------|
     | sorted2_reg_1__1_   | CK ^         |           |       |  -0.002 |    0.704 |
     | sorted2_reg_1__1_   | CK ^ -> Q v  | DFFRX1    | 0.584 |   0.582 |    1.288 |
     | U12682              | B1 v -> Y ^  | OAI22XL   | 0.285 |   0.867 |    1.573 |
     | U12683              | B ^ -> Y v   | NOR2X1    | 0.121 |   0.989 |    1.694 |
     | U12688              | A0 v -> Y ^  | OAI21XL   | 0.224 |   1.213 |    1.918 |
     | FE_RC_9_0           | B ^ -> Y ^   | AND3X2    | 0.213 |   1.426 |    2.131 |
     | FE_RC_10_0          | A ^ -> Y v   | INVX3     | 0.147 |   1.572 |    2.278 |
     | U12700              | A v -> Y ^   | CLKINVX1  | 0.111 |   1.684 |    2.389 |
     | U12701              | A ^ -> Y v   | NAND2X1   | 0.067 |   1.751 |    2.457 |
     | U9329               | A v -> Y ^   | NAND2X1   | 0.175 |   1.926 |    2.632 |
     | U9530               | A ^ -> Y v   | CLKINVX1  | 0.139 |   2.065 |    2.770 |
     | U12712              | A v -> Y ^   | NAND2X1   | 0.093 |   2.158 |    2.864 |
     | U12713              | C ^ -> Y v   | NAND3X1   | 0.103 |   2.261 |    2.967 |
     | U9315               | A v -> Y ^   | NAND3X1   | 0.115 |   2.376 |    3.081 |
     | U12720              | A1N ^ -> Y ^ | OAI2BB1X2 | 0.207 |   2.582 |    3.288 |
     | FE_OFC47_n10489     | A ^ -> Y ^   | BUFX4     | 0.191 |   2.773 |    3.479 |
     | U12721              | A ^ -> Y v   | CLKINVX1  | 0.101 |   2.875 |    3.581 |
     | U12756              | S0 v -> Y v  | MXI2X1    | 0.219 |   3.094 |    3.800 |
     | U12757              | A v -> Y ^   | NAND2X1   | 0.111 |   3.205 |    3.911 |
     | U12758              | B0 ^ -> Y v  | OAI21XL   | 0.088 |   3.294 |    3.999 |
     | U12760              | A1 v -> Y ^  | OAI21XL   | 0.260 |   3.554 |    4.260 |
     | U12761              | C ^ -> Y v   | NAND3X1   | 0.117 |   3.671 |    4.376 |
     | U12762              | A v -> Y v   | AND2X2    | 0.193 |   3.864 |    4.569 |
     | U12763              | A v -> Y ^   | INVX3     | 0.167 |   4.030 |    4.736 |
     | U12792              | S0 ^ -> Y ^  | MXI2X1    | 0.260 |   4.291 |    4.996 |
     | U8537               | A ^ -> Y v   | CLKINVX1  | 0.147 |   4.437 |    5.143 |
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U8537	A ^ -> Y v	CLKINVX1	0.147	4.437	5.143
U9079	A v -> Y ^	NAND2X1	0.104	4.541	5.247
U12798	A ^ -> Y v	NAND3X1	0.083	4.624	5.330
U12801	B0 v -> Y ^	AOI2BB2X1	0.226	4.850	5.556
U12802	B ^ -> Y v	NAND2X4	0.201	5.051	5.756
U12961	S0 v -> Y ^	MXI2X1	0.356	5.407	6.113
U12962	A ^ -> Y v	CLKINVX1	0.156	5.563	6.269
U10968	A v -> Y ^	NAND2X1	0.111	5.674	6.379
U12976	A ^ -> Y v	NAND3X1	0.071	5.744	6.450
U12980	A1N v -> Y v	OAI2BB1X1	0.173	5.917	6.623
U10239	A v -> Y ^	NAND3X1	0.117	6.034	6.740
U12983	A ^ -> Y v	NAND2X2	0.212	6.246	6.951
U12999	S0 v -> Y ^	MXI2X1	0.308	6.553	7.259
U13010	A ^ -> Y v	CLKINVX1	0.140	6.694	7.400
U10194	A1 v -> Y ^	OAI21XL	0.271	6.964	7.670
U13012	D ^ -> Y v	NAND4BX1	0.156	7.121	7.826
U9014	B v -> Y v	AND3X2	0.224	7.345	8.051
U9413	A v -> Y ^	INVX3	0.187	7.531	8.237
U13029	S0 ^ -> Y ^	MXI2X1	0.302	7.834	8.539
U9007	A ^ -> Y v	CLKINVX1	0.155	7.988	8.694
U13038	A v -> Y ^	NAND2X1	0.114	8.102	8.808
U13043	B ^ -> Y v	NAND3X1	0.090	8.192	8.898
U13044	B v -> Y ^	NOR2X1	0.107	8.300	9.005
U13045	B ^ -> Y v	NAND2X1	0.067	8.366	9.072
U13050	A v -> Y v	AND3X2	0.193	8.560	9.265
U13051	A v -> Y ^	INVX4	0.159	8.719	9.425
U13064	S0 ^ -> Y ^	MXI2X1	0.306	9.025	9.731
U8128	A ^ -> Y v	INVX1	0.090	9.115	9.821
U10080	B v -> Y ^	NAND2X1	0.096	9.211	9.917
U13076	B0 ^ -> Y v	OAI21XL	0.088	9.299	10.005
U13077	B v -> Y ^	NAND2X1	0.121	9.421	10.126
U13078	C ^ -> Y v	NAND3X1	0.146	9.567	10.272
U13084	A v -> Y ^	NAND2X4	0.185	9.751	10.457
U13087	S0 ^ -> Y ^	MXI2X1	0.403	10.155	10.860
U13088	A ^ -> Y v	CLKINVX1	0.170	10.325	11.031
U13095	A0 v -> Y ^	OAI21XL	0.247	10.572	11.278
U7935	B0 ^ -> Y v	OAI21XL	0.125	10.697	11.403
U13096	A v -> Y v	AND2X2	0.223	10.920	11.626
U13394	B v -> Y ^	NAND2X4	0.178	11.098	11.804
U13406	S0 ^ -> Y ^	MXI2X1	0.218	11.316	12.022
U13410	A ^ -> Y v	CLKINVX1	0.105	11.421	12.127
U13411	B v -> Y ^	NAND2X1	0.109	11.530	12.236
U13413	B ^ -> Y v	NAND3X1	0.110	11.640	12.346
U13422	C v -> Y ^	NAND4X1	0.241	11.881	12.586
U9363	A ^ -> Y v	NAND4X4	0.192	12.072	12.778
U13434	S0 v -> Y ^	MXI2X1	0.329	12.401	13.107

U13434	S0 v -> Y ^	MXI2X1	0.329	12.401	13.107
U7691	A ^ -> Y v	INVX1	0.143	12.544	13.250
U13469	A0 v -> Y ^	OAI21X1	0.197	12.741	13.446
U13473	C ^ -> Y v	NAND4BX1	0.137	12.878	13.584
U9996	A v -> Y v	AND2X2	0.225	13.103	13.809
U13499	A v -> Y ^	NAND2X8	0.108	13.211	13.917
U13501	S0 ^ -> Y ^	MXI2X4	0.124	13.335	14.041
U7603	A ^ -> Y v	NAND2X1	0.096	13.432	14.137
U13503	B0 v -> Y ^	OAI21X1	0.118	13.550	14.256
U13507	A ^ -> Y v	NAND3X2	0.113	13.663	14.368
U7556	A v -> Y ^	NAND2X1	0.164	13.827	14.532
U14751	A0 ^ -> Y v	AOI21X1	0.130	13.957	14.662
U14752	B0 v -> Y ^	OAI21X2	0.371	14.328	15.034
U15453	A ^ -> Y v	NOR2X2	0.180	14.508	15.214
U15455	C v -> Y ^	NAND4X1	0.150	14.657	15.363
t_o_out_data_reg_6_	D ^	DFFRX1	0.000	14.657	15.363

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ovus 3>
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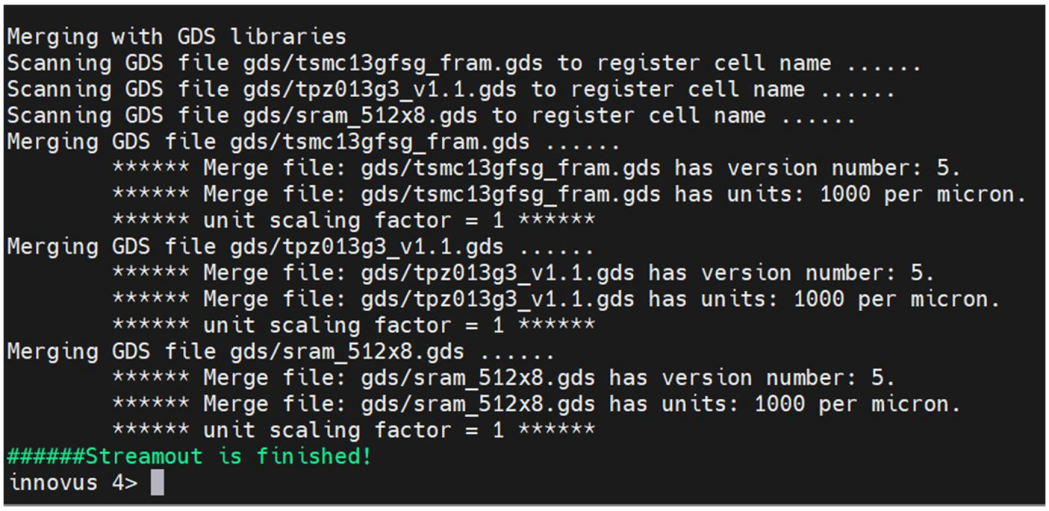
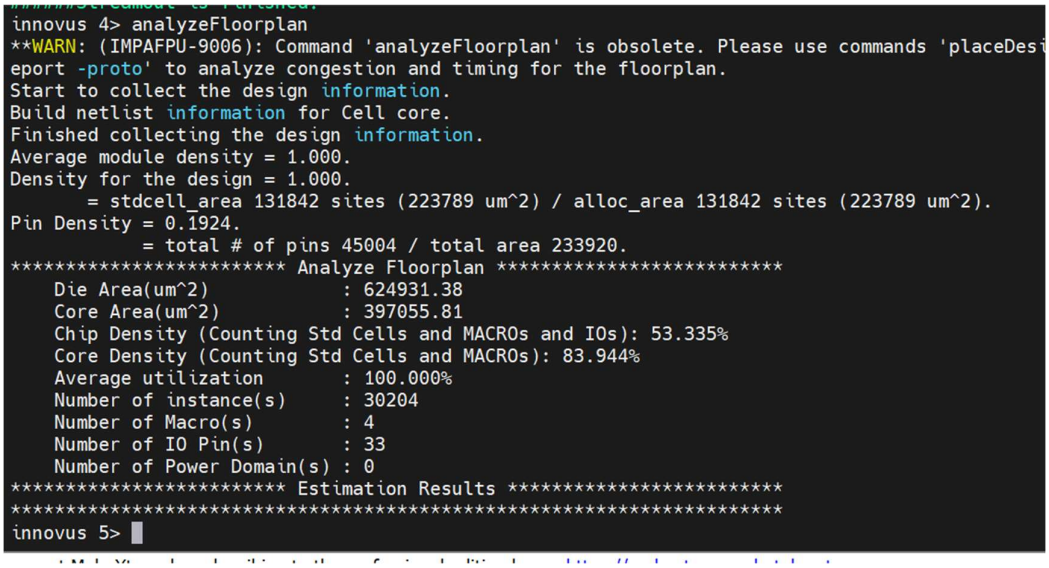
Path type 是從 register 到 register

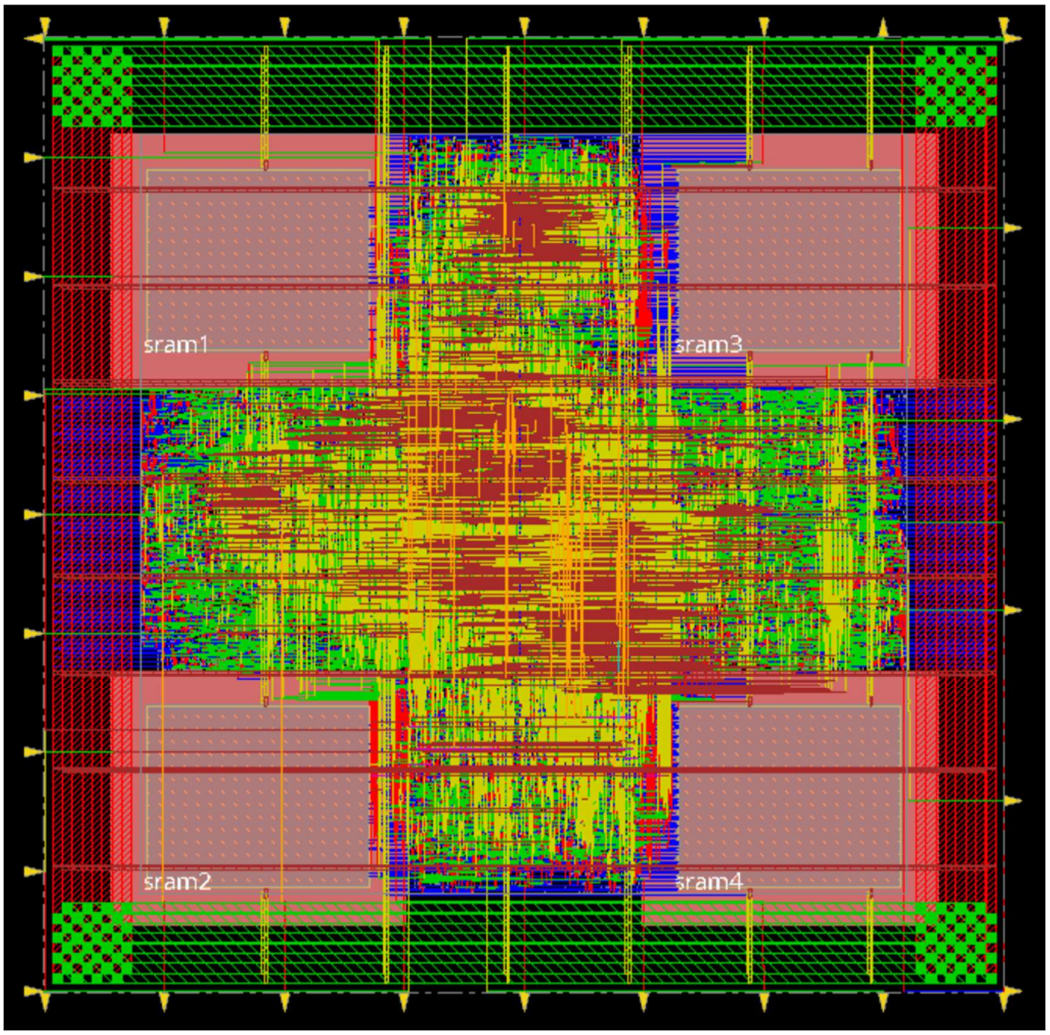
5. Attach the snapshot of GDS stream out messages. (10%)



6. Attach the snapshot of the final area result. (5%)



7. Attach the snapshot of your final layout **after adding core filler**. (Remember to switch to **Physical view** and make Pin Shapes visible) (10%)



8. What is your strategy for floorplanning (especially for placing the SRAMs)? What is the reason behind it? (10%)

   我在做 sram 的 floorplanning 的時候主要是用 innovus 的 automatic floorplan 的功能。不過依照原理，sram 是越靠近四個邊角越好，因為這樣一來才不會阻擋的 routing 的時候，wire 需要繞過許多障礙才連接到要連接的目的地。再來就是，為了避免 ir drop，以及 sram 對於電壓較敏感等等原因，像 sram 等 hard macro 也要盡量靠近 vdd 等電源。因此我們將 sram 盡量靠近四個邊角。 但要值得注意的是，也要不要違反 drc, lvs 等等規定，在離 boundary 的距離上也要有所注意。