Integrated Circuit Design
Homework #3
Layout

Deadline: Nov. 8

Introduction

In homework 3, you are asked to layout a 4-bit full adder in ***Virtuoso*****,** an integrated editor provided by Cadence. For simplicity, the architecture of the adder will remain the same as in homework 2 and is shown in below pictures. Besides, you will have to verify the correctness of the layout with Virtuoso's built-in tools and evaluate its performance by post-layout simulation.

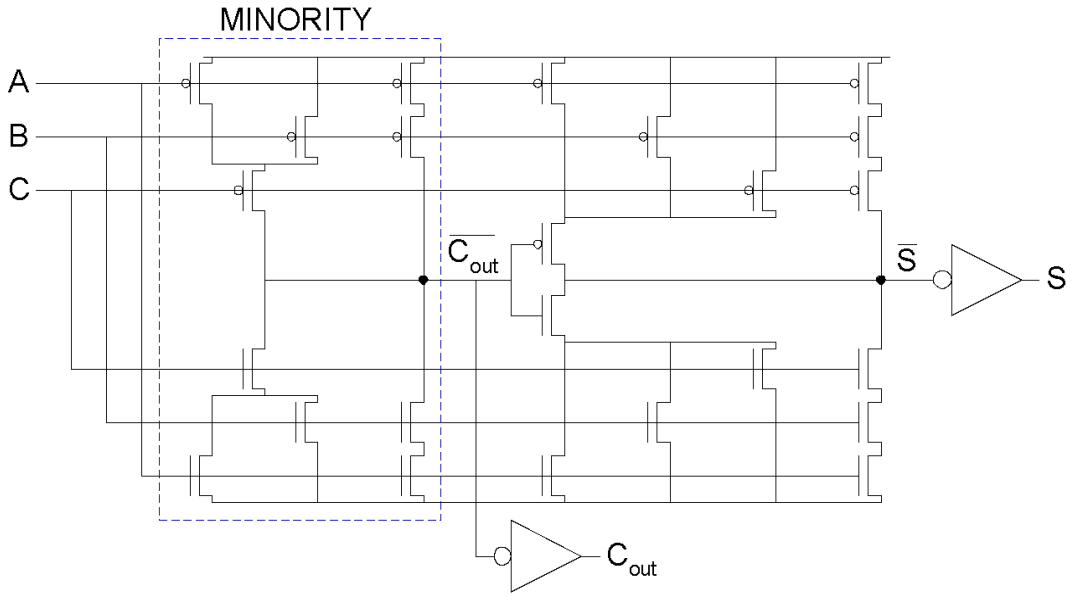


Fig. 1. Schematic of 1-bit full adder.

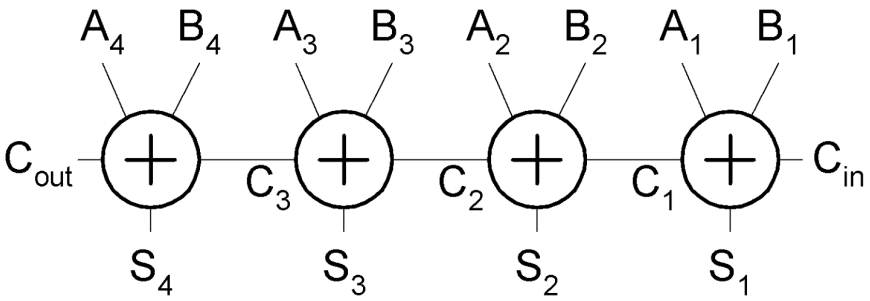


Fig. 2. Architecture of 4-bit adder

Submission

There are 7 files you should prepare before the submission. Put these files under a folder named <your_student_id>_hw3, then compress them to a zip file named <your_student_id>_hw3.zip. The following is an example of the file structure.

```
B01234567_hw3.zip
└──B01234567_hw3
      ├──presim.sp
      ├──postsim.sp
      ├──adder.sp
      ├──adder.pex.sp.adder.pxi
      ├──adder.pex.sp.pex
      ├──adder.pex.sp
      └──report.pdf
```

File	Note
presim.sp	SPICE program for pre-simulation
postsim.sp	SPICE program for post-simulation
adder.sp	netlist (.subckt) generated by *Composer* or handcraft
adder.pex.sp.adder.pxi	related file generated by *PEX*
adder.pex.sp.pex	related file generated by *PEX*
adder.pex.sp	netlist (.subckt) generated by *PEX*
report.pdf	your report

Schematic

Please define your netlist of 4-bit adder, obeying following rules,

- Except for the transistor naming and the sizing, the architecture of the adder is not adjustable.
- Your 4-bit adder should contain
  - 9 input pins: **A1~A4**, **B1~B4**, **Cin**
  - 5 output pins: **S1~S4, Cout**
  - 2 power pins: **VDD, GND**
- **A1**~**A4** should connect to pin **A** of corresponding 1-bit full adder, while **B1**~**B4** should connect to pin **B**. Please do not swap the connection, otherwise you might fail the demo.
- **DO NOT** connect pin **C** of LSB to ground in schematic directly.
- All PMOS body should be **VDD.**
- All NMOS body should be **GND.**

Layout

Please refer to the tutorial and layout a 4-bit adder. The layout should follow the following rules,

- No **DRC** violation.
- No **LVS** warning or error compared to your schematic.
- **PO_TEXT** layer is prohibited to use, you should put the label of above ports (**A1**~**A4**, **B1**~**B4**, **Cin**, **Cout**, **VDD**, and **GND**) on **ME1_TEXT** or above.
- You can adjust the height of layout or use any layers of metal as you want, though there are restrictions in real-world standard cell libraries.
- **DO NOT** use material layers (ME1, ME2…) for labels. Instead, use **ME1_TEXT**, **ME2_TEXT**… The tools could fail to find your labeled ports while running LVS.
- It is prohibited to use any predefined cells from the libraries. Otherwise, you'll get 0 points at the layout part.

Report

Complete the following tasks and questions in ***report.pdf.*** We only accept the **.pdf** format of report files. The report should contain

- [Netlist, 15%]
  - (5 pts) screenshot of *adder.sp*
  - (10 pts) screenshot of *adder.pex.sp*
- [Layout, 50%]
  - (10 pts) Screenshot of layout with measuring the area
  - (20 pts) Screenshot of successful DRC (with your account)
  - (20 pts) Screenshot of successful LVS (with your account)
- [Simulation, 30%] Simulate following pattern with setting the input rising time to 1ns. There are total 12 screenshots required in this part.

  *Output delay is defined as the time from last input signal transition to 50% to last output signal transition to 50%

  *You are allowed to keep only the latest input and output waveforms for output delay

  a. (10 pts) 0001+0001
     - waveform of **A1~A4**, **B1~B4**, **S1~S4** and **Cout** in pre-sim
     - waveform of **A1~A4**, **B1~B4**, **S1~S4** and **Cout** in post-sim
     - waveform of output delay in pre-sim
     - waveform of output delay in post-sim

  b. (10 pts) 1111+0001
     - waveform of **A1~A4**, **B1~B4**, **S1~S4** and **Cout** in pre-sim
     - waveform of **A1~A4**, **B1~B4**, **S1~S4** and **Cout** in post-sim
     - waveform of output delay in pre-sim
     - waveform of output delay in post-sim

  c. (10 pts) 0101+1010
     - waveform of **A1~A4**, **B1~B4**, **S1~S4** and **Cout** in pre-sim
     - waveform of **A1~A4**, **B1~B4**, **S1~S4** and **Cout** in post-sim
     - waveform of **output delay** in pre-sim
     - waveform of **output delay** in post-sim
- [Analysis, 5%] Compare the results of pre-sim and post-sim. What is the difference and what is the reason?

Note

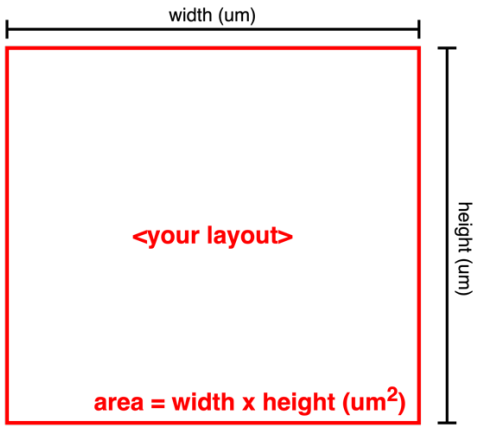
- Plagiarism is strictly prohibited. Otherwise, you will get 0 points in homework 3.
- 5 points are deducted if there is any naming error in your submission files.
- Please put your questions on NTU cool instead of sending emails.

Hint

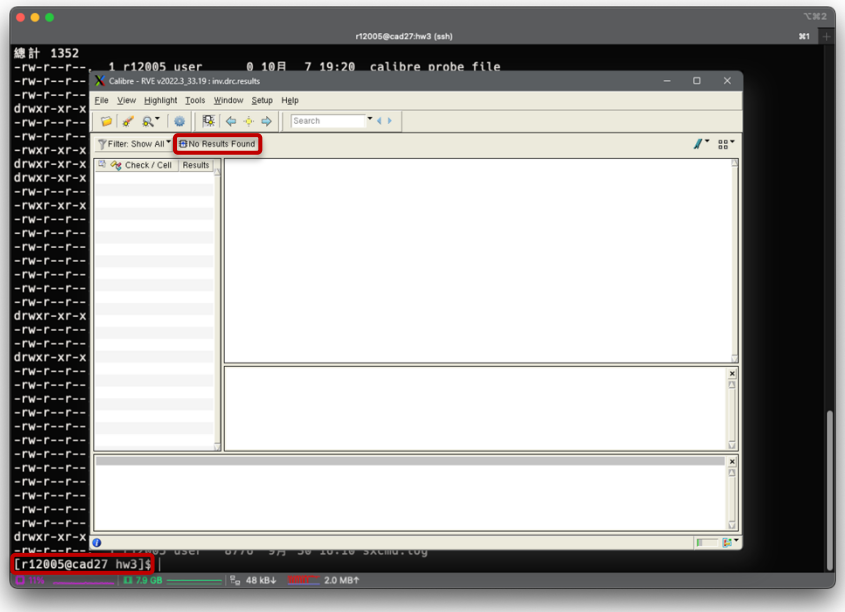
- It is recommended to use *Composer* to construct the netlist for easier debugging.
- If you find it hard to start the layout, you can run the DRC and LVS on 1-bit full adder and then stack it to 4 bits.

Appendix

- Layout with measuring the area



- Successful DRC



- Successful LVS