EX. NO: 11

DATE:

FOUR-BIT BINARY SUBTRACTOR

AIM:

To draw circuit to perform Subtractor using 1's Complement and 2's Complement

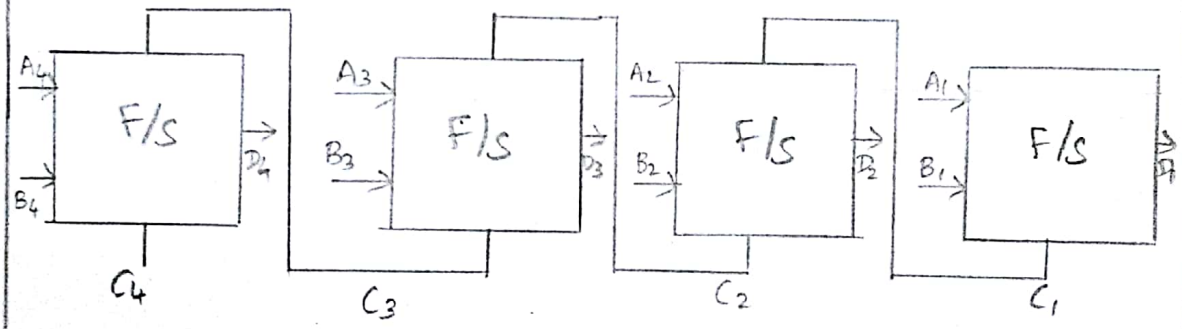
FORMULA:

$D = A - B$ (full subtractor)

$D = A + \overline{B}$ (1's Complement)

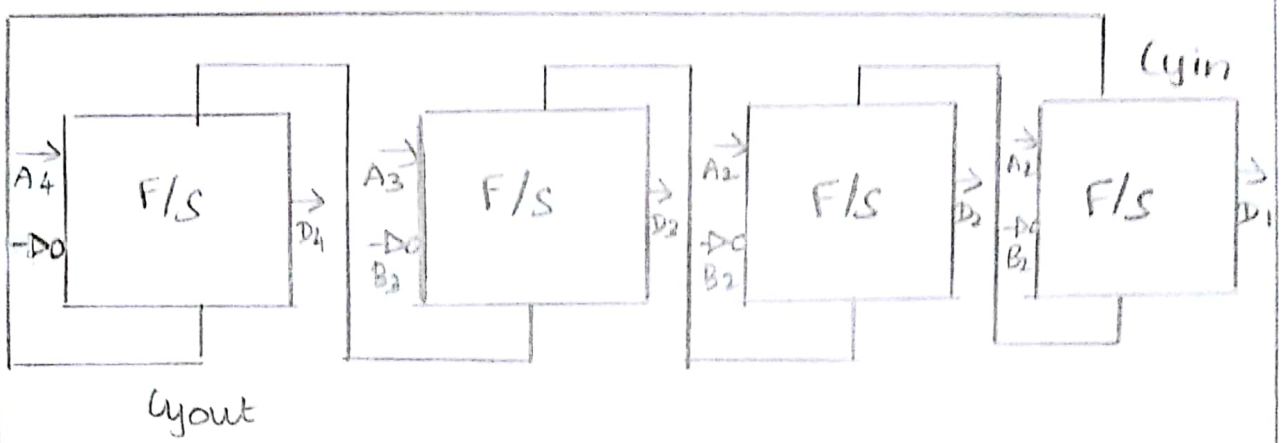
$D = A\left(\frac{1}{B} + 1\right)$ (2's Complement)

CIRCUIT DIAGRAM:



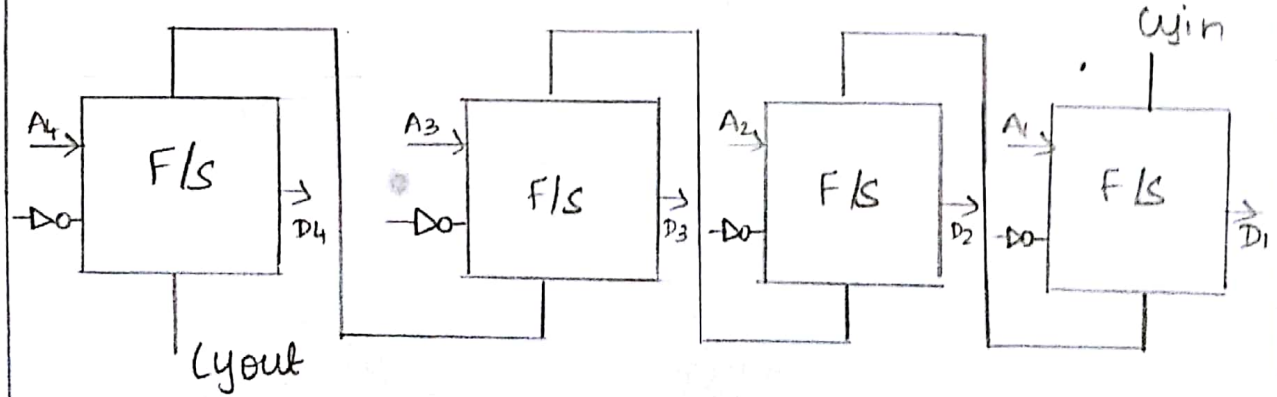
S No	A_4	A_3	A_2	A_1	B_4	B_3	B_2	B_1	C_4	D_4	D_3	D_2	D_1
1	1	1	0	1	1	0	1	0	0	0	0	1	1
2	1	1	1	1	0	1	1	1	0	1	0	0	0
3	1	0	0	0	0	0	1	1	0	0	1	0	1
4	0	0	1	1	1	0	0	1	1	1	0	1	0
5	1	1	1	0	0	0	1	0	0	1	1	0	0

4-bit Subtractor using 1's complement :



S.NO	A_4	A_3	A_2	A_1	B_4	B_3	B_2	B_1	Cy	D_4	D_3	D_2	D_1
1.	1	1	0	1	0	1	1	1		0	0	1	1	0
2.	0	1	1	1	0	0	0	1		0	0	1	1	0
3.	0	0	0	1	1	0	0	1		1	1	0	0	1
4.	1	0	1	0	0	0	0	1		0	1	0	0	1
5.	1	0	1	0	0	0	1	0		0	1	0	0	0

4-bit Subtractor using 2's Complement :



SNo	A_4	A_3	A_2	A_1	B_4	B_3	B_2	B_1	Cy	S_4	S_3	S_2	S_1
1	0	0	0	1	1	1	1	1	0	1	0	1	0
2	0	1	1	1	1	0	0	0	0	1	1	1	1
3	1	0	0	0	0	0	1	0	1	0	1	1	0
4	1	1	1	0	0	0	1	0	1	1	1	0	0
5	1	0	1	0	0	1	0	0	1	0	1	1	0

RESULT:

It has been verified.

Ex. No: 12 DATE:	DECIMAL ADDER

AIM:

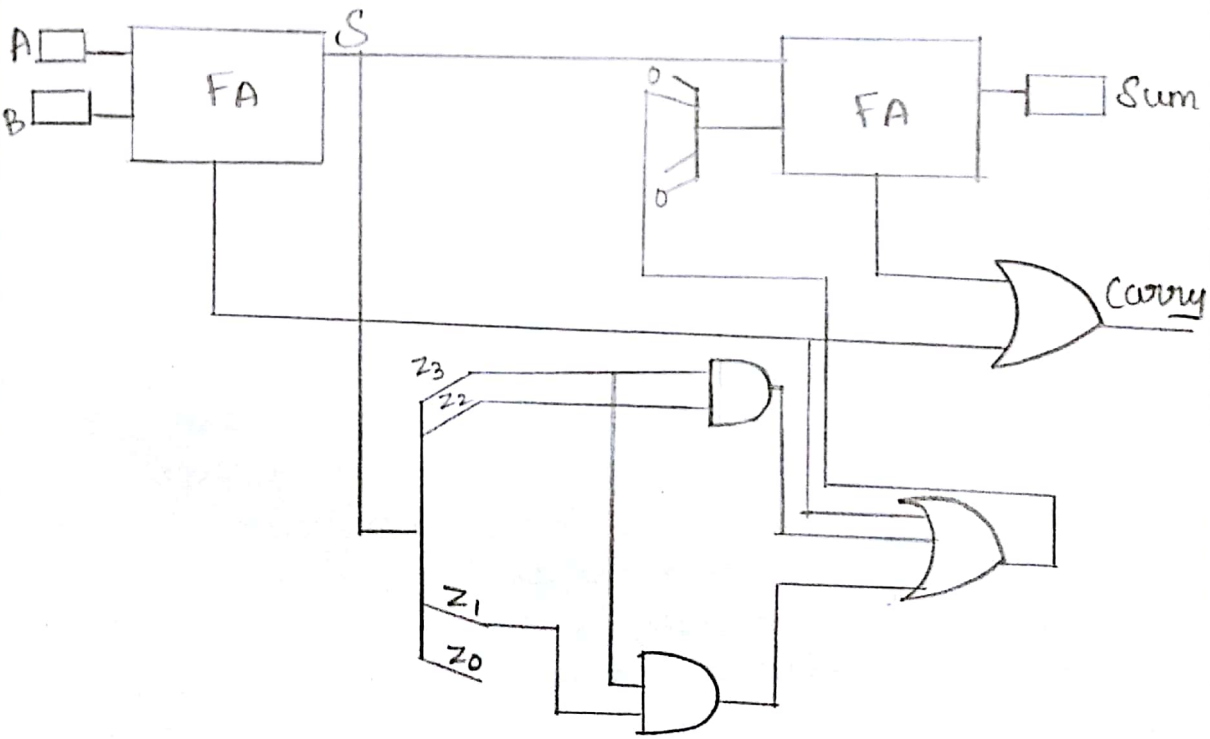
To implement to add BCD numbers.

FORMULA:

$T = A + B$

$S = T + 0110$ if $CY = 1$ or $T > 1001$

CIRCUIT DIAGRAM:



TRUTHTABLE:

S No	A_4	A_3	A_2	A_1	B_4	B_3	B_2	B_1	Cy	S_4	S_3	S_2	S_1
1	1	0	1	1	0	1	1	1	1	1	0	0	0
2	1	0	0	0	0	0	0	1	0	1	0	0	1
3	1	0	1	0	0	1	1	1	1	0	1	1	1
4	1	1	1	0	0	0	1	1	1	0	1	1	1
5	1	1	1	1	0	0	0	0	1	0	1	0	1

RESULT:

Thus Decimal adder has been Verified.

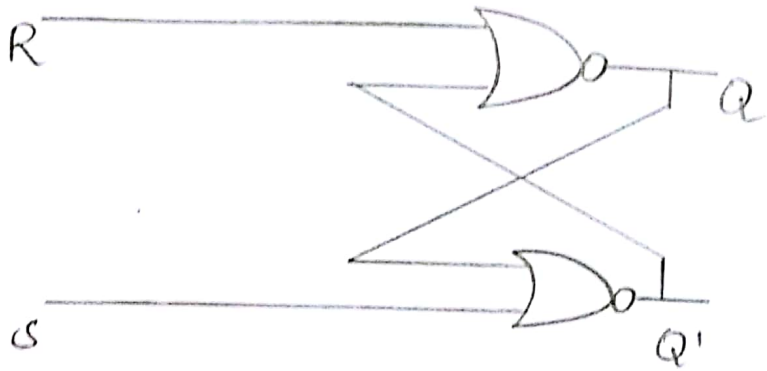
Ex No: 13 DATE:	FLIP-FLOPS

AIM:

To verify the truth table of SR, JK and D flip flop.

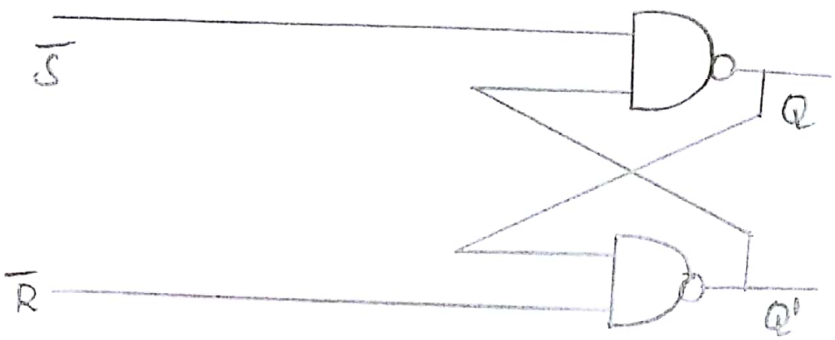
CIRCUIT DIAGRAM:

i) SR FLIPFLOP USING NOR :



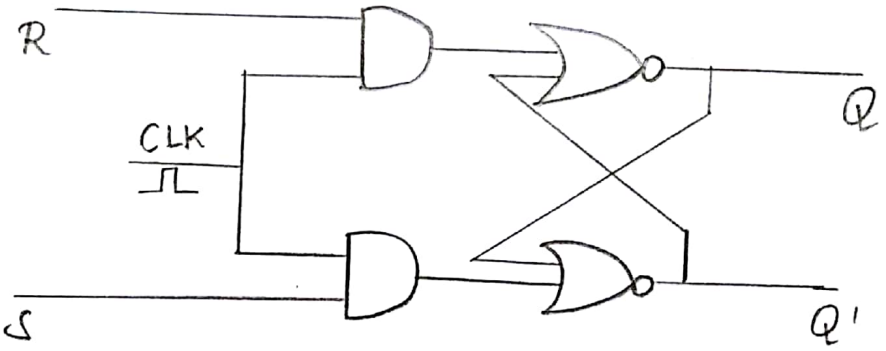
S	R	Q	Q'	Operator
0	0	0	1	Reset
0	0	0	1	Nochange
1	0	1	0	Set
0	0	1	0	Nochange
1	1	0	0	Nochange

ii.) SR FLIP FLOP USING NAND



$\overline{S}$	$\overline{R}$	Q	Q'	Operators
0	1	1	0	Set
1	1	1	0	Nochange
1	0	0	1	Reset
1	1	0	1	Nochange
0	0	1	1	Indeterminant

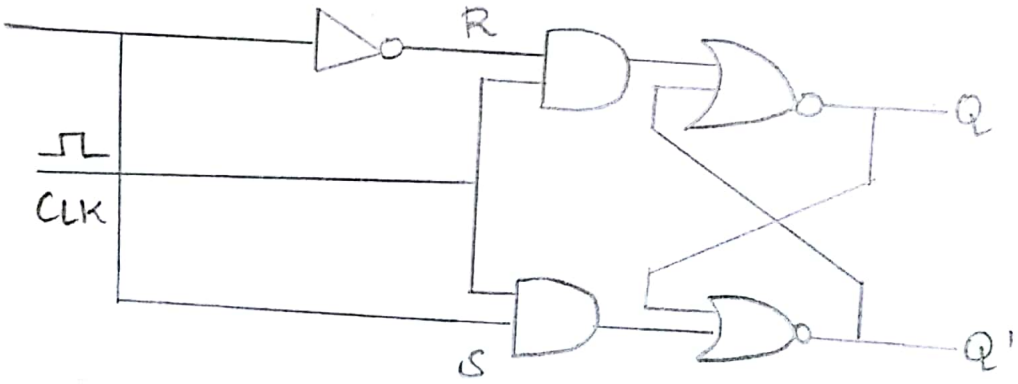
iii.) CLOCKED RS FLIP FLOP:



CLK	R	S	Q	Operators
⎍	1	0	0	Reset
⎍	0	0	0	Nochange
⎍	0	1	1	Set
⎍	0	0	1	Nochange
⎍	1	1	X	Indeterminant

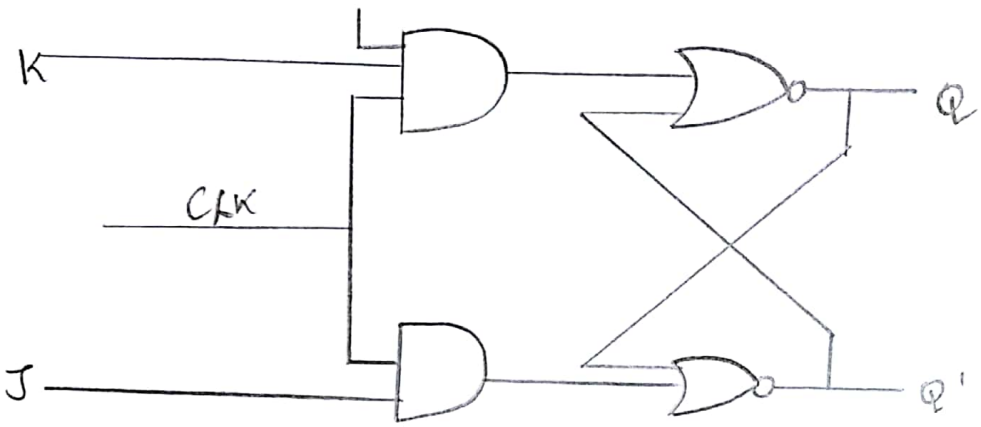
alt	R	S	Q(++1)	Operators
0	0	0	0	No change
0	0	1	1	Set
0	1	0	0	Reset
0	1	1	X	Indeterminant
1	0	0	1	No change
1	0	1	1	Set
1	1	0	0	Reset
1	1	1	X	Indeterminant

D - FLIP FLOP :



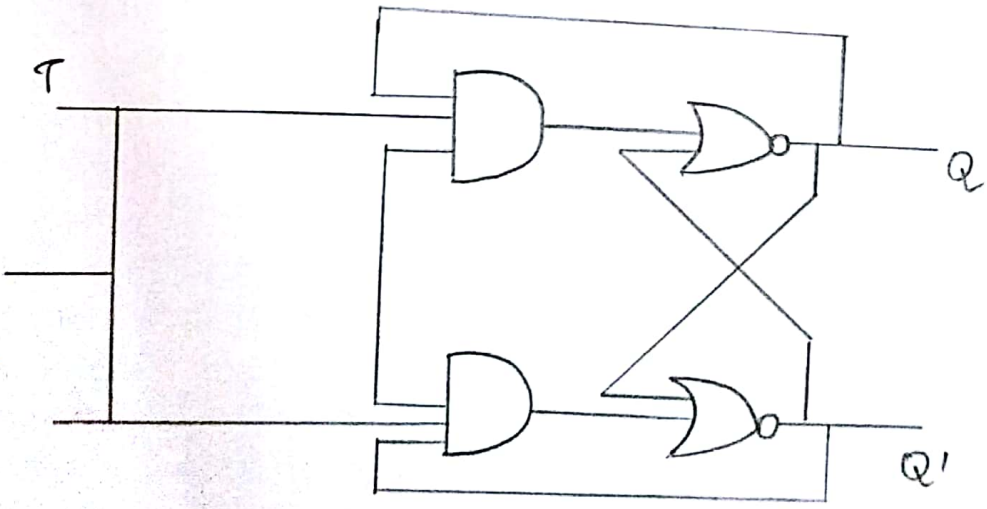
D	S	R	Q	Operator
0	0	1	0	Reset
1	1	0	1	Set

JK- FLIP FLOP:



Q(t)	J	K	Q (t+1)
0	0	0	0
0	0	1	0
0	1	0	1
0	1	1	1
1	0	0	1
1	0	1	0
1	1	0	1
1	1	1	0

T- FLIP FLOP:



Q(t)	t	Q(t+1)
0	0	0
0	1	1
1	0	1
1	1	0

RESULT:

Thus the truth table of SR, D, JK and T- flipFlop are verified successfully.

EX.NO: 11

DATE:

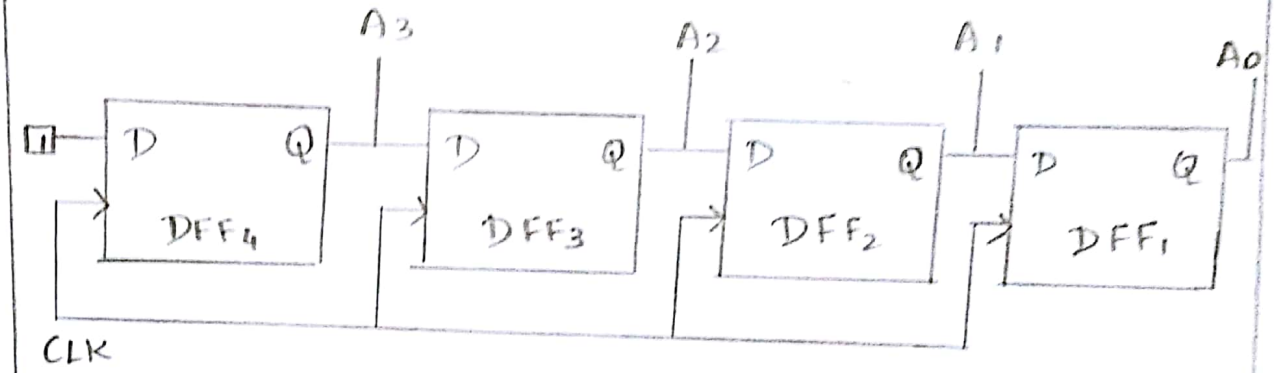
SHIFT REGISTER

AIM:

To implement left and right register using D-Flipflop.

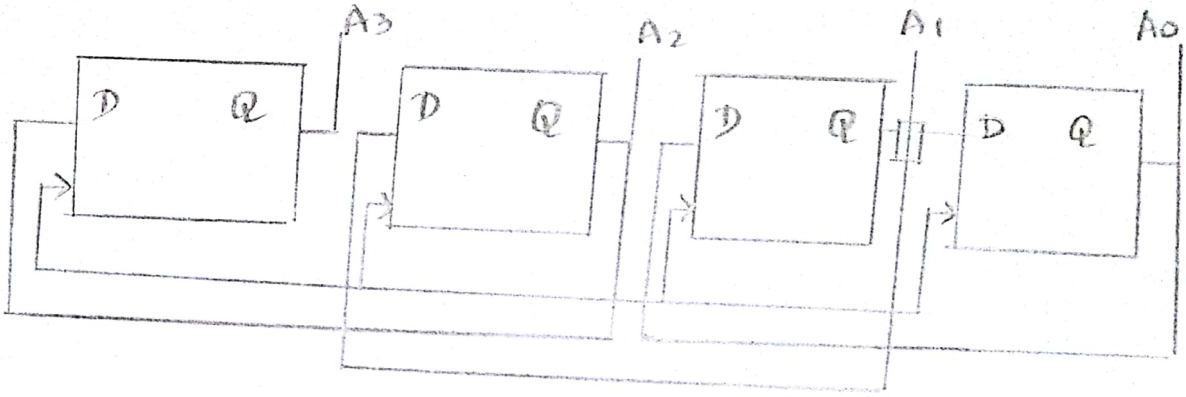
CIRCUIT DIAGRAM:

4-bit Right Shift Key:



CLK	D	A3	A2	A1	A0	Lost Bit
1	1	1	0	0	0	0
2	0	0	1	0	0	0
3	1	1	0	1	0	0
4	1	1	1	0	1	0
5	0	0	1	1	0	1
6	0	0	0	1	1	0
7	0	0	0	0	1	1
8	0	0	0	0	0	1

4-bit left shift key:



Clk	D	A_3	A_2	A_1	A_0	Lost Bit
1	1	0	0	0	1	0
2	1	0	0	1	1	0
3	0	0	1	1	0	0
4	1	1	1	0	1	0
5	0	1	0	1	0	1
6	0	0	1	0	0	1
7	0	1	0	0	0	0
8	0	0	0	0	0	1

RESULT:

Thus the 4-bit value is shifted in right, left directions using D-flip flop.

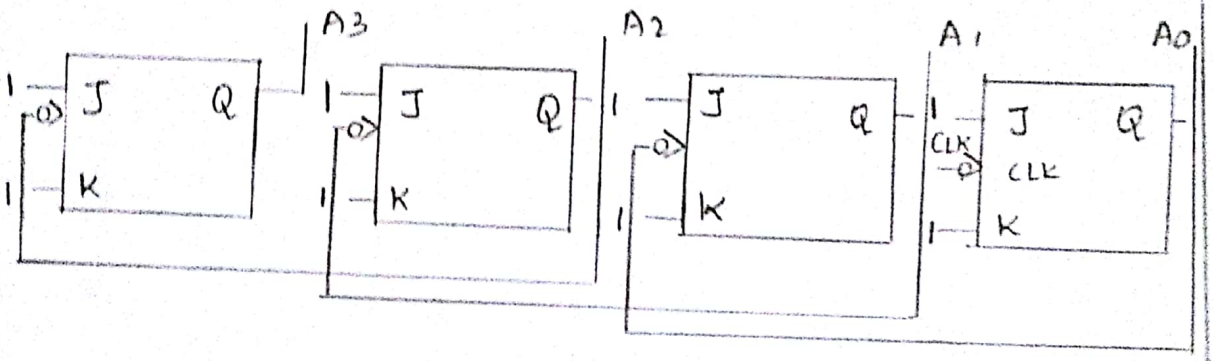
Ex No: 15 DATE:	COUNTERS

AIM:

To implement 4-bit counters using JK flipflop.

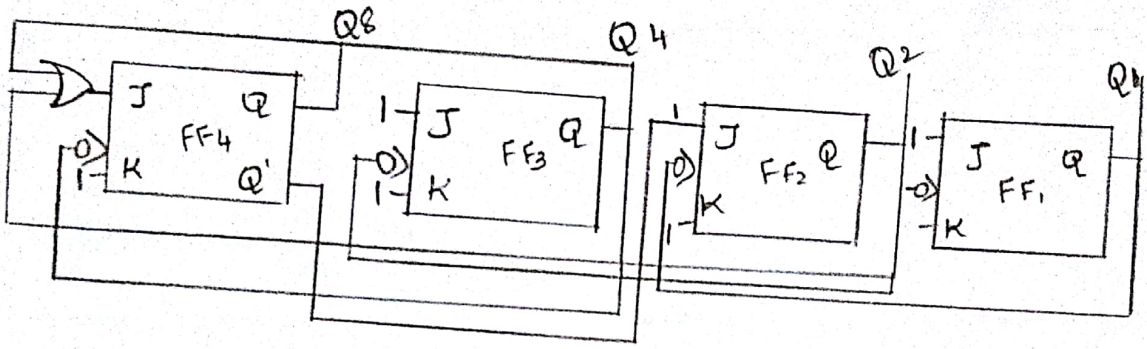
CIRCUIT DIAGRAM:

4-Bit Asynchronous / Ripple up counters



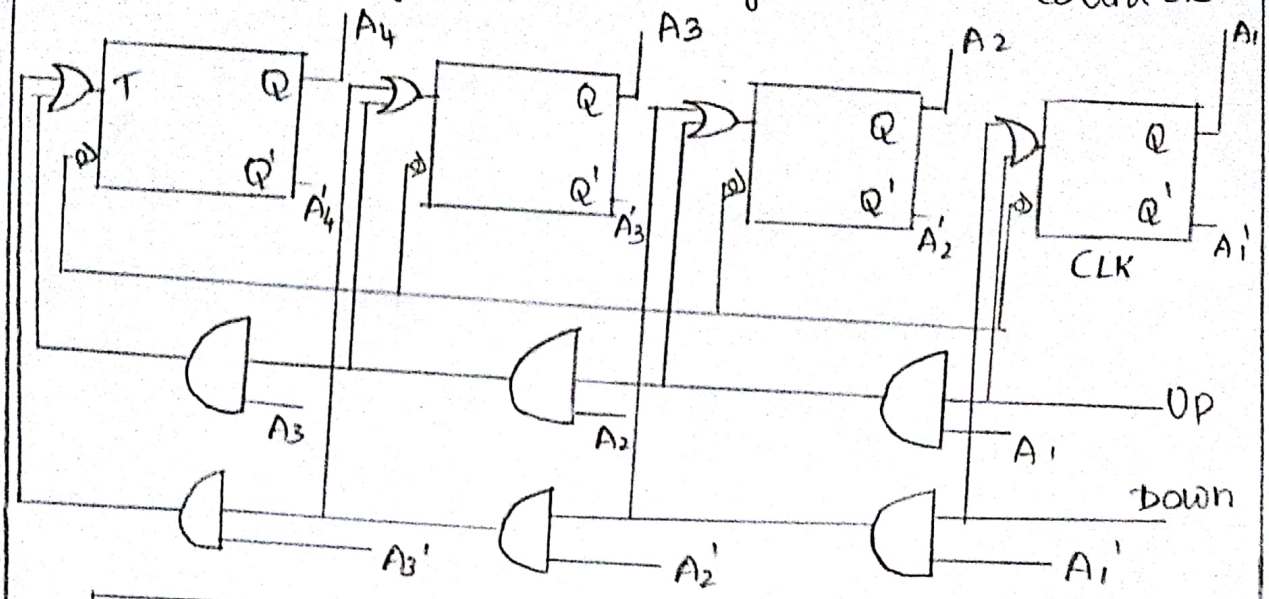
CLK	A_3	A_2	A_1	A_0
X	0	0	0	0
1	0	0	0	1
2	0	0	1	0
3	0	0	1	1
4	0	1	0	0
5	0	1	0	1
6	0	1	1	0
7	0	1	1	1
8	1	0	0	0
9	1	0	0	1
10	1	0	1	0
11	1	0	1	1
12	1	1	0	0
13	1	1	0	1
14	1	1	1	0
15	1	1	1	1
16	0	0	0	0

BCD Ripple counters:



CLK	Q_8	Q_4	Q_2	Q_1
0	0	0	0	0
1	0	0	0	1
2	0	0	1	0
3	0	0	1	1
4	0	1	0	0
5	0	1	0	1
6	0	1	1	0
7	0	1	1	1
8	1	0	0	0
9	1	0	0	1
10	1	0	1	0
11	1	0	1	1
12	1	1	0	0
13	1	1	0	1
14	1	1	1	0
15	1	1	1	1

4-Bit Binary up / Down Synchronous Counters:



DOWN	CLK	A_4	A_3	A_2	A_1
1	0	0	0	0	0
1	1	0	0	0	1
1	2	0	0	1	0
1	3	0	0	1	1
1	4	0	1	0	0
1	5	0	1	0	1
1	6	0	1	1	0
1	7	0	1	1	1
1	8	1	0	0	0
1	9	1	0	0	1
1	10	1	0	1	0
1	11	1	0	1	1
1	12	1	1	0	0
1	13	1	1	0	1
1	14	1	1	1	0
1	15	1	1	1	1

RESULT:

Using ripple and synchronous Countered Binary value are Countered using BCD countered BCD values incremented.