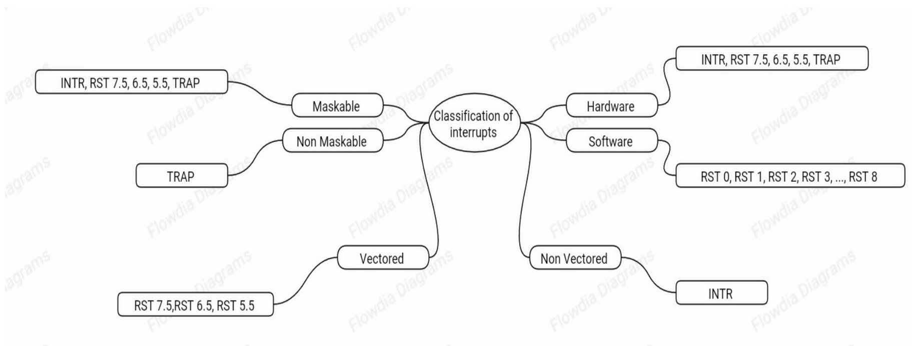
UNIT 5

Interrupts in 8085 microprocessor

When microprocessor receives any interrupt signal from peripheral(s) which are requesting its services, it stops its current execution and program control is transferred to a sub-routine by generating CALL signal and after executing sub-routine by generating RET signal again program control is transferred to main program from where it had stopped.

When microprocessor receives interrupt signals, it sends an acknowledgement (INTA) to the peripheral which is requesting for its service.



Interrupts can be classified into various categories based on different parameters:

<u>Hardware and Software Interrupts</u>

- When microprocessors receive interrupt signals through pins (hardware) of microprocessor, they are known as Hardware Interrupts. There are 5 Hardware Interrupts in 8085 microprocessor. They are – INTR, RST 7.5, RST 6.5, RST 5.5, TRAP

- Software Interrupts are those which are inserted in between the program which means these are mnemonics of microprocessor. There are 8 software interrupts in 8085 microprocessor. They are – RST 0, RST 1, RST 2, RST 3, RST 4, RST 5, RST 6, RST 7.

<u>Vectored and Non-Vectored Interrupts</u>

- Vectored Interrupts are those which have fixed vector address (starting address of sub-routine) and after executing these, program control is transferred to that address.

- Non-Vectored Interrupts are those in which vector address is not predefined. The interrupting device gives the address of sub-routine for these interrupts. INTR is the only non-vectored interrupt in 8085 microprocessor.

Maskable and Non-Maskable Interrupts

- Maskable Interrupts are those which can be disabled or ignored by the microprocessor. These interrupts are either edge-triggered or level-triggered, so they can be disabled. INTR, RST 7.5, RST 6.5, RST 5.5 are maskable interrupts in 8085 microprocessor.

- Non-Maskable Interrupts are those which cannot be disabled or ignored by microprocessor. TRAP is a non-maskable interrupt. It consists of both level as well as edge triggering and is used in critical power failure conditions.

TRAP interrupt

It is the only non maskable interrupt which cannot be needed to enabled as it cannot be disabled. It has the highest priority among all the interrupts. *It is edge and level sensitive it needed to be hight and stay high when recognised.* Once recognized, it cannot be recognized again until it goes low and high again.Trap is used for power failure and emergency sutoff.

Priority of Interrupts –

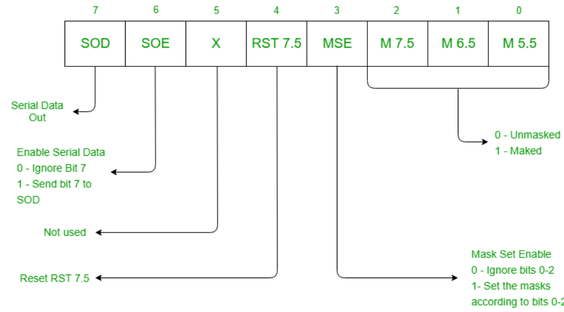
When microprocessor receives multiple interrupt requests simultaneously, it will execute the interrupt service request (ISR) according to the priority of the interrupts.

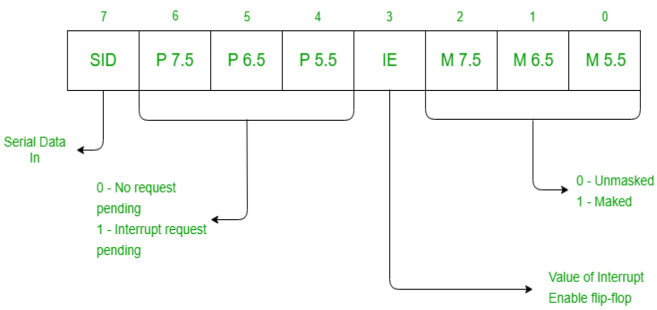
Instruction for Interrupts –

Enable Interrupt (EI) – The interrupt enable flip-flop is set and all interrupts are enabled following the execution of next instruction followed by EI. No flags are affected. After a system reset, the interrupt enable flip-flop is reset, thus disabling the interrupts. This instruction is necessary to enable the interrupts again (except TRAP).

Disable Interrupt (DI) – This instruction is used to reset the value of enable flip-flop hence disabling all the interrupts. No flags are affected by this instruction.

Set Interrupt Mask (SIM) – It is used to implement the hardware interrupts (RST 7.5, RST 6.5, RST 5.5) by setting various bits to form masks or generate output data via the Serial Output Data (SOD) line. First the required value is loaded in accumulator then SIM will take the bit pattern from it.





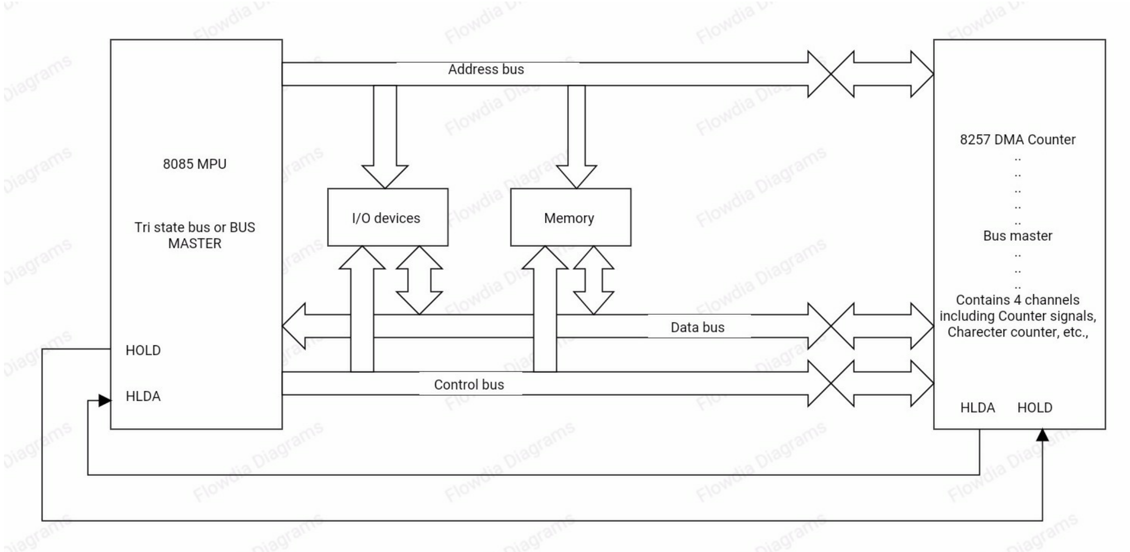
Read Interrupt Mask (RIM) – This instruction is used to read the status of the hardware interrupts (RST 7.5, RST 6.5, RST 5.5) by loading into the A register a byte which defines the condition of the mask bits for the interrupts. It also reads the condition of SID (Serial Input Data) bit on the microprocessor.

Direct Memory Access (DMA)

The Direct Memory access is the process of communication or data transfer controlled by an peripheral. The microprocessor something become slow in control of data transfer, In such situation DMA is used.

The 8085 microprocessor has 2 important signals for DMA. They are HOLD and HLDA (Hold acknowledgement).

- ★ HOLD – This is an active high input signal to the 8085 from other master memory questioning the use of the address and data buses. After receiving the HOLD request, the MPU relinquishes the buses in the following machine cycle. All buses are tri-states and a Hold acknowledge signal is sent out. The MPU regains the control buses after HOLD goes low
- ★ HLDA –Hold acknowledge is an active high output signal indication that the MPU is relinguishing the control of the buses.



FUNCTIONS:

1. The external DMA controller sends the high signal to the hold signal.
2. The processor completes the machine cycle, floats the address, data and control lines and sends the hold acknowledgement signal to the controller.
3. DMA takes the control of the buses and transfers the data from the source to destination.
4. At the end of the data transfer, the DMA controller sends the low signal to the processor and finally, the processor regains the control of the buses.