1. Operating systems and compilers are called application software.
F 5p

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2. If Computer A runs a program in 4 s and Computer B run the same program in 6 s, Computer B is therefore 1.5 times as fast as Computer A.
F 5p

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3. Assume the following register contents:

X9 = 0x1907ABCDEF865432
X10 = 0x1234567812345678
1907ABCDEF865432000

what is the value of X12 for the following sequence of instructions?

```
LSL    X11, X9, #3
AND    X12, X10, X11
```

0x34566810300010 5p

---

4. For the following statement, write the corresponding assembly code.

$k = i + (j \text{ OR } k)$

Assume that variables *i*, *j* and *k* have already been placed in registers X0, X1 and X10 respectively.

```
ORR    X11, X1, X10      5p
ADD    X10, X11, X0      5p
```

---

5. Write down the binary representation of the decimal number -189.4 assuming the IEEE 754 single precision format. Show your calculations.

1 10000110 01111010110011001100110 10p

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6. Consider a computer running a program that requires 400 s, with 150 s spent executing floating-point (FP) instructions, 140 s spent executing Load/Store (L/S) instructions, 70 s spent executing integer (INT) and 40 s spent executing branch instructions. By how much is the total time reduced if the time for FP operations is reduced by 40%?

15 % 5p

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7. Consider the following instruction mix:

R-type	I-Type	LDUR	STUR	CBZ	B
25%	30%	20%	10%	13%	2%

What fraction of all instructions uses data memory and, all instructions uses instruction memory?

30%, 100% 5p

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8. There is no way to reduce compulsory misses.
F 5p

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9. Consider the fragment of LEGv8 assembly below and suppose the pipeline modified so that it has only one memory (that handles both instructions and data). In this case, there will be a structural hazard every time a program needs to fetch an instruction during the same cycle in which another instruction accesses data. Draw a pipeline diagram.

```
PL1:    ADD   X2, X1, X0          IF ID EX ME WB                          2p
        LDUR  X11, [X3, #8]          IF ID EX ME WB                       2p
        SUB   X9, X2, X0                IF ID EX ME WB                    2p
        CBZ   X9, Ruby                     ** ** IF ID EX ME WB           5p
        STUR  X11, [X3, #12]                        IF ID EX ME WB        2p
        SUB   X2, X10, X0                              IF ID EX ME WB     2p
Ruby:
```

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10. Calculate the mean time between failures and the availability for the device that has the following metrics:

Mean time to failure	Mean time to repair
2 Years	2 Day

732 days, 0.9973 5p

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11. For a data cache with a 3% miss rate and a 7-cycle hit latency, calculate the average memory access time. Assume that latency to memory and the cache miss penalty together is 100 cycles. Note: The cache must be accessed after memory returns the data.

10 cycles 5p

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12. Which of the following is not true?
Parallelism achieved by performing the same operation on independent data is called data-level parallelism. 5p

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13. Which of the following is true?
Memory hierarchy is a structure that uses multiple levels of memories; as the distance from the processor increases, the size of the memories and the access time both increase. 5p

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14. Suppose you want to achieve a speed-up of 80 times faster with 200 processors. What percentage of the original computation can be sequential?
0.75% 5p

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15. GPUs are highly multi-threaded.
T 5p

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16. A warehouse-scale computer (WSC) is a cluster comprised of tens of thousands of servers.
T 5p