F27CS
Introduction to Computer Systems
Class Test 2
ANSWERS

March 2017

1. In the following code, identify *all* instruction hazards and the registers involved

```
add $s1,$s3,$s4
sub $s2,$s6,$s5
add $s6,$s5,$s2
sub $s1,$s6,$s3
```

(4 marks)

Answer RAR s5 (s3 already beyond pipeline when read a second time, s6 has been written to in between the two reads)
RAW s2, s6
WAR s6
WAW none (s1 is already beyond the pipeline when the second instruction writing to it enters)

2. Assuming that each stage takes 1 cycle, calculate how long the above sequence of instructions takes. Show your working. (6 marks)

Answer

	Pipeline Stage					Scoreboard					
	Fetch	Decode	Read	Execute	Write	1	2	3	4	s	6
1	add s1,s3,s4	-	-	-	-	1	1		1	1	1
2	sub s2,s6,s5	add s1,s3,s4	-	-	-	1	1	1	1	1	1
3	add s6,s5,s2	sub s2,s6,s5	add s1,s3,s4	-	-	0	1	1	1	1	1
4	sub s1,s6,s3	add s6,s5,s2	sub s2,s6,s5	add s1,s3,s4	-	0	0	1	1	1	1
5	-	sub s1,s6,s3	add s6,s5,s2	sub s2,s6,s5	add s1,s3,s4	1	0	1	1	1	1
6	-	sub s1,s6,s3	add s6,s5,s2	bubble	sub s2,s6,s5	1	1	1	1	1	1
7	-	sub s1,s6,s3	add s6,s5,s2	bubble	bubble	1	1	1	1	1	0
8	-	-	sub s1,s6,s3	add s6,s5,s2	bubble	0	1	1	1	1	0
9	-	-	sub s1,s6,s3	bubble	add s6,s5,s2	0	1	1	1	1	1
10	-	-	sub s1,s6,s3	bubble	bubble	0	1	1	1	1	1
11	-	-	-	sub s1,s6,s3	bubble	0	1	1	1	1	1
12	-	-	-	-	sub s1,s6,s3	1	1	1	1	1	1

Scoreboard 1 represents availability of corresponding register value, at the *end* of the cycle. e.g. in cycle 4 register `$s1` was not available at the beginning of the cycle, but register `$s2` was originally available, but because the instruction now at the read stage stores into `$s2`, it is no longer availabe at the end of the stage. If any register is not available at the beginning of a read stage, then the instruction will stall until the corresponding register is written and the scoreboard is set to 1 again. Register `$s2` becomes available at the end of its writing stage, cycle 6, it becomes available, so the instruction at the read stage can execute its read in cycle 7.

3. Indicate two mechanisms for avoiding the structural hazard caused by branch instructions and comment on their advantages and disadvantages. (4 marks)

   Answer Branch prediction - advantage only need one set of registers disadvantage may have to back out and undo operations if wrong branch predicted
   Speculative execution - assume both branches taken - needs shadow registers and significant extra hardware - advantage no time lost

4. What are the advantages of memory mapped I/O? (2 marks)

   Answer No special instructions needed because device registers are mapped to memory locations. Protection of devices from unexpected commands is achieved by memory protection of the relevant address ranges.
   The alternative (not required as answer) uses special instructions to address devices on the bus, and these instructions are only available in supervisor state.

5. Outline the sequence of events that occur when a DMA transfer is initiated from a disk. (4 marks)

   Answer Command given to start I/O with appropriate arguments to identify the disk segment to read (or write) and the address of memory to read the segment into (or write from); OS moves to other processes; disk transfers data directly to memory; interrupt when transfer completes allows the process to return to the ready state
   Too many people saw disk, and went into the seeking of heads to the correct track, waiting for the correct sector, etc. What was wanted was the fact that the CPU was not involved, and only got told when the transfer was complete, using an interrupt

6. Assume that a fully associative cache has lines of 64 bytes long. Initially the cache is empty, and the following addresses are referenced in order. Identify the addresses that will cause cache misses. (all addresses are specified in decimal here)

   104, 812, 108, 1020, 112, 116, 120, 812, 124, 104, 816, 108, 1024, 112, 116, 120, 816, 124, 104, 820, 108, 1028, 112, 116, 120, 820, 124,

(Relevant multiples of 64 are 0, 64, 128, 192, 256, ..., 768. 832, 896, ..., 960, 1024, 1088, ...) (4 marks)

Answer 104 (bringing in 64-127)
812 (bringing in 768 to 831)
1020 (bringing in 960 to 1023)
1024 (brings in 1024 to 1088)

7. How does the logical view of memory as seen by the application programmer differ from the view seen by the system architect? (4 marks)

   Answer application programmer sees a single level of main memory
   system architect sees cache memory close to processor and hardware updating cache from main memory
   system architect also sees virtual memory on disk - requiring software support

8. What is the purpose of the Translation Lookaside Buffer (TLB)? (2 marks)

   Answer The TLB is a fully associate cache that stores the physical page address corresponding to recent virtual page addresses.