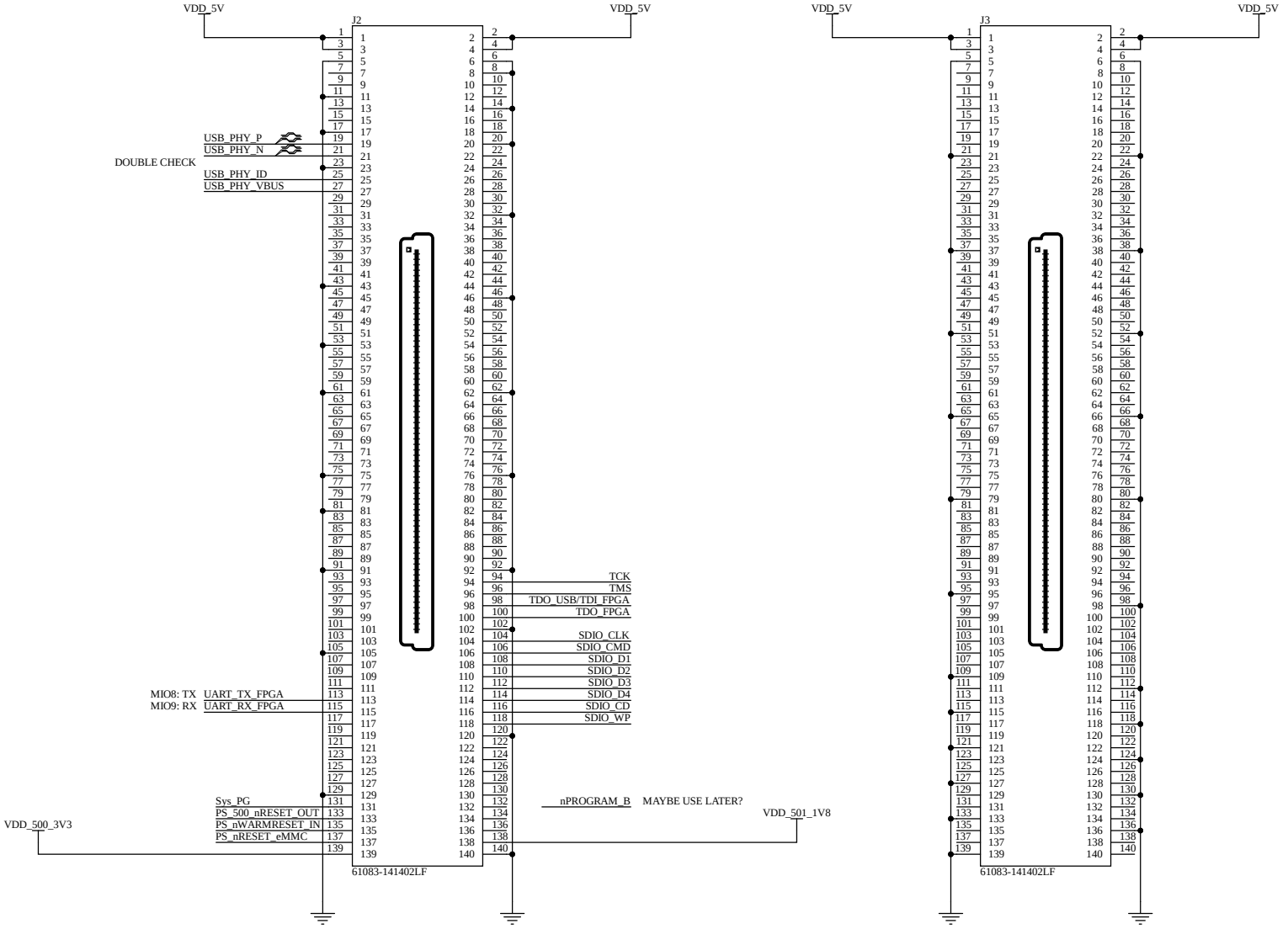
Mezzanine Board-to-Board Connectors between FPGA SOM and FPGA Development Board



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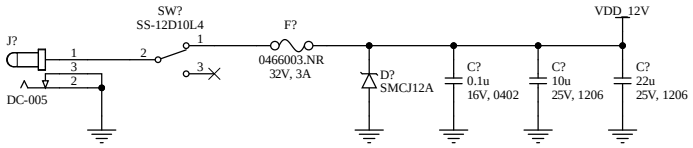
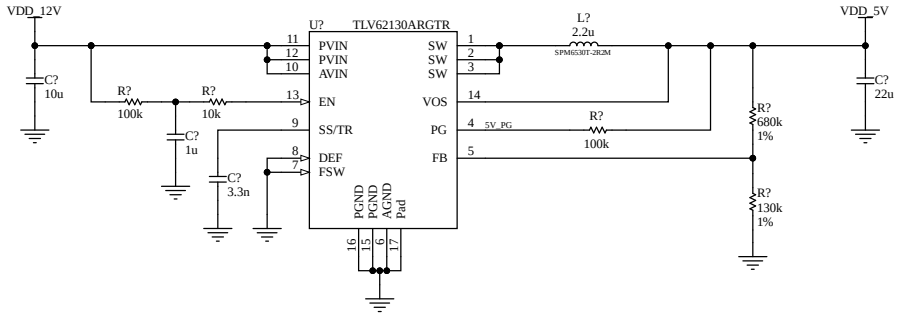
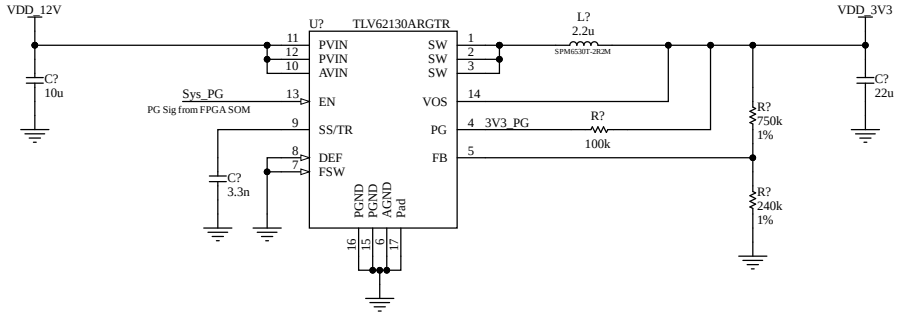
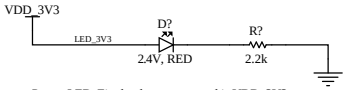
File: C:\Users\..\BTB Mezzanine.SchDoc		Drawn By:

Start-up Sequence: VDD_12V > VDD_5V > FPGA SOM > VDD_3V3









Power LED, Final voltage generated is VDD_3V3

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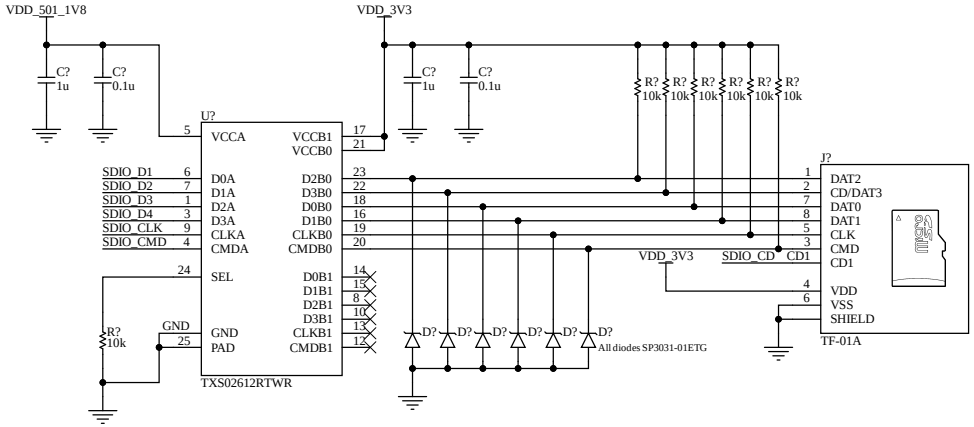
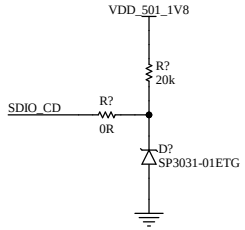
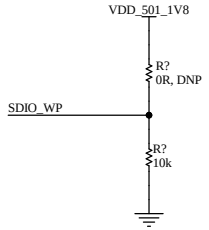
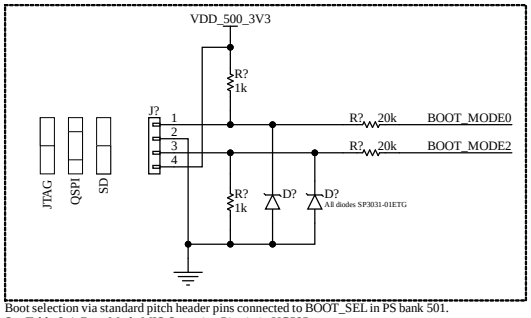
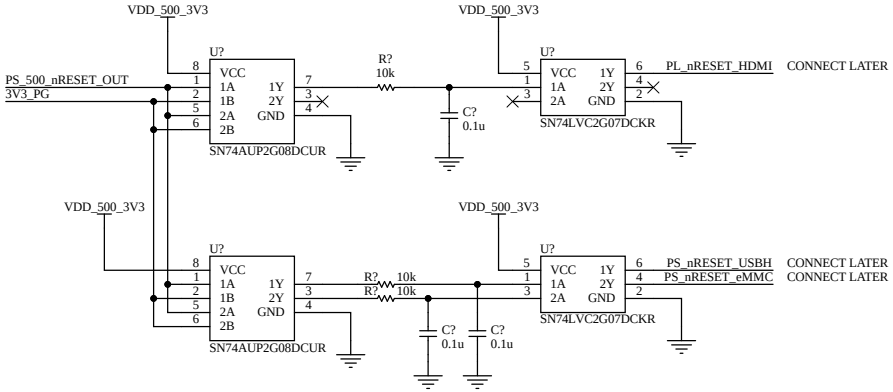


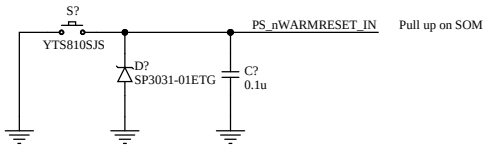






Boot selection via standard pitch header pins connected to BOOT_SEL in PS bank 501.
See Table 6-4: Boot Mode MIO Strapping Pins in in UG585.





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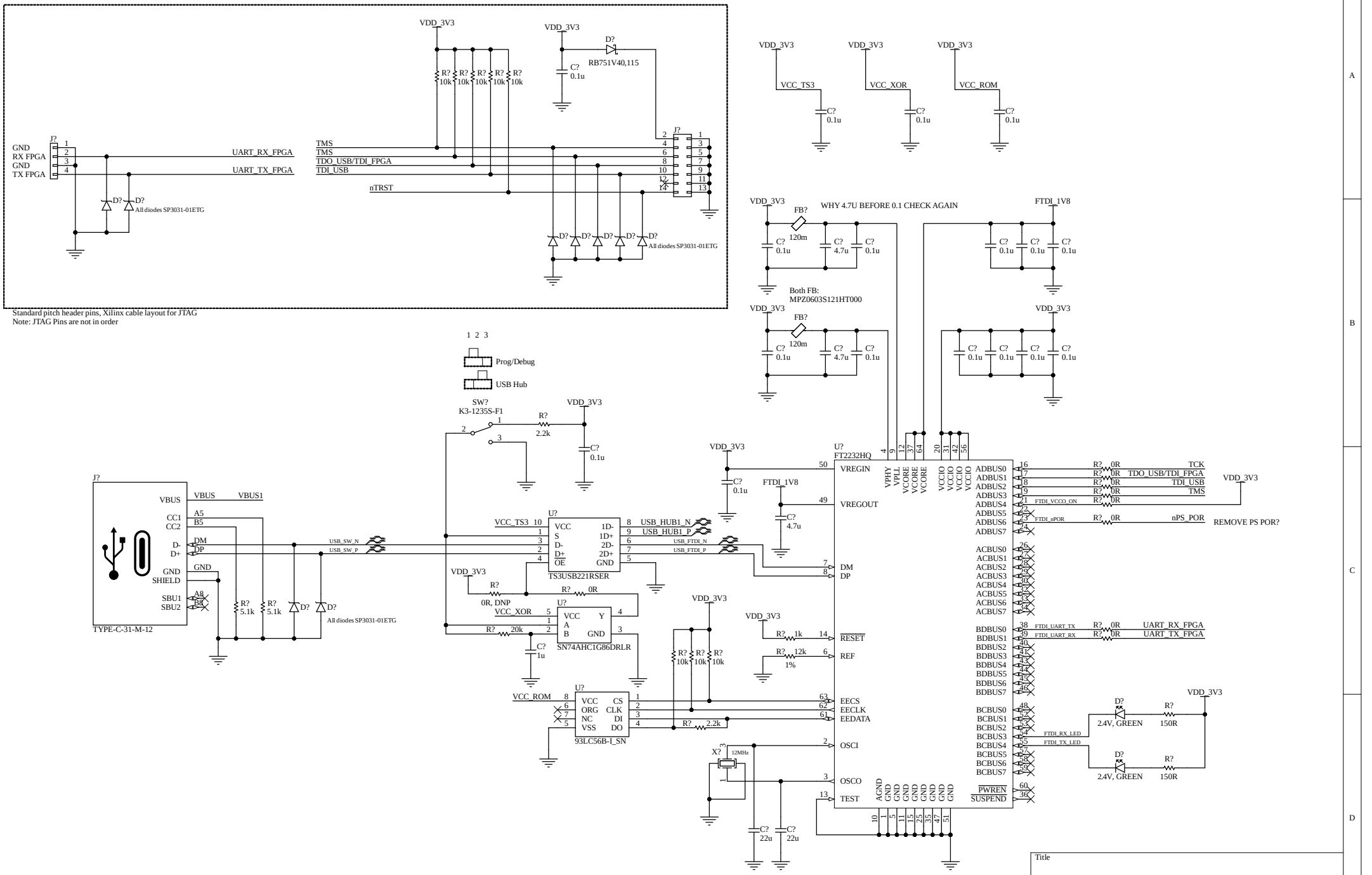
Standard pitch header pins, Xilinx cable layout for JTAG
Note: JTAG Pins are not in order
All diodes SP3031-01ETG
RB751V40,115
WHY 4.7U BEFORE 0.1 CHECK AGAIN
Both FB:
MPZ0603S121HT000
Prog/Debug
USB Hub
TYPE-C-31-M-12
TS3USB221RSER
SN74AHC1G86DRLR
93LC56B-I_SN
FT2232HQ
2.4V, GREEN
REMOVE PS POR?
Title
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Revision
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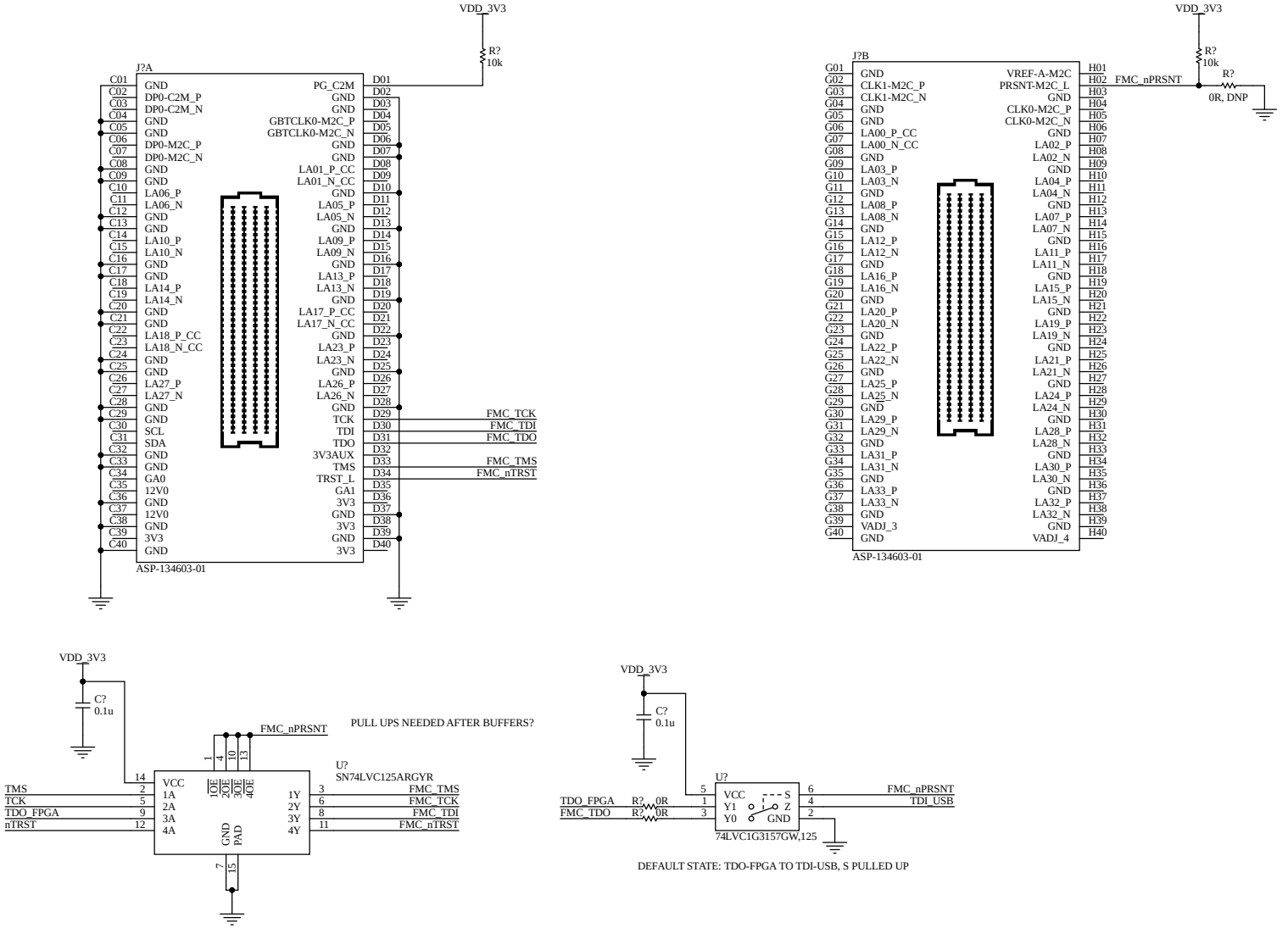

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Date: 4/27/2025		Sheet of
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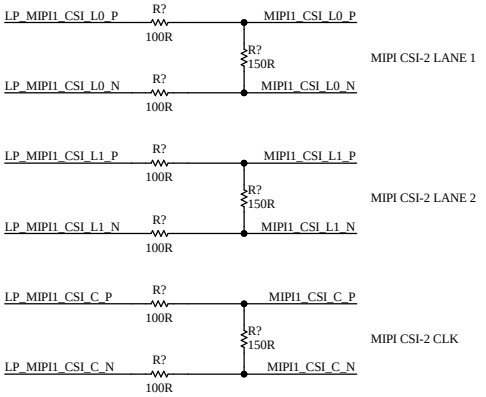
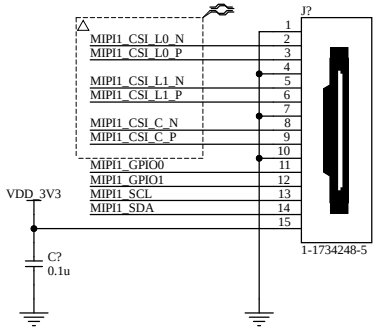
CONNECT TO FPGA

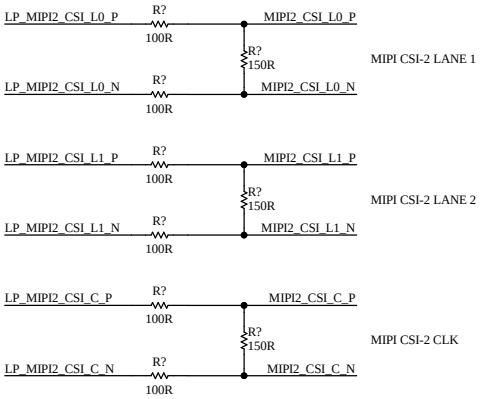


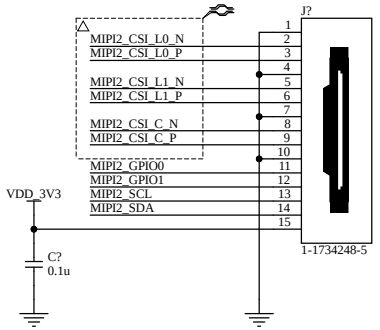


ALL RESISTORS 1%

Place all 150R resistors and 100R shunt resistors next to BTB Connectors

CONNECT TO FPGA





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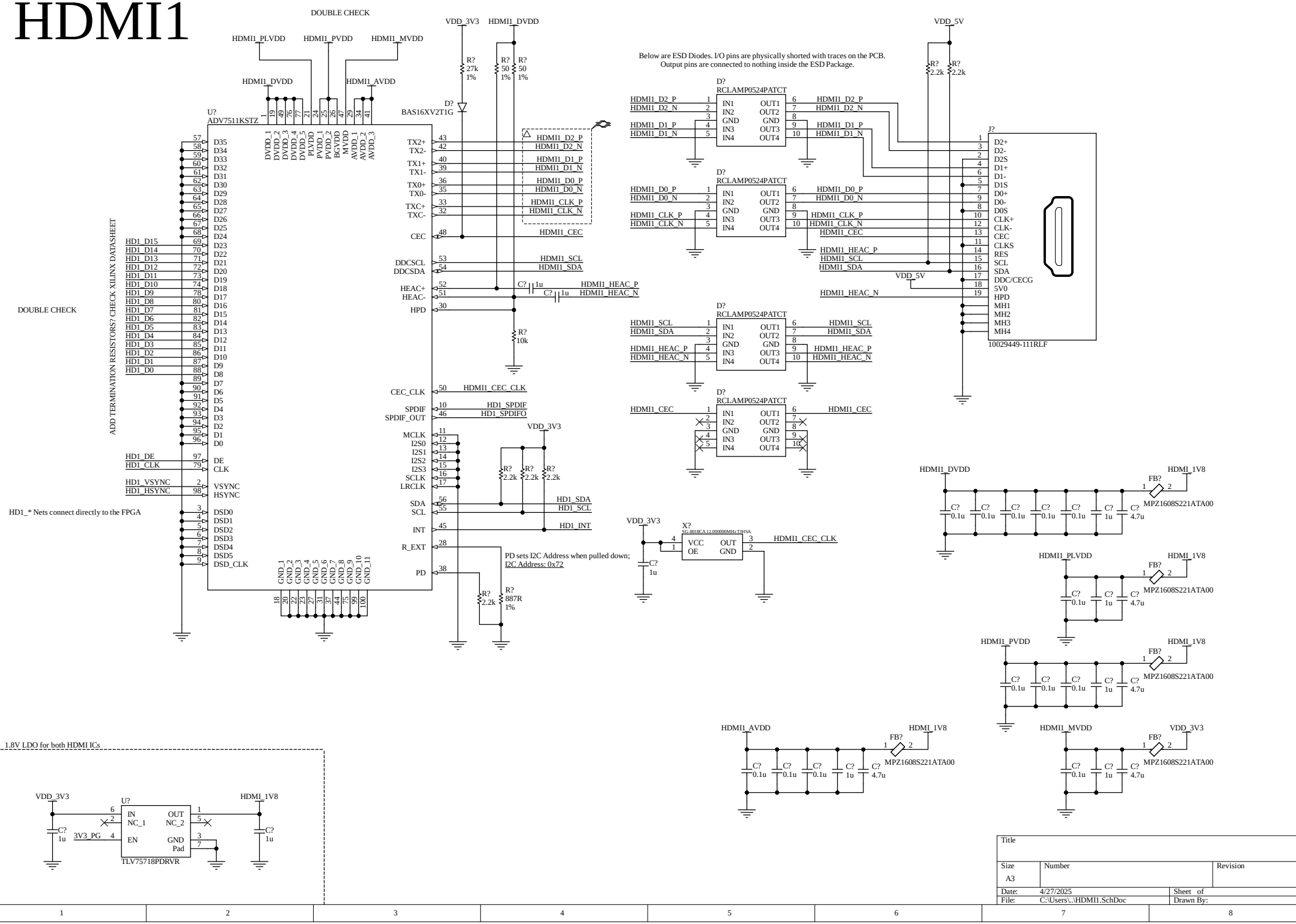
HDMI1


DOUBLE CHECK
HDMI1_PLVDD
HDMI1_PVDD
HDMI1_MVDD
HDMI1_DVDD
HDMI1_AVDD
VDD_3V3
HDMI1_DVDD
U?
ADV7511KSTZ
D?
BAS16XV2T1G
R? 27k 1%
R? 50 1%
R? 50 1%
DVDD_1
DVDD_2
DVDD_3
DVDD_4
DVDD_5
PLVDD
PVDD_1
PVDD_2
BGVDD
MVDD
AVDD_1
AVDD_2
AVDD_3
TX2+
TX2-
TX1+
TX1-
TX0+
TX0-
TXC+
TXC-
CEC
DDCSCL
DDCSDA
HEAC+
HEAC-
HPD
CEC_CLK
SPDIF
SPDIF_OUT
MCLK
I2S0
I2S1
I2S2
I2S3
SCLK
LRCLK
SDA
SCL
INT
R_EXT
PD
HDMI1_D2_P
HDMI1_D2_N
HDMI1_D1_P
HDMI1_D1_N
HDMI1_D0_P
HDMI1_D0_N
HDMI1_CLK_P
HDMI1_CLK_N
HDMI1_CEC
HDMI1_SCL
HDMI1_SDA
HDMI1_HEAC_P
HDMI1_HEAC_N
C? 1u
R? 10k
HDMI1_CEC_CLK
HD1_SPDIF
HD1_SPDIFO
HDMI1_INT
R? 2.2k
R? 887R 1%
PD sets I2C Address when pulled down;
I2C Address: 0x72
GND_1
GND_2
GND_3
GND_4
GND_5
GND_6
GND_7
GND_8
GND_9
GND_10
GND_11
DOUBLE CHECK
ADD TERMINATION RESISTORS? CHECK XILINX DATASHEET
HD1_D15
HD1_D14
HD1_D13
HD1_D12
HD1_D11
HD1_D10
HD1_D9
HD1_D8
HD1_D7
HD1_D6
HD1_D5
HD1_D4
HD1_D3
HD1_D2
HD1_D1
HD1_D0
HD1_DE
HD1_CLK
HD1_VSYNC
HD1_HSYNC
HD1_* Nets connect directly to the FPGA
Below are ESD Diodes. I/O pins are physically shorted with traces on the PCB.
Output pins are connected to nothing inside the ESD Package.
D?
RCLAMP0524PATCT
VDD_5V
R? 2.2k
J?
D2+
D2-
D2S
D1+
D1-
D1S
D0+
D0-
D0S
CLK+
CLK-
CEC
CLKS
RES
SCL
SDA
DDC/CECG
5V0
HPD
MH1
MH2
MH3
MH4
10029449-111RLF
X?
SG-8018CA 12.000000MHz TJHSA
VCC
OE
OUT
GND
HDMI1_CEC_CLK
HDMI_1V8
FB?
MPZ1608S221ATA00
C? 0.1u
C? 1u
C? 4.7u
HDMI1_PLVDD
HDMI1_PVDD
HDMI1_AVDD
HDMI1_MVDD
1.8V LDO for both HDMI ICs
U?
IN
OUT
NC_1
NC_2
EN
GND
Pad
3V3_PG
TLV75718PDRVR
Title
Size
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Number
Revision
Date: 4/27/2025
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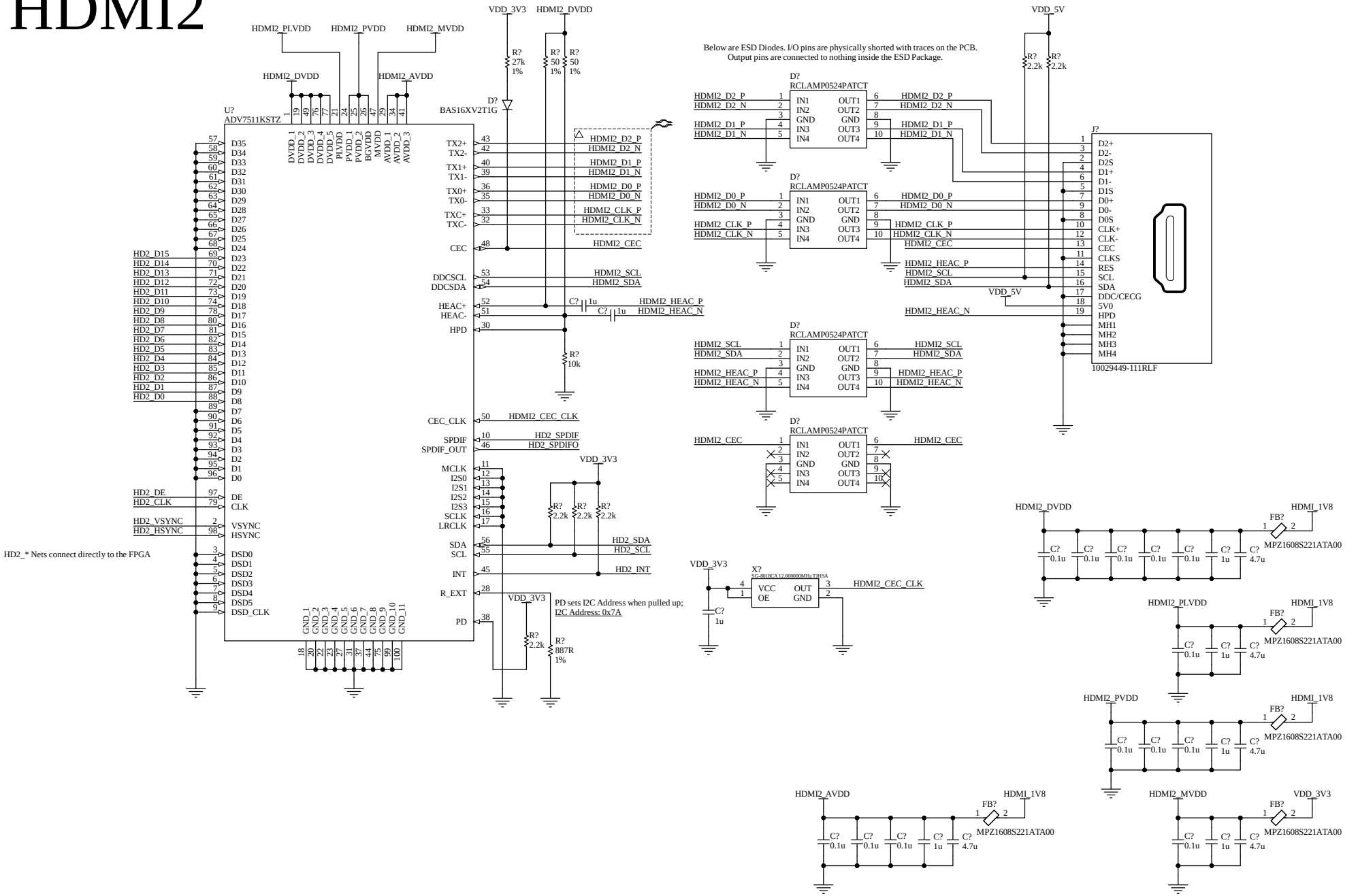
HDMI2



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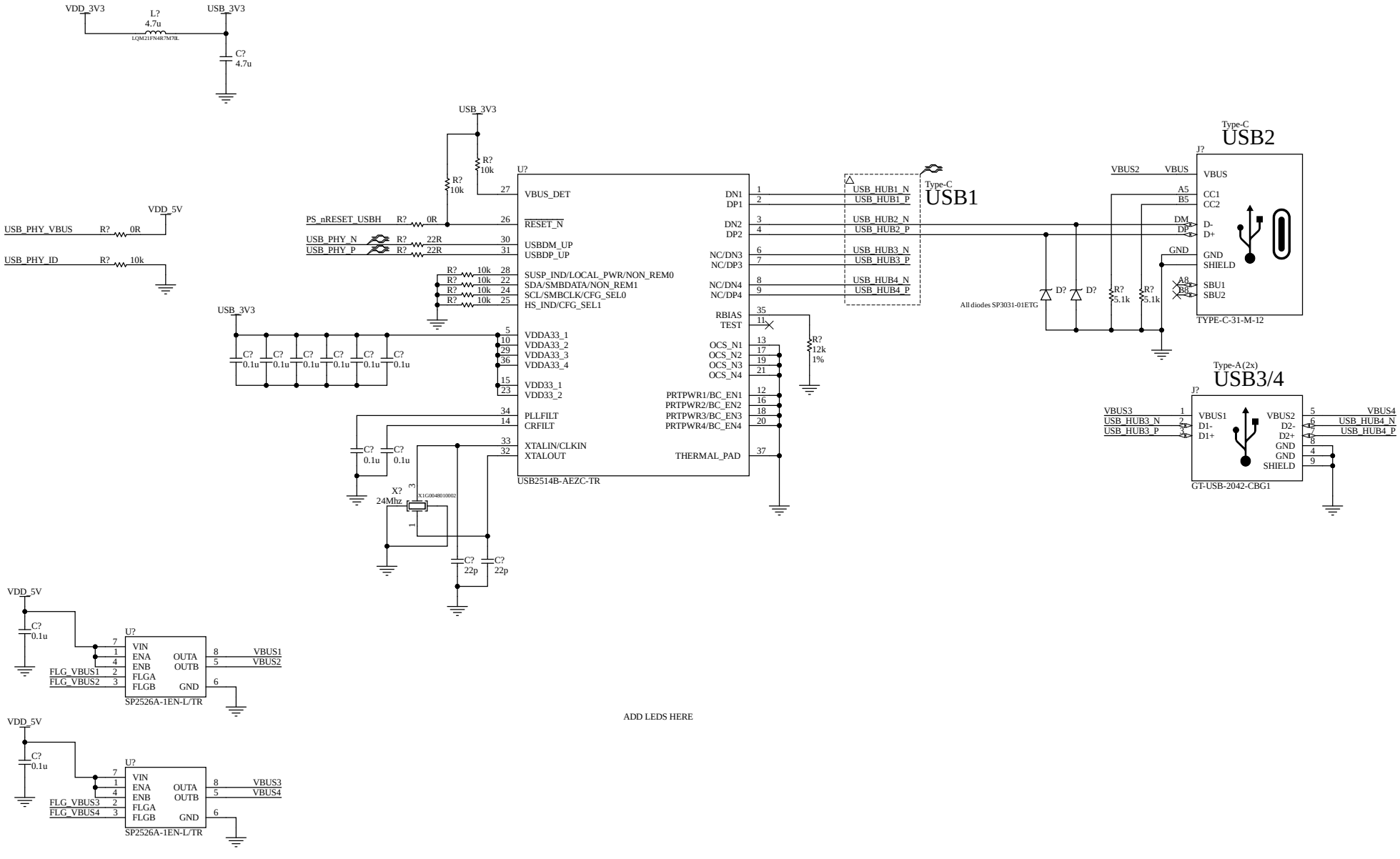

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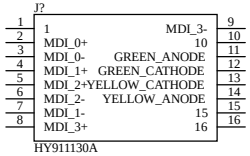

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