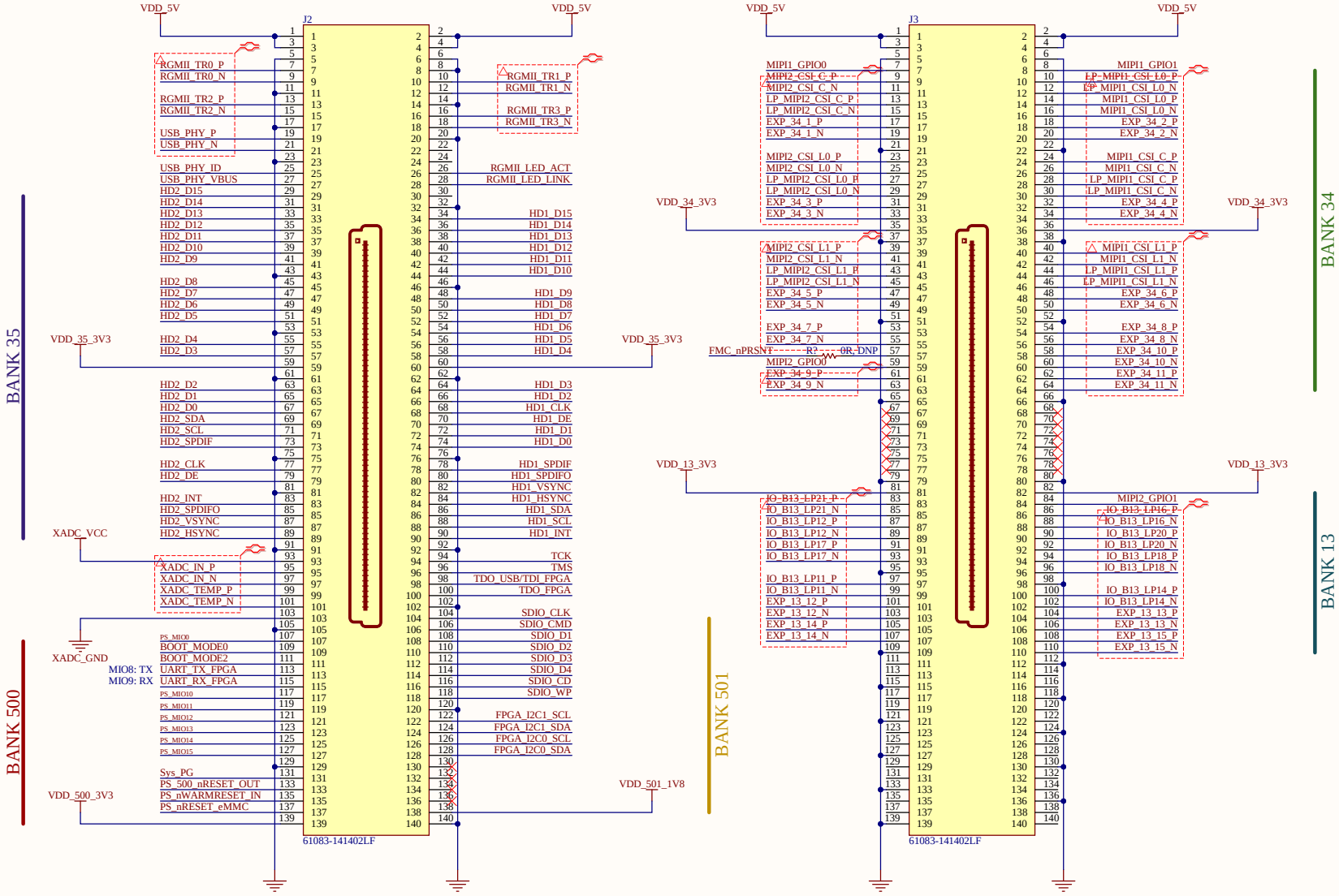
Hasan AlAref • Revision 1.0 • 2025

SoM: MYC-C7Z020-V2
Package: XC7Z020-CLG400-2
Documentation

CHECK:
MIPI PLACEMENT, MIGHT BE BETTER TO PUT BOTH ON ONE SIDE
ALL DIFF PAIRS' POLARITIES
ALL CONNECTIONS WITH PACKAGE FILE

Mezzanine Board-to-Board Connectors between FPGA SOM and FPGA Development Board



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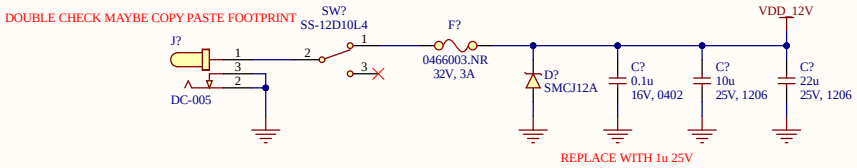
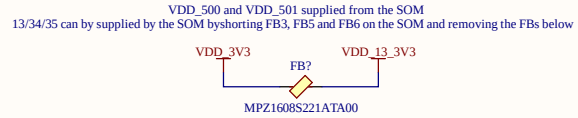
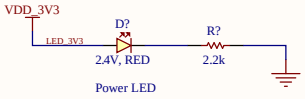
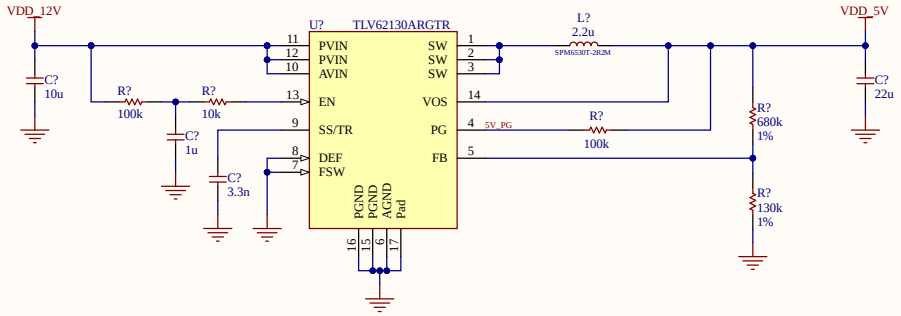
Size: A3	Number	Revision: 1.0
Date: 5/12/2025	Sheet of	
File: G:\Other computers\..\BTB Mezzanine.SchDoc	Drawn By: Hasan AlAref	

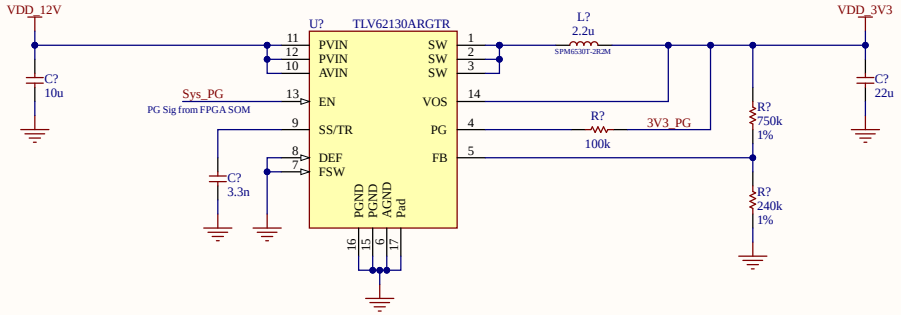
Start-up Sequence: VDD_12V > VDD_5V > FPGA SOM > VDD_3V3 > HDMI_1V8 > FTDI_1V8











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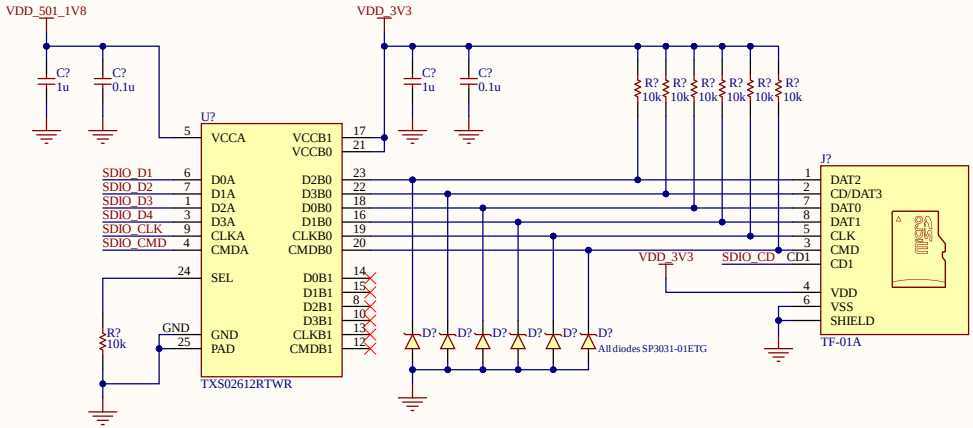
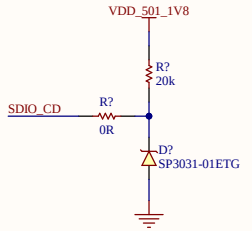
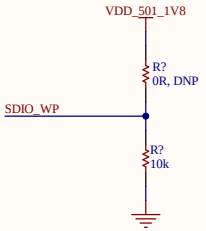
Date: 5/12/2025		Sheet of	
File: G:\Other computers\..\Power.SchDoc		Drawn By: Hasan AlAref	

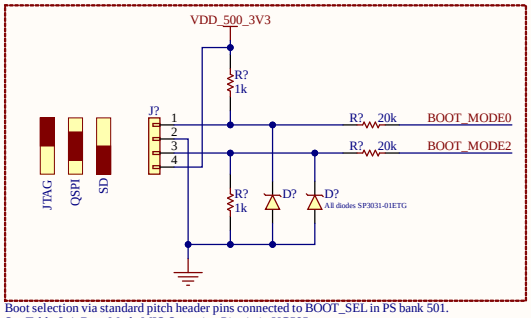
SD CARD





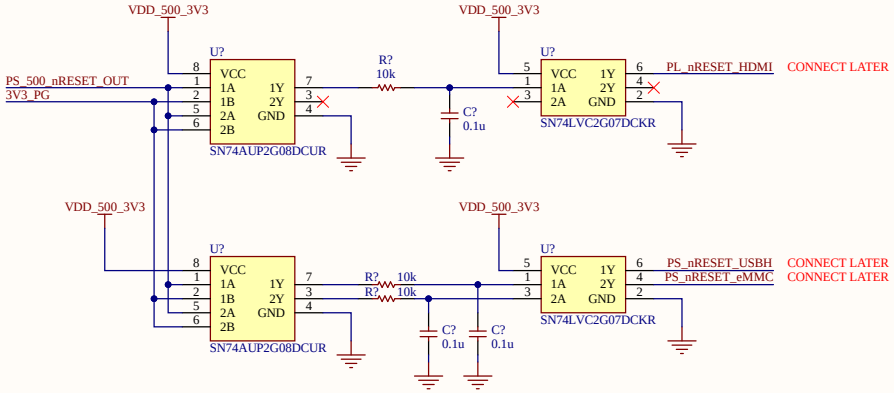


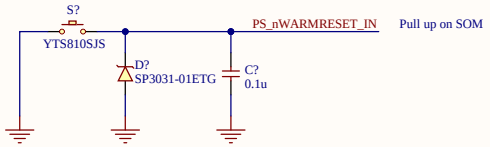
BOOT SEL



Boot selection via standard pitch header pins connected to BOOT_SEL in PS bank 501.
See Table 6-4: Boot Mode MIO Strapping Pins in in UG585.

RESET





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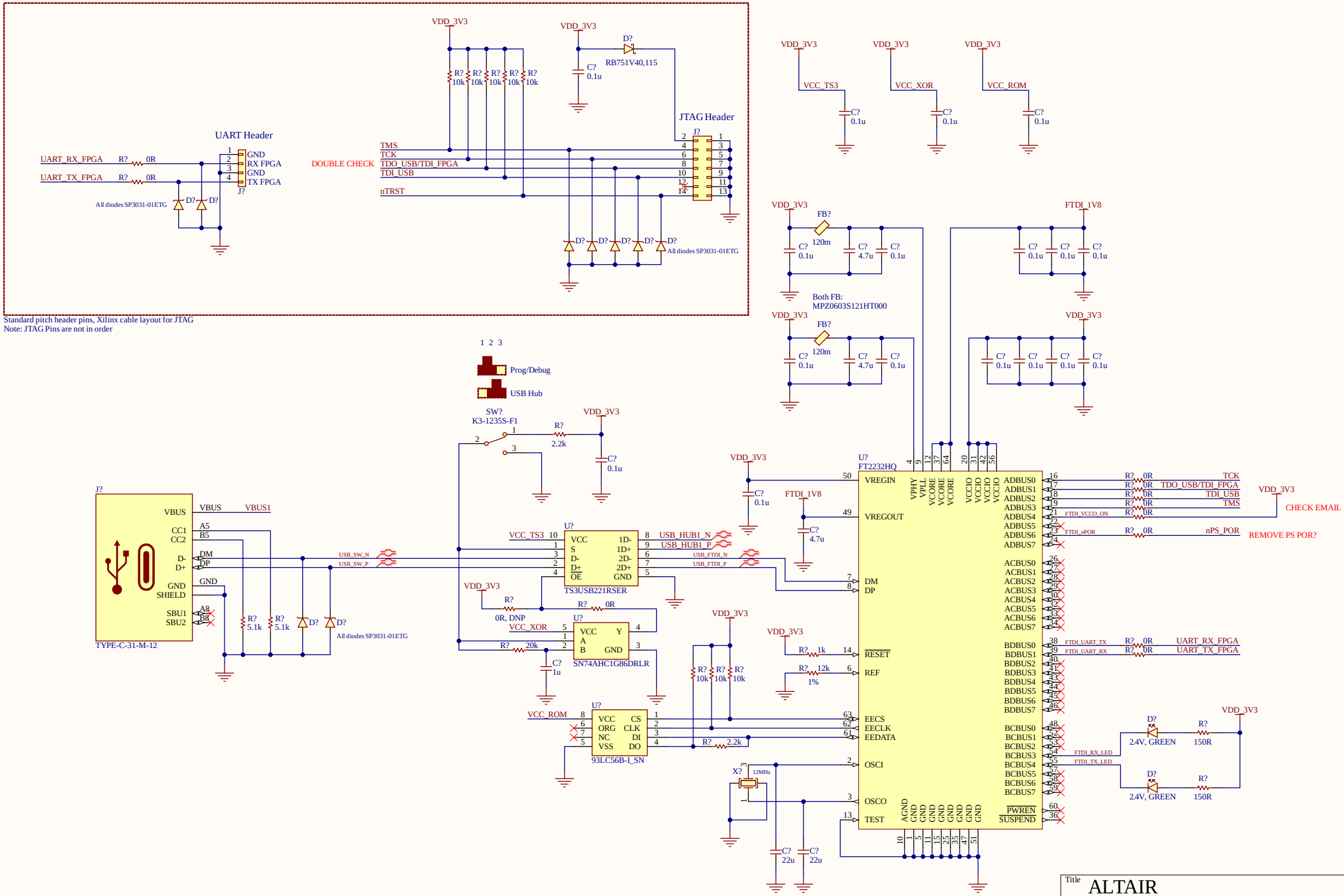
File: G:\Other computers\..\SD & Boot.SchDoc	Drawn By: Hasan AlAref	


UART Header
UART_RX_FPGA
UART_TX_FPGA
GND
RX FPGA
TX FPGA
All diodes SP3031-01ETG
DOUBLE CHECK
JTAG Header
TMS
TCK
TDO_USB/TDI_FPGA
TDI_USB
nTRST
RB751V40,115
Standard pitch header pins, Xilinx cable layout for JTAG
Note: JTAG Pins are not in order
Prog/Debug
USB Hub
SW?
K3-1235S-F1
TYPE-C-31-M-12
TS3USB221RSER
SN74AHC1G86DRLR
93LC56B-I_SN
FT2232HQ
Both FB:
MPZ0603S121HT000
2.4V, GREEN
CHECK EMAIL
REMOVE PS POR?
Title
ALTAIR
Size
A3
Number
Revision
1.0
Date:
5/12/2025
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File:
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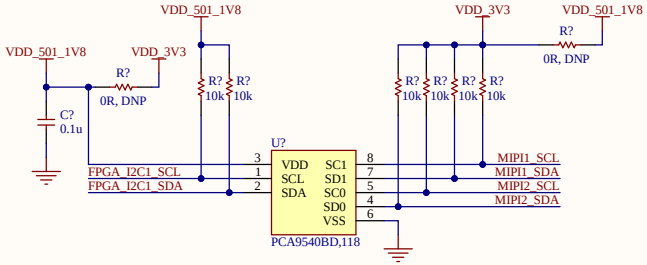
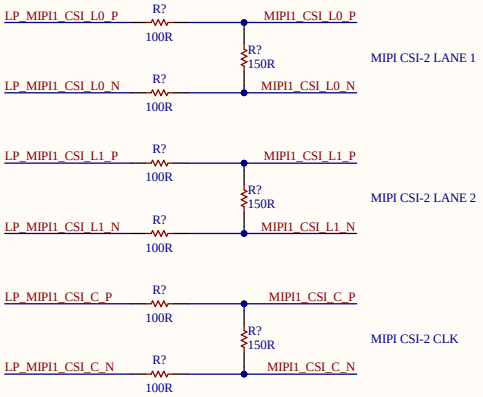
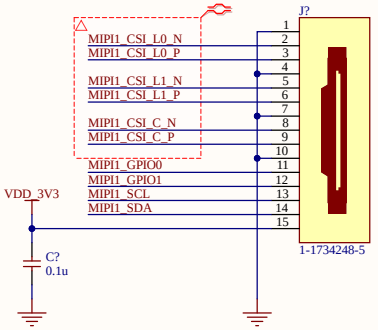
CORRECT VOLTAGES? FOR VOLTAGE TRANSLATION



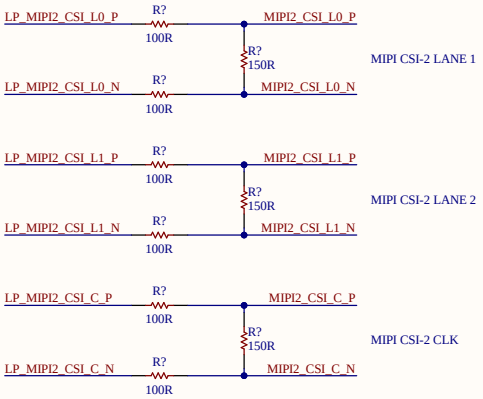
DOUBLE CHECK FOOTPRINT

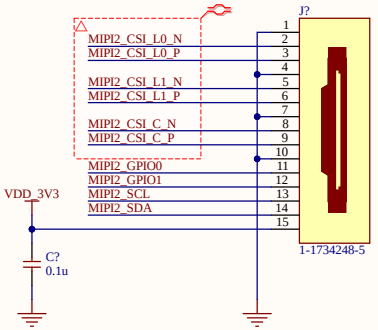




ALL RESISTORS 1%

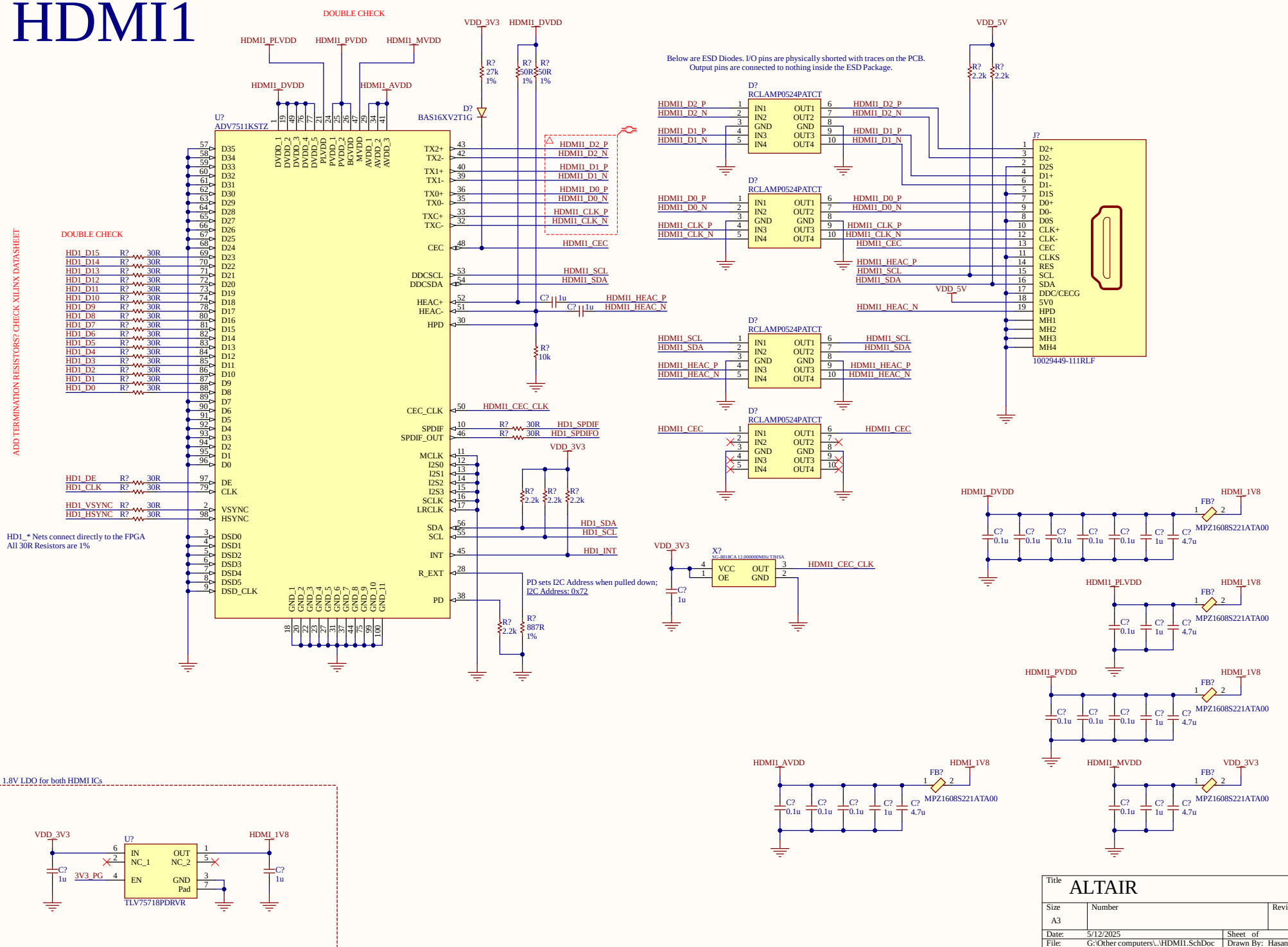
Place all 150R resistors and 100R shunt resistors next to BTB Connectors





Title: ALTAIR		
Size: A3	Number:	Revision: 1.0
Date: 5/12/2025		Sheet of
File: G:\Other computers\..\MIPI.SchDoc		Drawn By: Hasan AlAref

HDMI1



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Date: 5/12/2025		Sheet of
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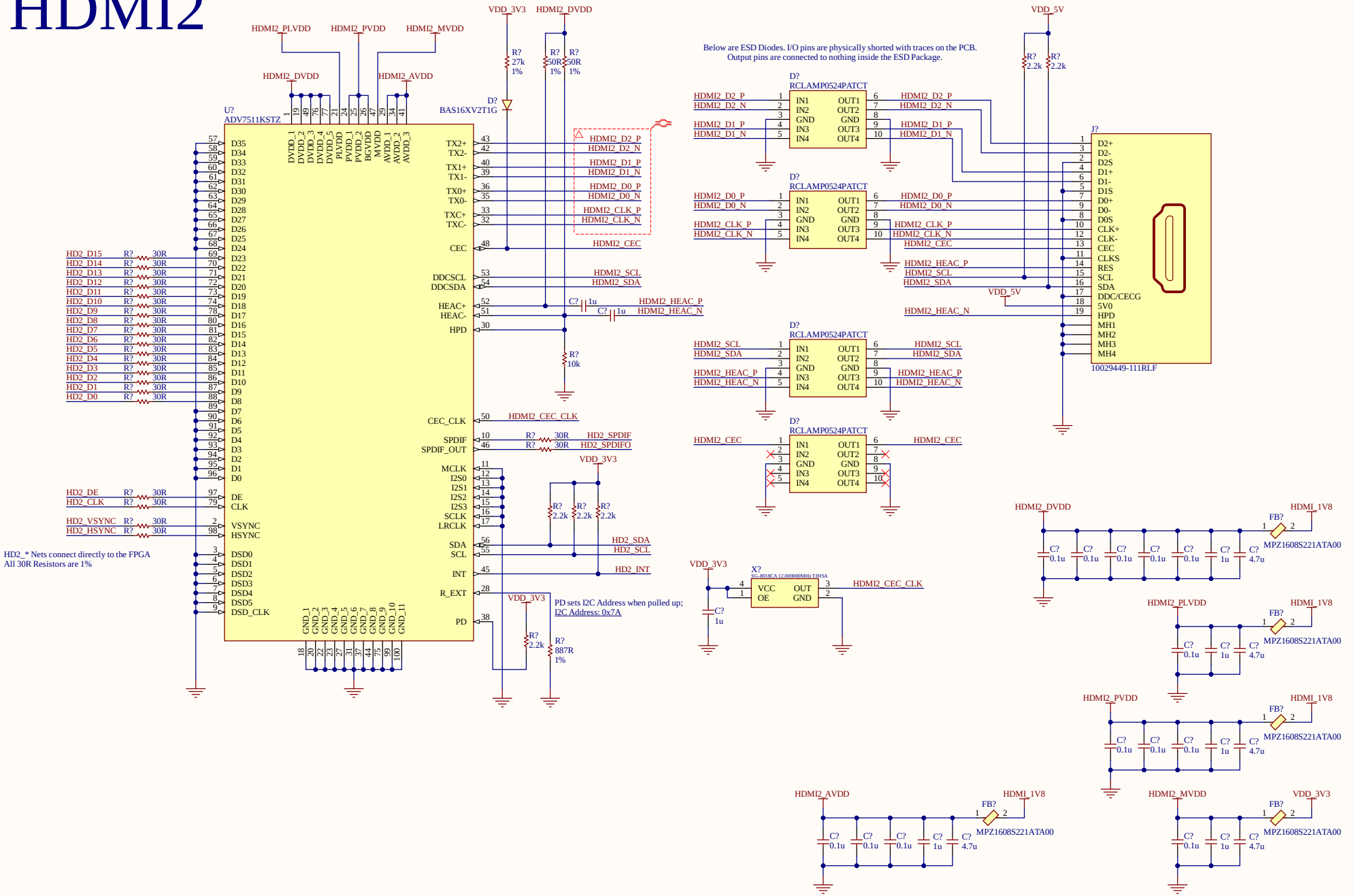
HDMI2



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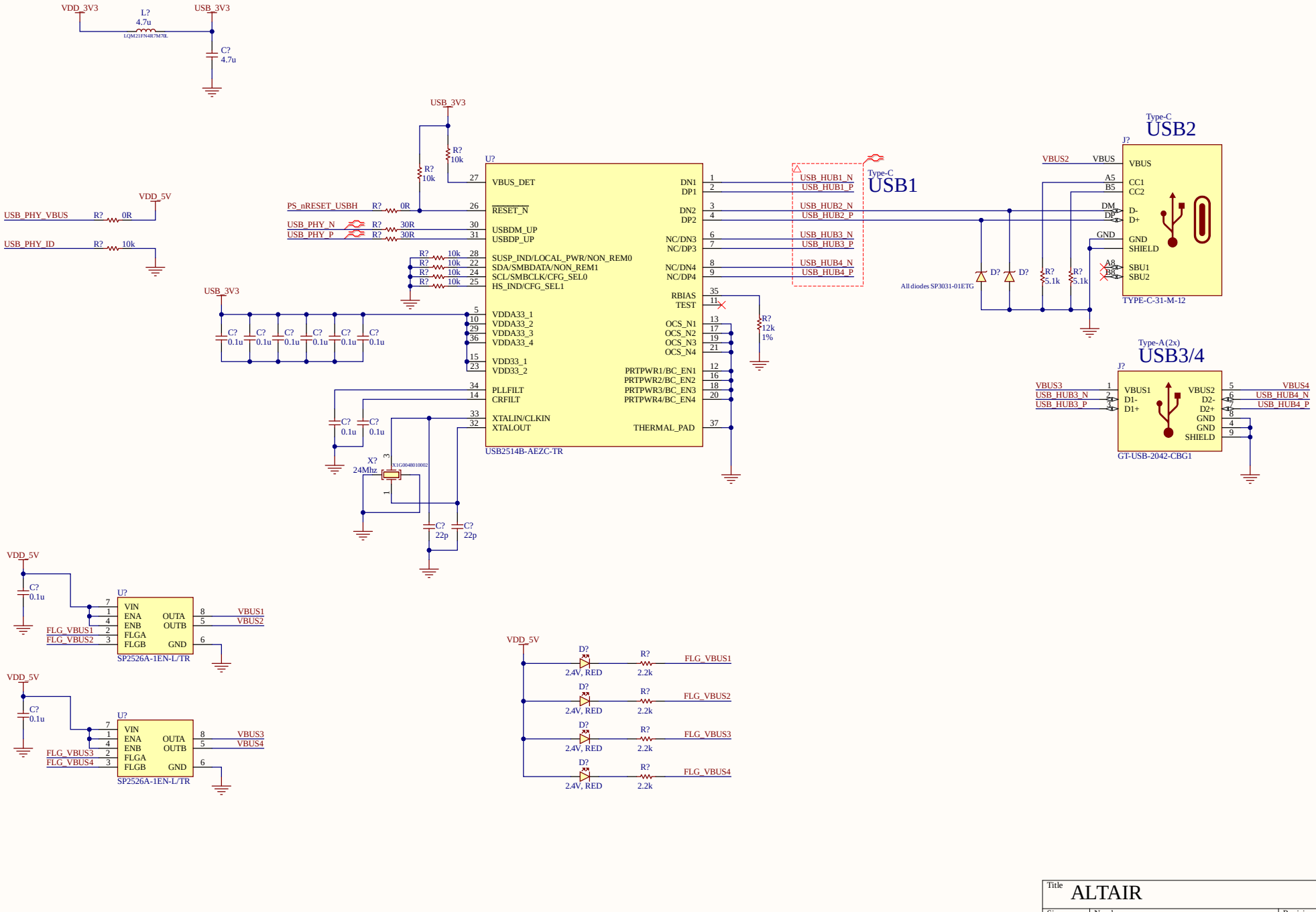

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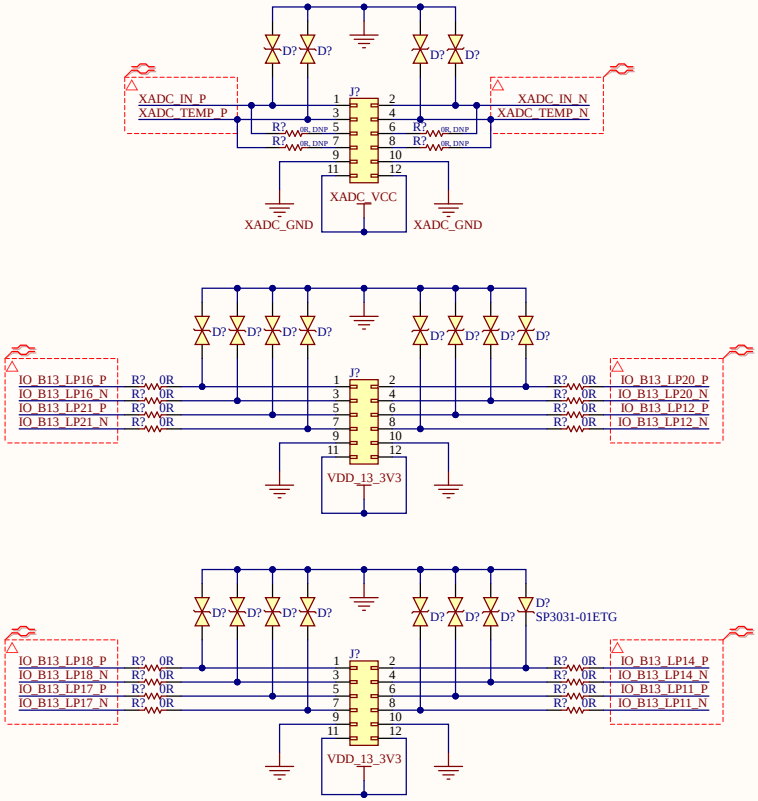
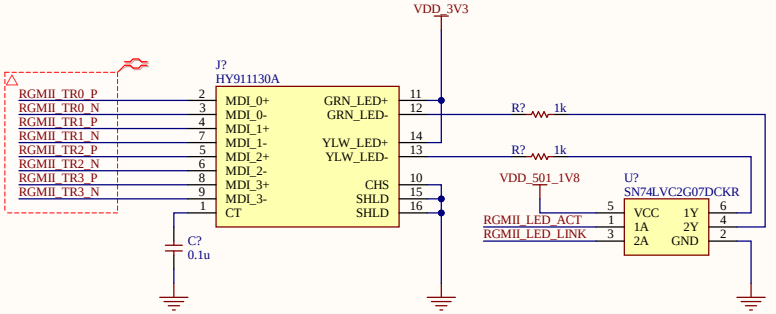
PMOD

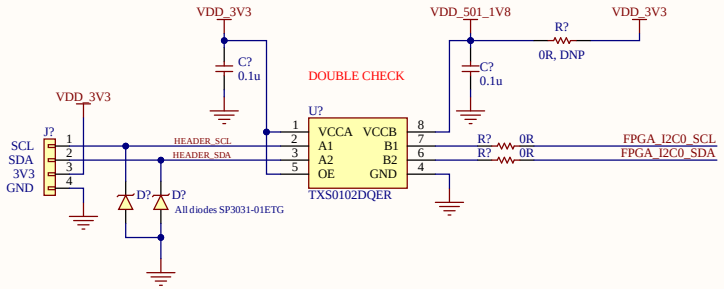


PMOD via standard pitch header pins connected to Bank 13.
All ESD Diodes SP3022-01ETG.

ETHERNET



I2C Header



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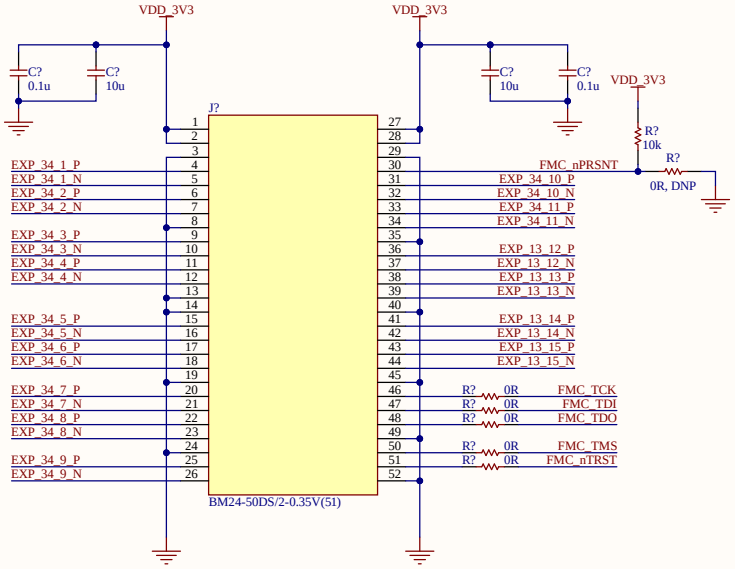

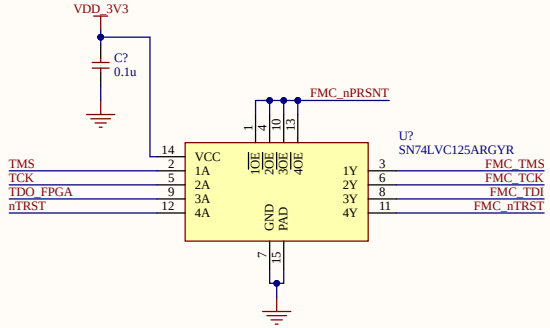

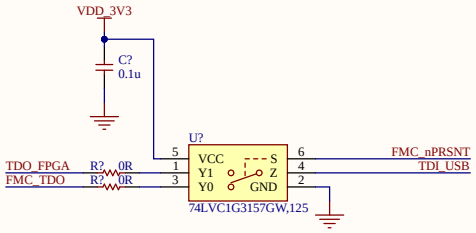

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