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CS381-16 Assignment 2

Answer to 2.1

a. Floating point addition time = 5 + 2 * 2 = 9 ns
b. Unpipelined FP addition = 9 * 1000 = 9000 ns
c. Pipelined FP addition = fetch delay + other remaining operators store
   = 2 * 1000 + 5 + 2 = 2007 ns
d. When there is a level 1 cache miss, the fetch is done from L2 cache so the time to fetch increases from 2 nanoseconds to 5 nanoseconds. When there is a level 2 cache miss, there is a fetch from main memory, the time increases to 50 nanoseconds so there is significantly more delay.

Answer to 2.3

The first pair of nested loops will have 4 misses one for each beginning of the row A[0][0], A[1][0], A[2][0], A[3][0] as there would be miss before each new line is loaded in cache.
In the second pair, there would also be 4 misses, one for the first run of the nested for loop for A[0][0], A[1][0], A[2][0], A[3][0]. It seems that a larger matrix and a larger cache does improve the performance of the second loop only if the cache is large enough to hold all the elements of the matrix. Otherwise if there is a smaller cache, the first loop has a better performance than the second loop.

Answer to 2.4

Logical address space = 2 ^ 32 bytes
Total number of pages = 2^20
Size of each page = 2^12 bytes