AIR UNIVERSITY	**Department of Electrical and Computer Engineering**
	Subject: Linear Integrated Circuit Design
	LAB # 6 CS-amplifier on Cadence Virtuoso

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Objective: Investigate common source amplifiers using Cadence-Vituoso

LAB ASSESSMENT:

Attributes	Excellent (5)	Good (4)	Average (3)	Satisfactory (2)	Unsatisfactory (1)
Ability to Conduct Experiment					
Ability to assimilate the results					
Effective use of lab equipment and follows the lab safety rules					

Total Marks: 15 Obtained Marks : _____

LAB REPORT ASSESSMENT:

Attributes	Excellent (5)	Good (4)	Average (3)	Satisfactory (2)	Unsatisfactory (1)
Data presentation					
Experimental results					
Conclusion					

Total Marks: 15 Obtained Marks: _____

Date: _____ Signature: _____

CS-amplifier on Cadence Virtuoso

Objectives:

The objective of this lab is to.

- Investigate common source amplifiers using Cadence-Vituoso
- Observe the various graphs of the different configurations on Common-Source Amplfier

Apparatus:

- VMware workstation
- CentOS 6.5
- Candence Virtuoso

Procedure:

- Common source amplifier with a resistive load

  a. Determine input-output characteristics Vin-Vout, identify the regions of operation and the operating region that is most suitable for amplification.

  b. Observe the output current, transconductance and gain as a function of Vin.

  c. Bias the amplifier and amplify a small signal without distortion and determine the gain.

- Common source amplifier with a current source load and diode connected load

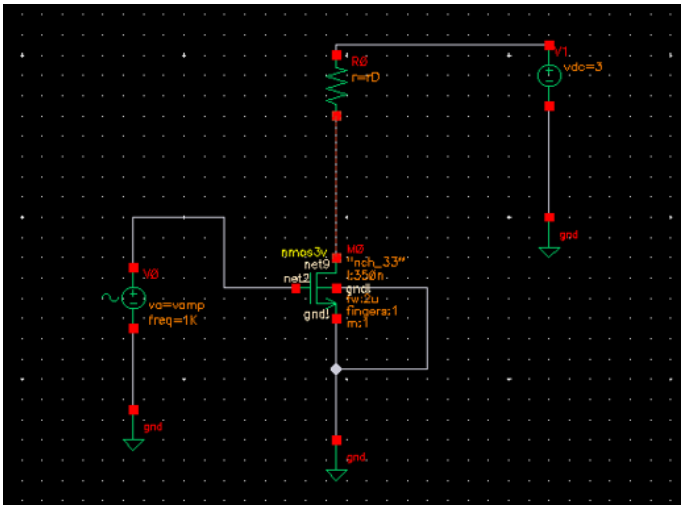
  a. Input-output characteristics Vin-Vout, transconductance and gain as a function ofVin; biasing and amplification of a small signal and determine the gain.

- Comparison

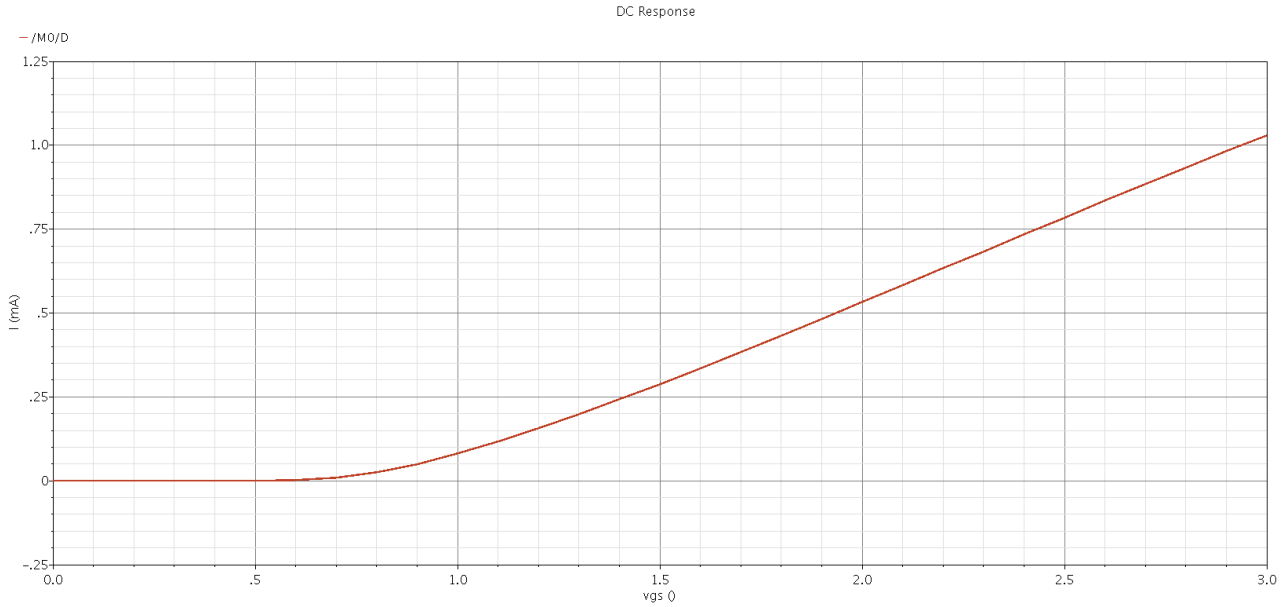
  a. Input-output characteristics; gain, and signal swing.

Implementation:

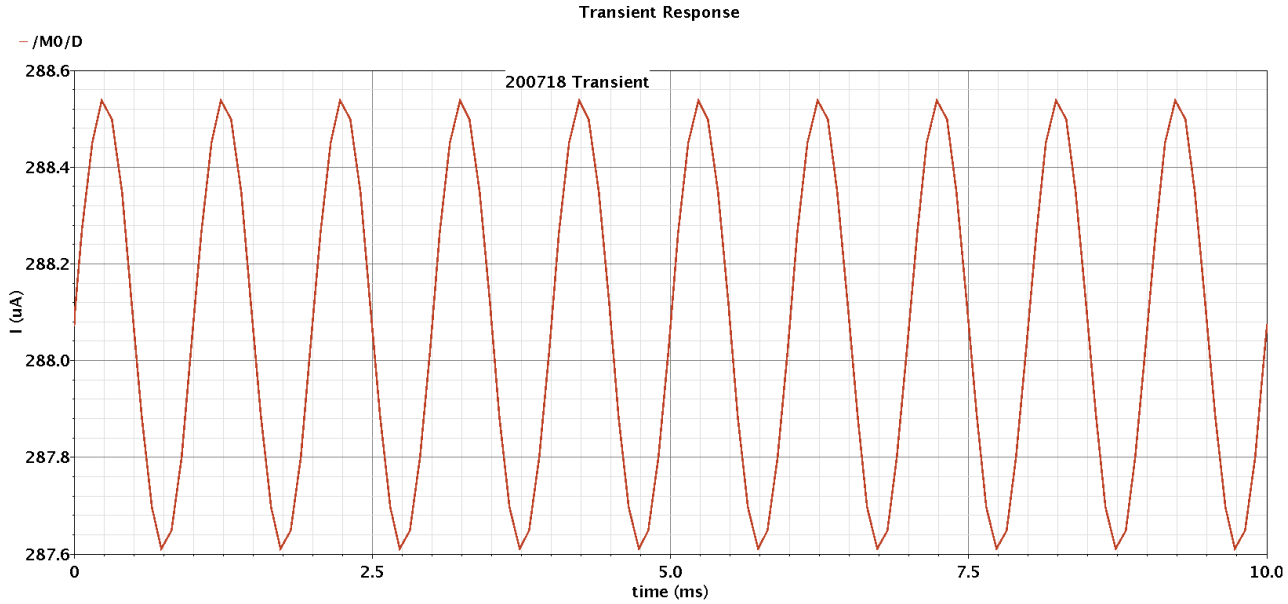
With Resistive Load



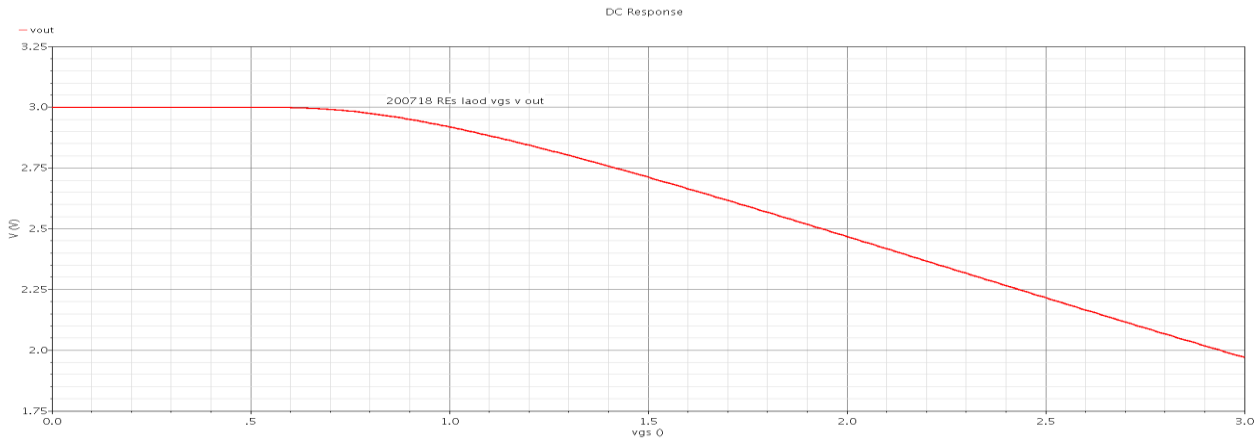
Drain Current vs VGS:



Transient Analysis:



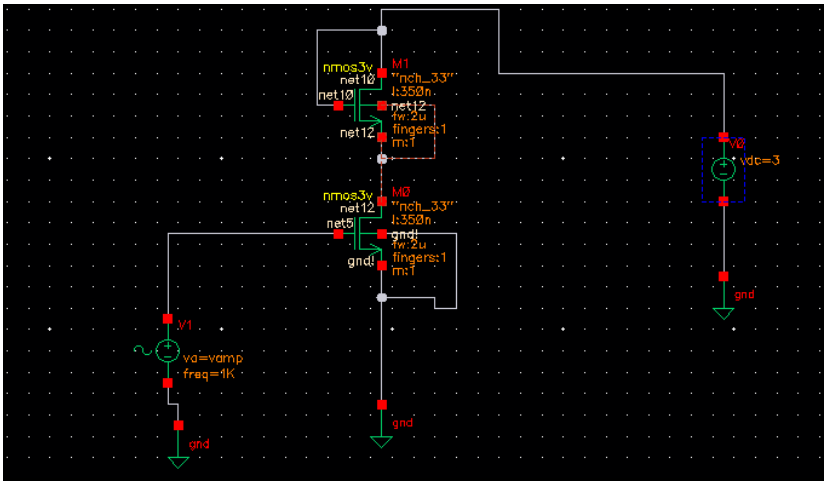
Vout Vs Vgs:



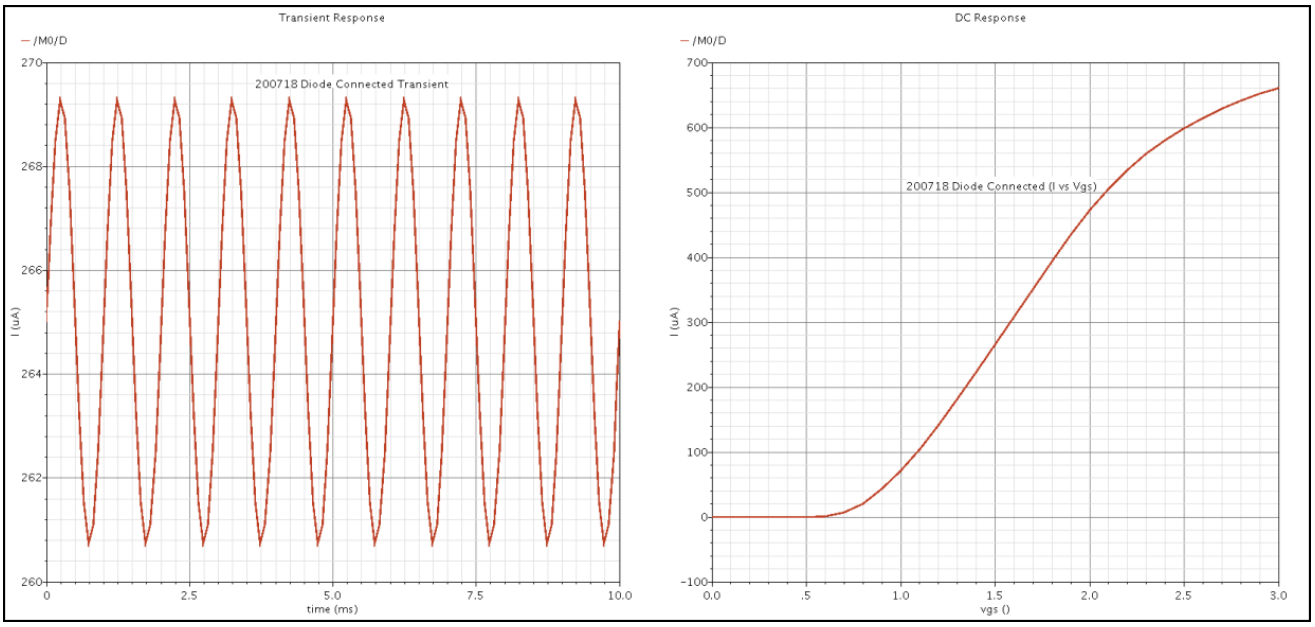
Explanation:

In common source amplifier with resistive load we set the properties of the Vsine voltage to variable voltage so that we can change the vgs voltage in the graph.To plot the current versus vgs graph we select the drain terminal of the MOSFET similarly transient analysis we set the stop timeas ten microseconds and for vgs vs Vout graph we select the wire instead of the drain terminal.

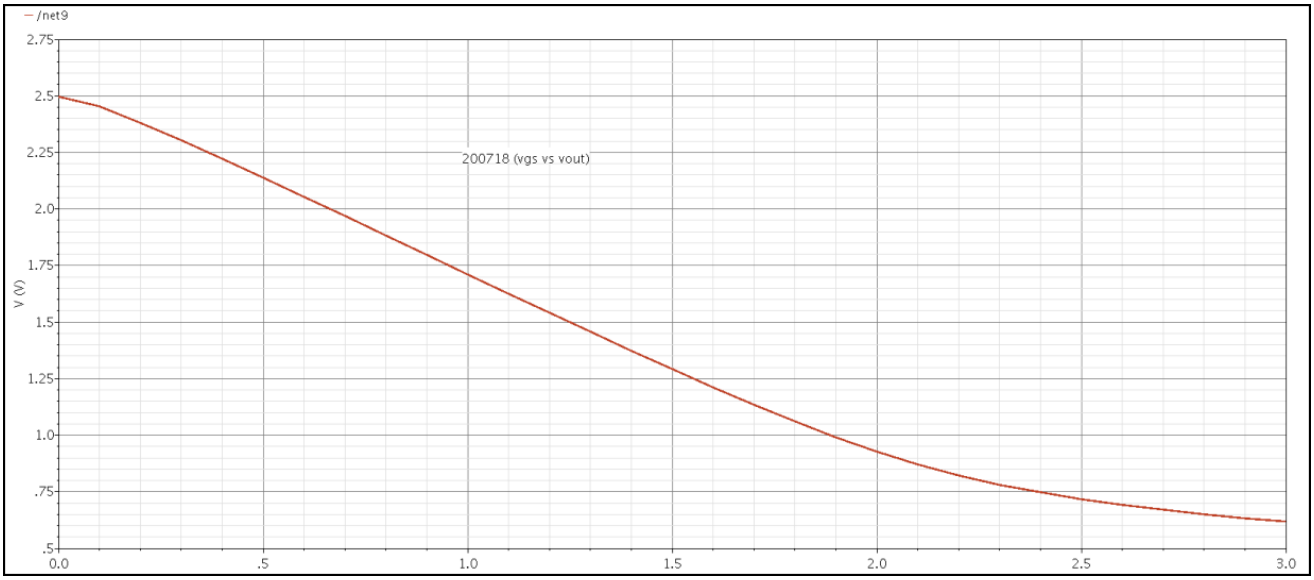
Common Source Amplifier With Diode Connected load



Drain Current vs VGS and Transient Analysis:



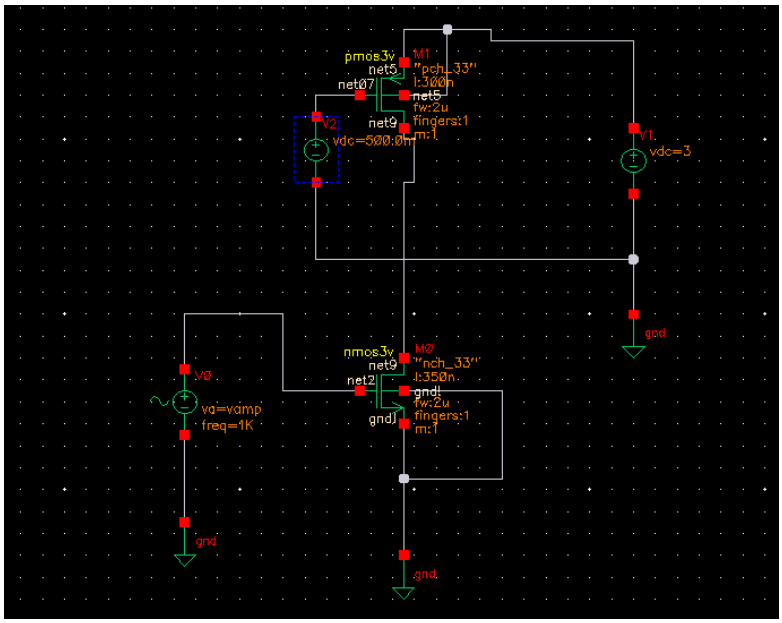
Vout Vs Vgs:



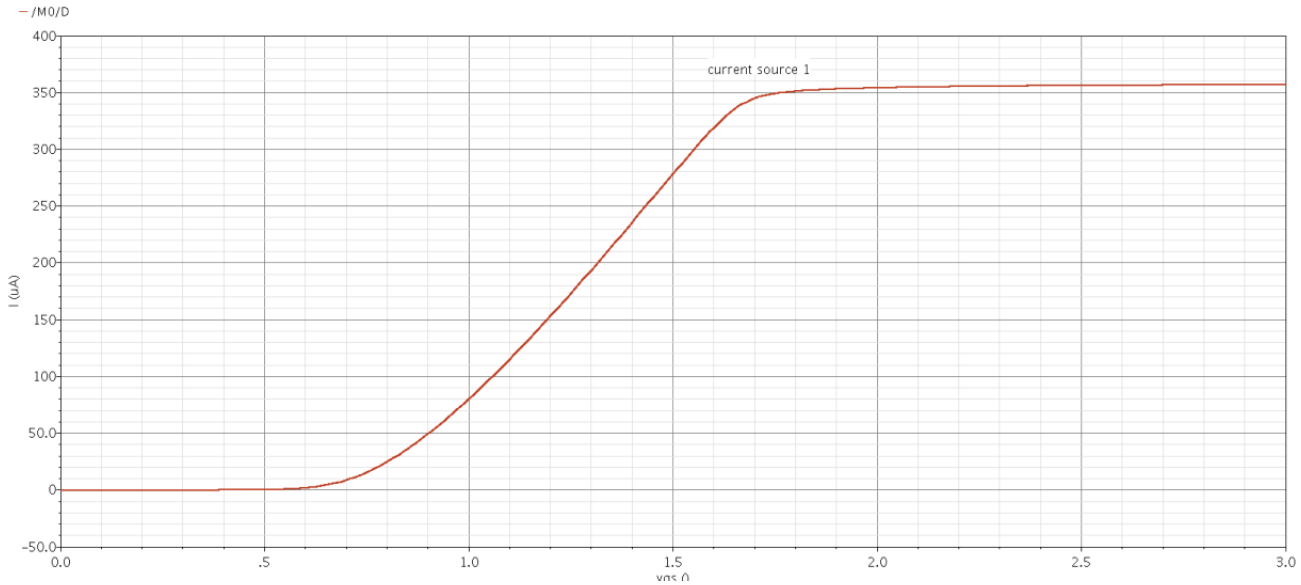
Explanation:

In common source amplifier with Diode connected load we replace the resistor with another NMOS and connect its gate with the dc supply.Rest of the procedure is same as it was with the resistive load to get above graphs.

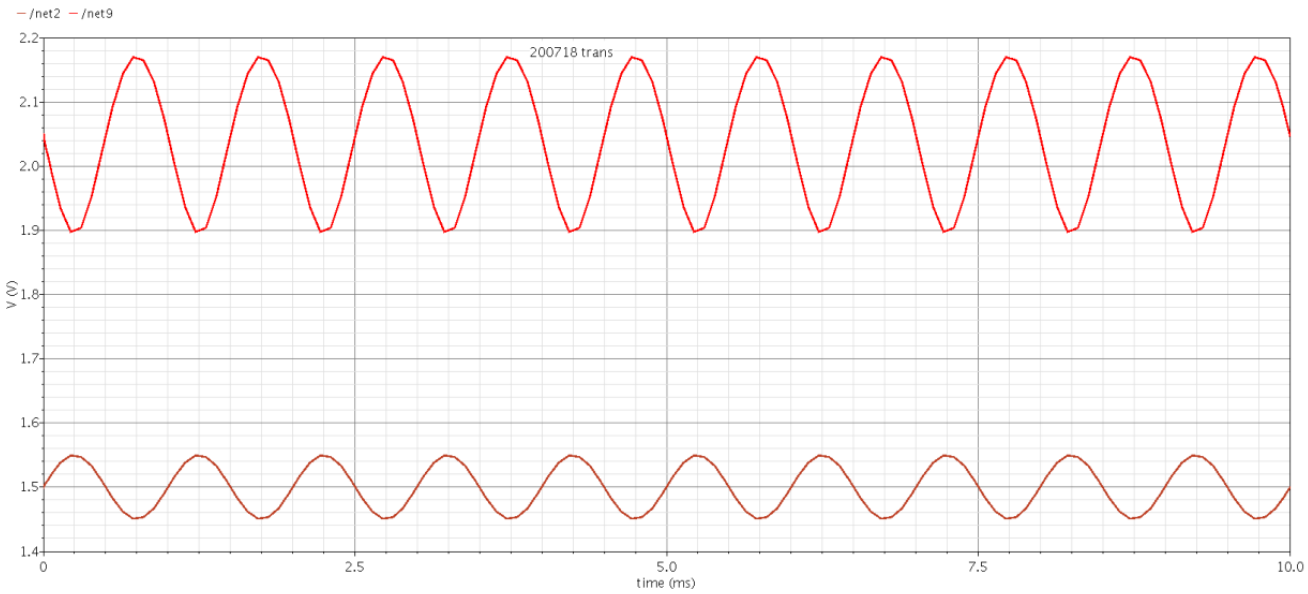
Common source amplifier with a current source load and diode



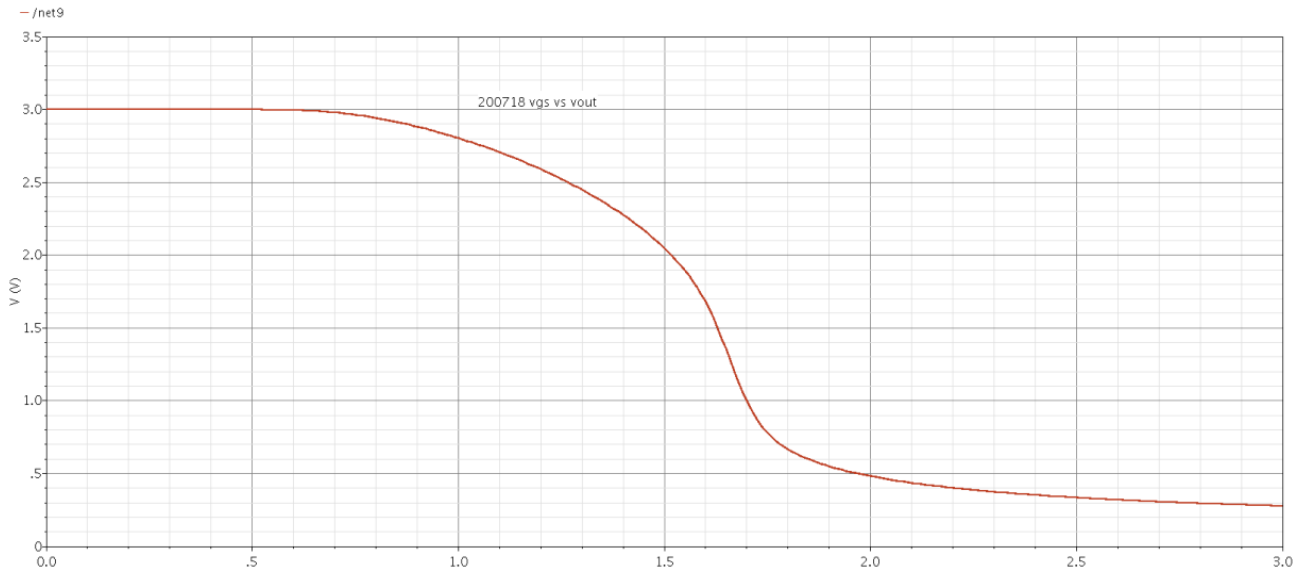
Drain Current vs VGS:



Transient Analysis:



Vout vs Vgs:



Explanation:

For the PMOS we need to find the gate voltage where it goes into saturation mode. For transient analysis select both the input wire from the Nmos Gate and the output Wire between the drains of the two mosfets.

Conclusion:

In this lab we performed simulation of different configurations of the Common Source Amplifer and performed Dc and Transient analysis .We also plotted the input and output relationship of all the configurations.