AIR UNIVERSITY	**Department of Electrical and Computer Engineering**
	Subject: Linear Integrated Circuit Design
	LAB # 5 Designing symbol from schematic and symbol simulation

Student Name: Muhammad Haseeb **Reg. No:** 200718 **Section:** BEEE-7A

Objective: Design a symbol of an inverter in Cadence Virtuoso.

Use the symbol in a sample circuit and perform its simulation.

LAB ASSESSMENT:

Attributes	Excellent (5)	Good (4)	Average (3)	Satisfactory (2)	Unsatisfactory (1)
Ability to Conduct Experiment					
Ability to assimilate the results					
Effective use of lab equipment and follows the lab safety rules					

Total Marks: 15 Obtained Marks : _____

LAB REPORT ASSESSMENT:

Attributes	Excellent (5)	Good (4)	Average (3)	Satisfactory (2)	Unsatisfactory (1)
Data presentation					
Experimental results					
Conclusion					

Total Marks: 15 Obtained Marks: _____

Date: _____ Signature: _____

Designing a symbol from schematic and symbol simulation

Objectives:

The objective of this lab is to.

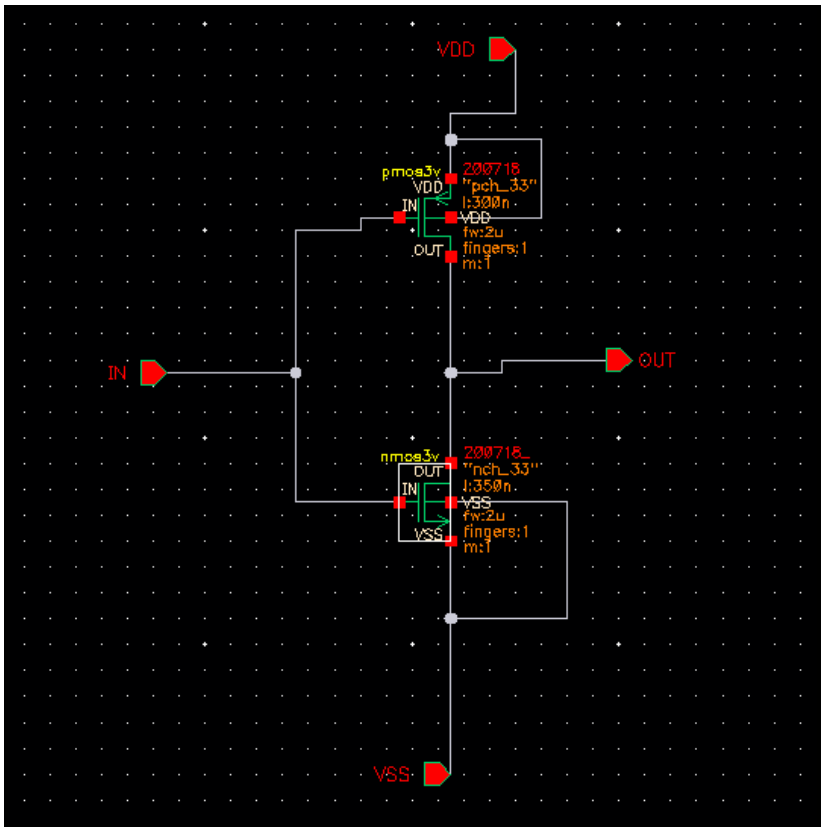
- Design a symbol of an inverter in Cadence Virtuoso.
- Use the symbol in a sample circuit and perform its simulation.

Apparatus:

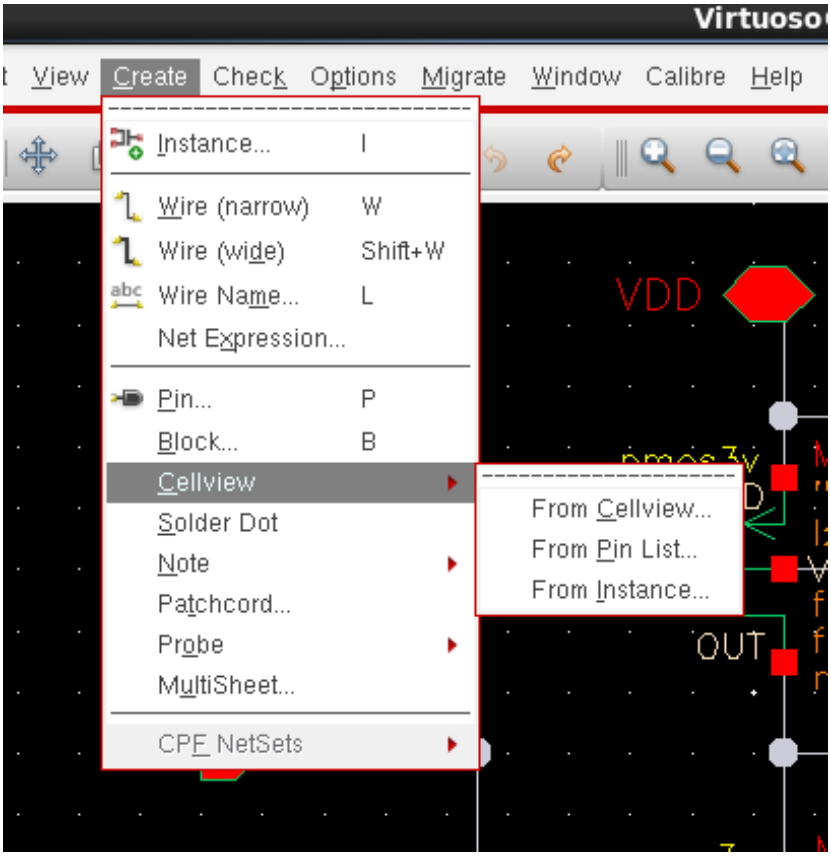
- VMware workstation
- CentOS 6.5
- Candence Virtuoso

Procedure:

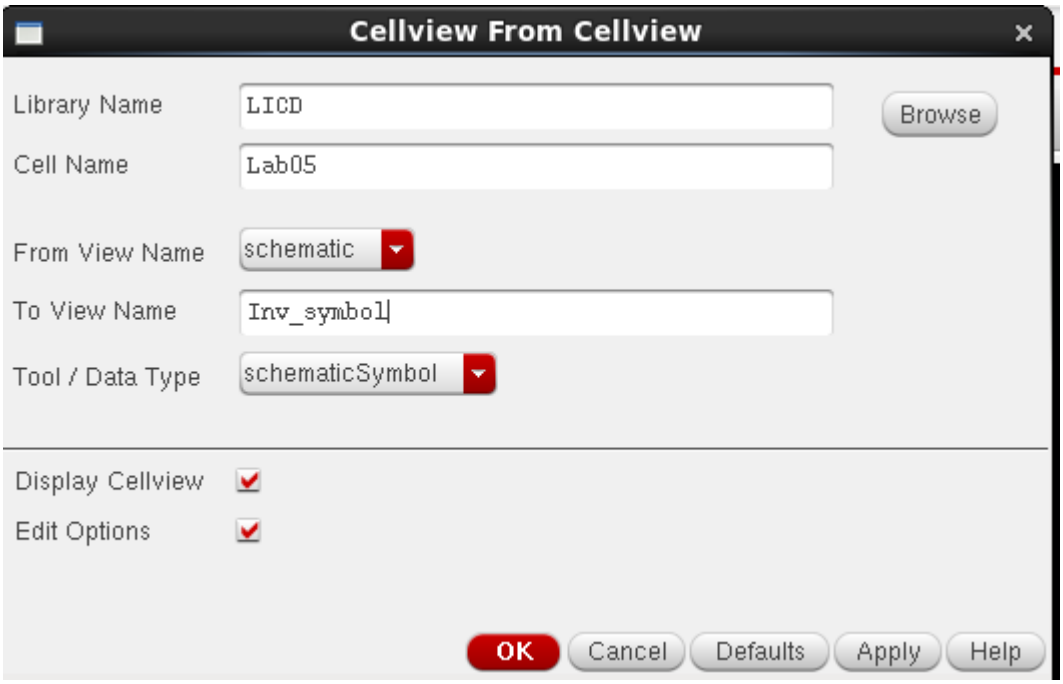
Step 1: Create the schematic of an inverter.



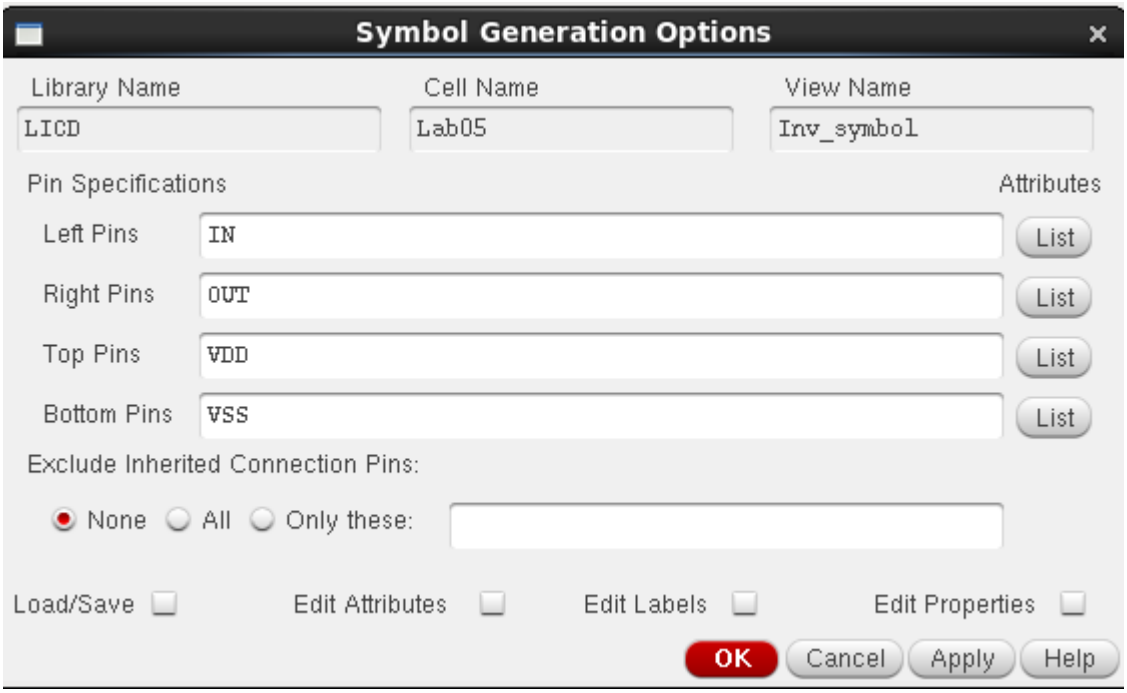
Step 2:



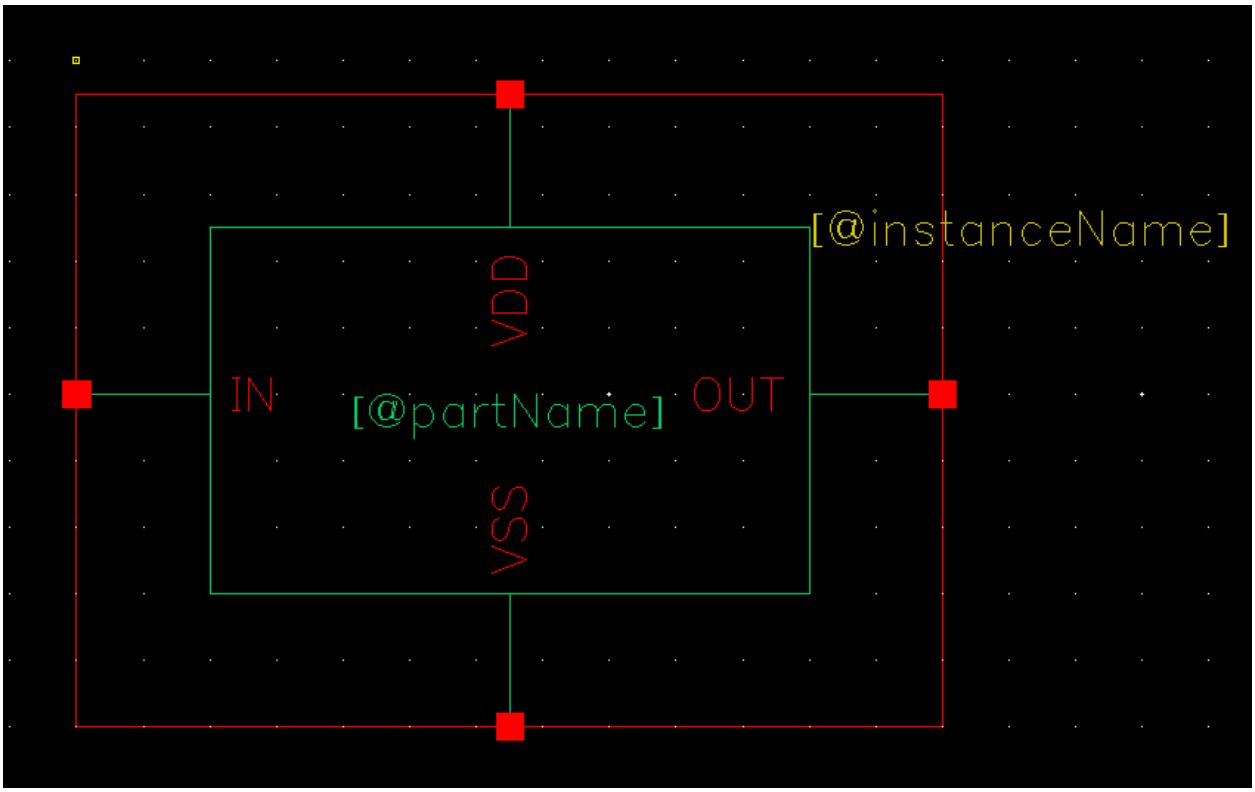
Step 3: Add symbol name and Click OK



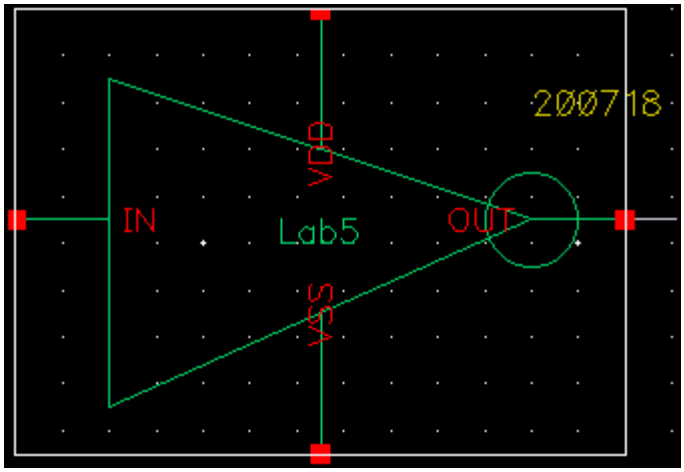
Step 4: Write pin names according to the location.



A symbol will appear like following figure.



Step 5: Modify its shape according to the original symbol of invertor using the line tool and click check & save.

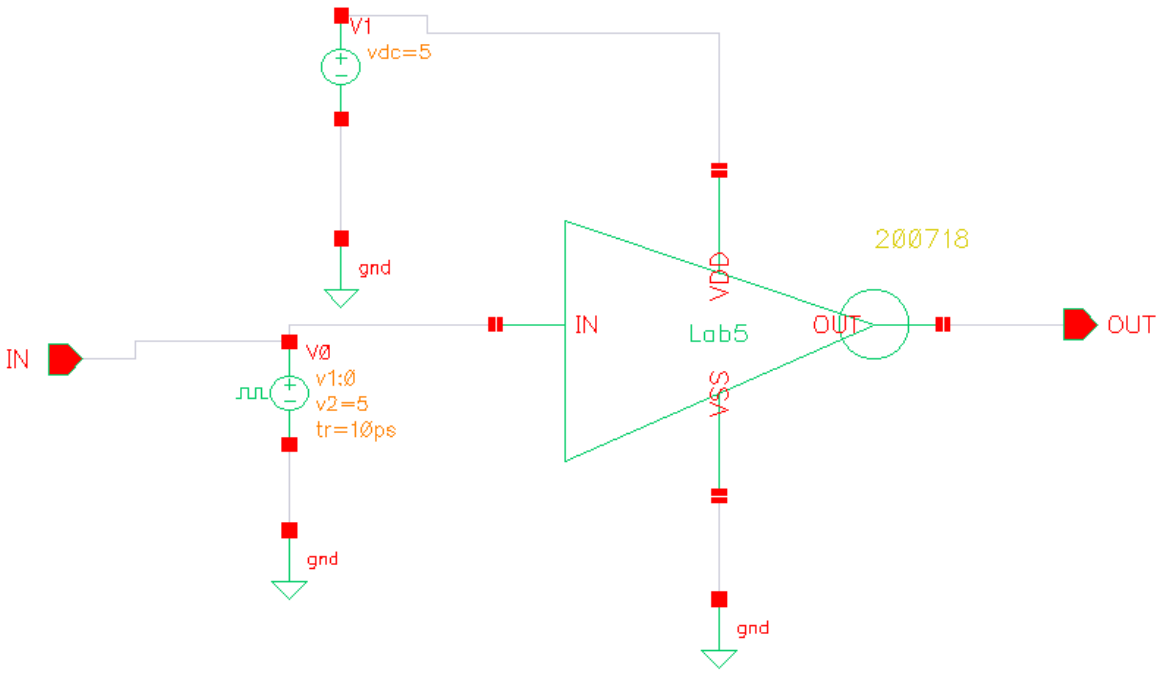


Step 6: Now use this symbol in another cell view and simulate its circuit to verify the functionality.

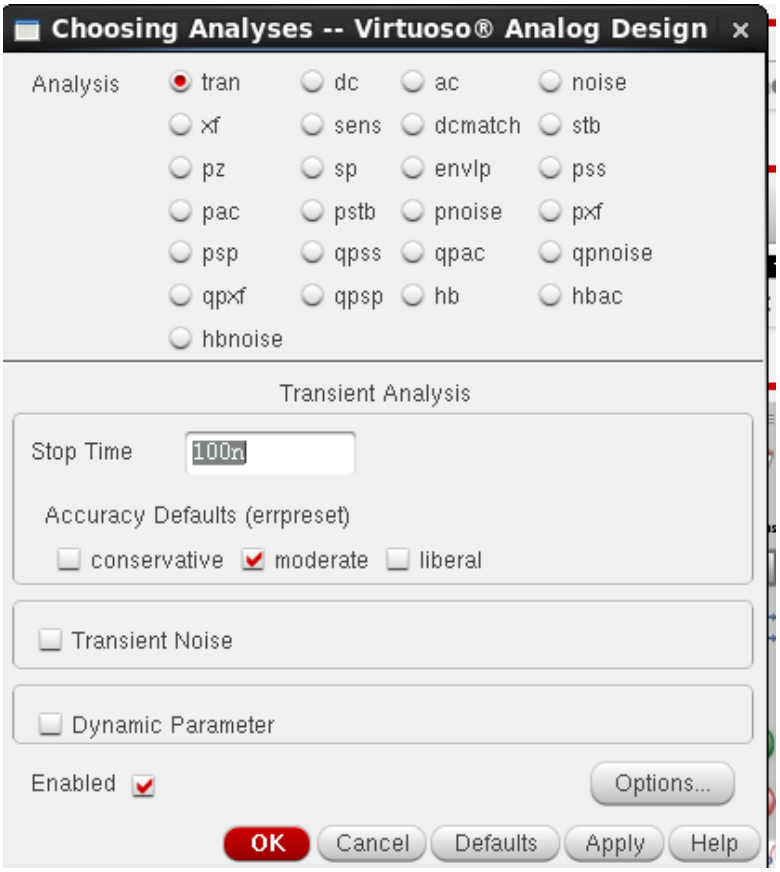
Parameters: IN= Vpulse [Voltage 1 = 0V, Voltage 2 = 5V, Pulse width = 5ns, Period=10ns, Rise/Fall time = 10ps], VDD=5v and VSS=gnd

Analysis: Transient Analysis, for time t=100ns

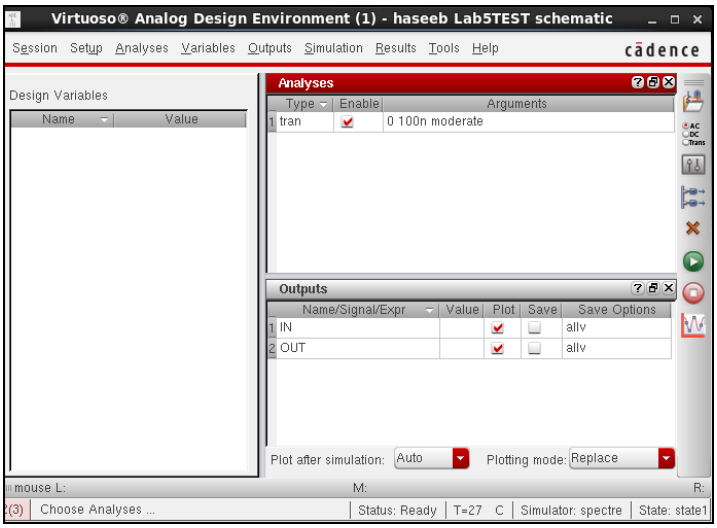
Implementation:



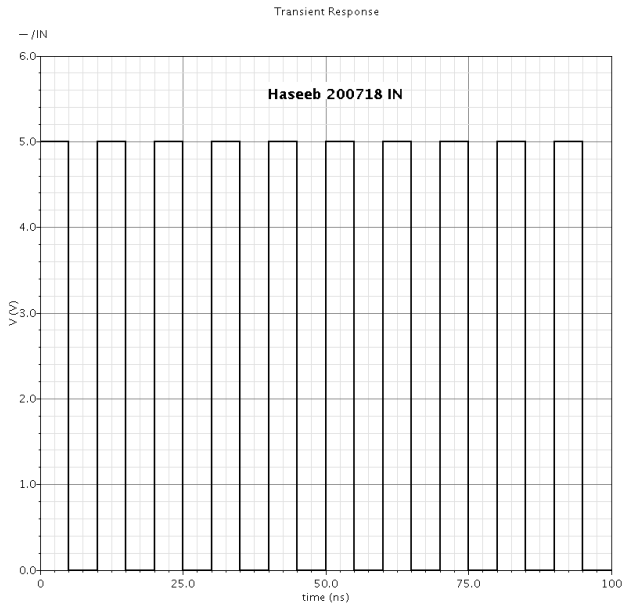
- Select transient in analysis and choose 100ns at stop time

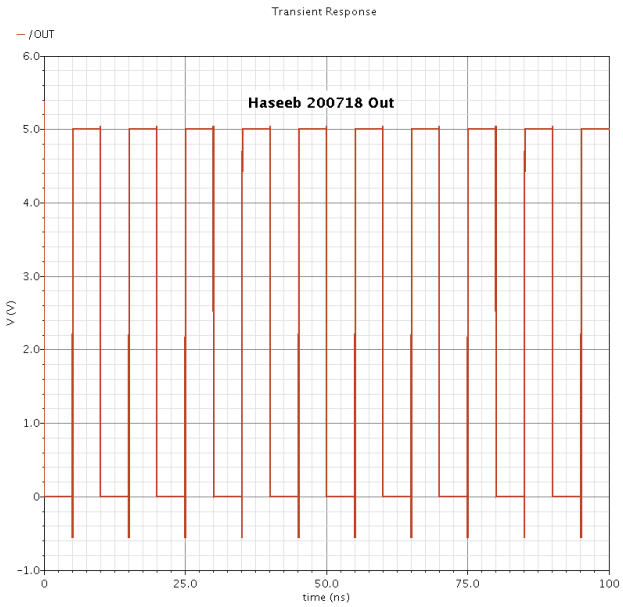


- Output points to be selected are the input and output pins



Results & Discussion:





The input pulse is applied to the gates of both the NMOS and PMOS transistors. When the input is low (0), the PMOS transistor is turned on, and the NMOS transistor is turned off.

When the input is high the NMOS transistor is turned on and the PMOS transistor is turned off so the output is zero .When the input is low , the PMOS transistor is turned on, and the NMOS transistor is turned off and the vdd from the Pmos to output terminal is shown on output.

CONCLUSION

In this lab we studied how to make an inverter on cadence virtuoso and also how to create a symbol of the circuit and then use it in other circuits.We can also manually draw the shape of the symbol.