

Department of Electrical and Computer Engineering

Subject: Linear Integrated Circuit Design

LAB # 3 Device characteristics of an PMOS.

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Objective: To observe	e various graphs	of PMOS t	ransistor					
LAB ASSESSMENT:								
Attributes	Excellent (5)	Good (4)	Average (3)	Satisfactory (2)	Unsatisfactory (1)			
Ability to Conduct Experiment								
Ability to assimilate the results								
Effective use of lab equipment and follows the lab safety rules								
	15				Obtained Marks :			
Total Marks:	15		Obtained M	Iarks :				
Total Marks:			Obtained M	Iarks :				
		Good (4)	Obtained M Average (3)	Satisfactory (2)	Unsatisfactory (1)			
LAB REPORT ASSES	SMENT: Excellent		Average	Satisfactory	Unsatisfactory			
LAB REPORT ASSES Attributes	SMENT: Excellent		Average	Satisfactory	Unsatisfactory			
Attributes Data presentation	SMENT: Excellent		Average	Satisfactory	Unsatisfactory			
Attributes Attributes Data presentation Experimental results	Excellent (5)		Average (3)	Satisfactory (2)	Unsatisfactory			

Title:

• Device characteristics of an PMOS.

Equipment:

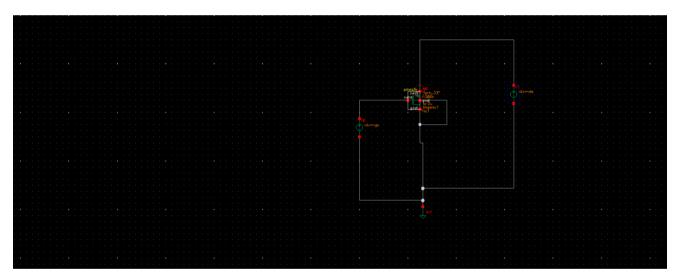
- Personal Computer
- VMware software
- Cadence Virtuoso

Introduction

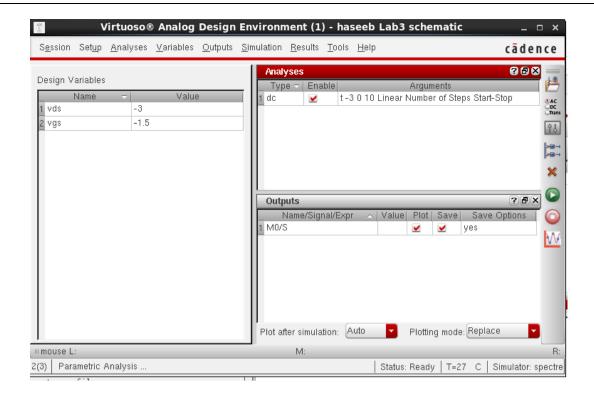
In this lab we will study about the characteristics of an PMOS transistor by obtaining various graphs between various variables and observe the region of operations.

Lab Task

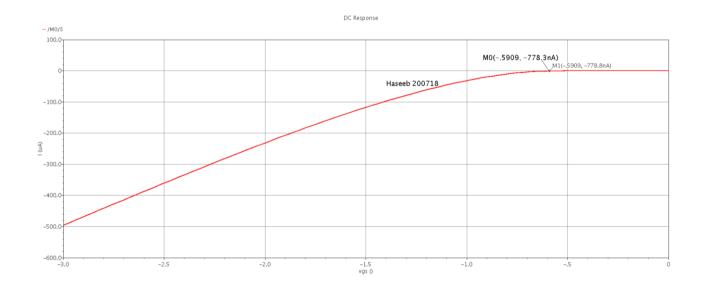
Below is the circuit which is designed on Cadence virtuoso to observe Pmos characteristics:



Click Ade L and select the following settings

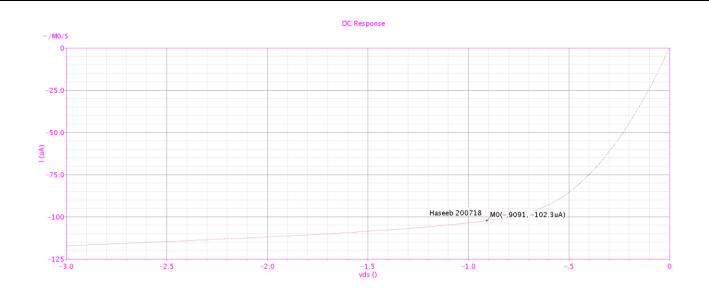


Click on run to get the following graph:



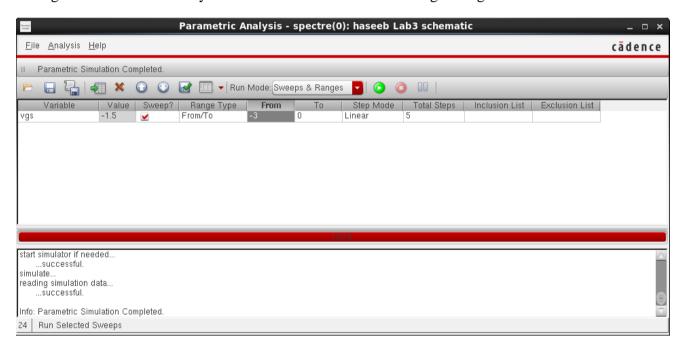
<u>Graph Explanation</u>: The labelled point on this graph is the threshold voltage VTH. The variable on x-axis is vgs and after its absolute value reaches VTH the transister goes into saturation mode and before that it remains in cutoff mode.

Now we will plot the drain current with the drain to source voltage. For this change the design variable to vds in the analysis window and then click on Run.

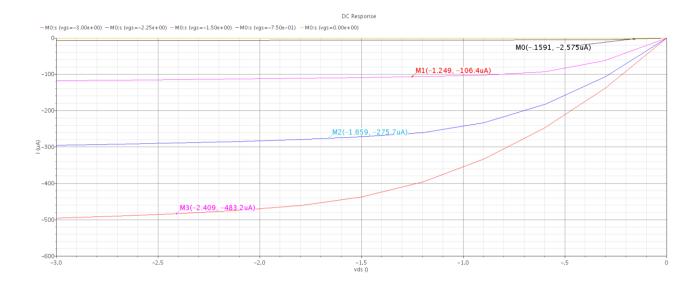


<u>Graph Explanation</u>: The labeled point is the subtraction of threshold voltage from the vgs voltage(1.5v). In the graph the transistor before this point is in triode mode and after this point it is in saturation mode.

Now go to Parametric Analaysis under tools and set the following settings:

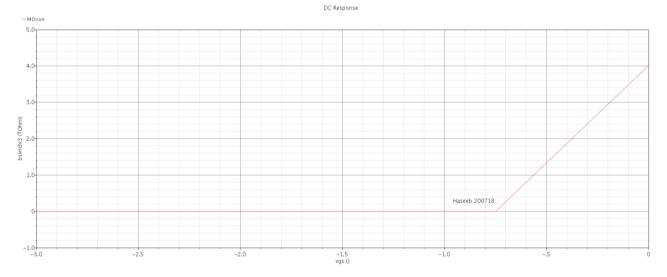


The following graph is obtained:



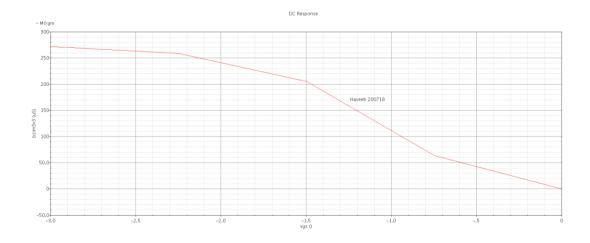
Graph Explanation: In parametric analysis we give a range of gate to source voltages Vgs from -3 to 0 volts. We will again subtract the threshold voltage Vth from all these different vgs voltages to get the points on the graph.

On the same analysis window go to dcopt-info and select Ron:



Graph Explanation: When the graph reaches the straight line is enters in Deep triode region which is achieved when Vds becomes less the 2 times overdrive voltage.(|Vds|<<2|Vov|)

Now we will plot the graph with gm on y axis and Vgs on X axis:



<u>Graph Explanation</u> : Gm = Slope of current				
CON	CLUSION			
In thi	s lab we studied different graphs related to Pmos characteristics. We also Plotted graphs			
	st current of Vds and Vgs and then calculated points and labeled them which			
deteri	mine the different regions of the mode of operation of the transistor.			