ELECENG 2EI4

Bonus Project

Instructor: Dr. Haddara

Muhammad Haseeb Aslam

aslamm14- 400449291

As a future member of the engineering profession, the student is responsible for performing the required work in an honest manner, without plagiarism and cheating. Submitting this work with my name and student number is a statement and understanding that this work is my own and adheres to the Academic Integrity Policy of McMaster University and the Code of Conduct of the Professional Engineers of Ontario. Submitted by [Muhammad Haseeb Aslam, 400449291]

Summary

This project focused on designing and implementing a 3-bit Digital-to-Analog Converter (DAC) capable of converting binary input values into proportional analog voltage outputs across a full-scale range of 0 to 5 volts. The system's foundation rested on a summing amplifier architecture, which effectively integrated the weighted digital inputs to generate the corresponding analog signal.

Ultimately, the project fulfilled its main objective by successfully facilitating digital-to-analog conversion within the intended voltage range. However, the resulting output revealed opportunities for further optimization, particularly in enhancing the accuracy and consistency of the analog voltage levels.

Design

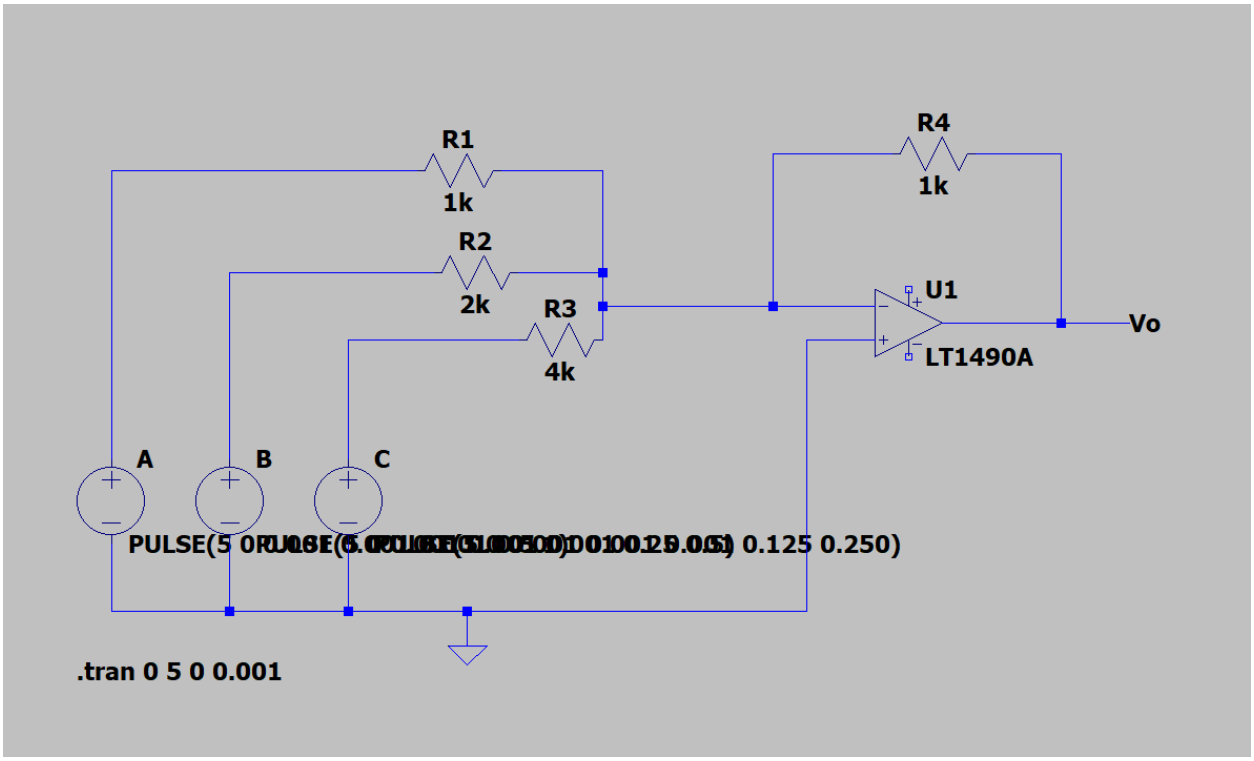

Figure 1: LTspice schematic

Netlist:

```
* C:\2cf3\Draft2.asc
X§U1 0 N001 NC_01 NC_02 Vo LT1490A
V§A N002 0 PULSE(5 0 0.001 0.001 0.001 0.5 1)
V§B N003 0 PULSE(5 0 0.001 0.001 0.001 0.25 0.5)
V§C N004 0 PULSE(5 0 0.001 0.001 0.001 0.125 0.250)
R1 N001 N002 1k
R2 N001 N003 2k
R3 N001 N004 4k
R4 Vo N001 1k
.tran 0 5 0 0.001
.lib LTC.lib
.backanno
.end
```

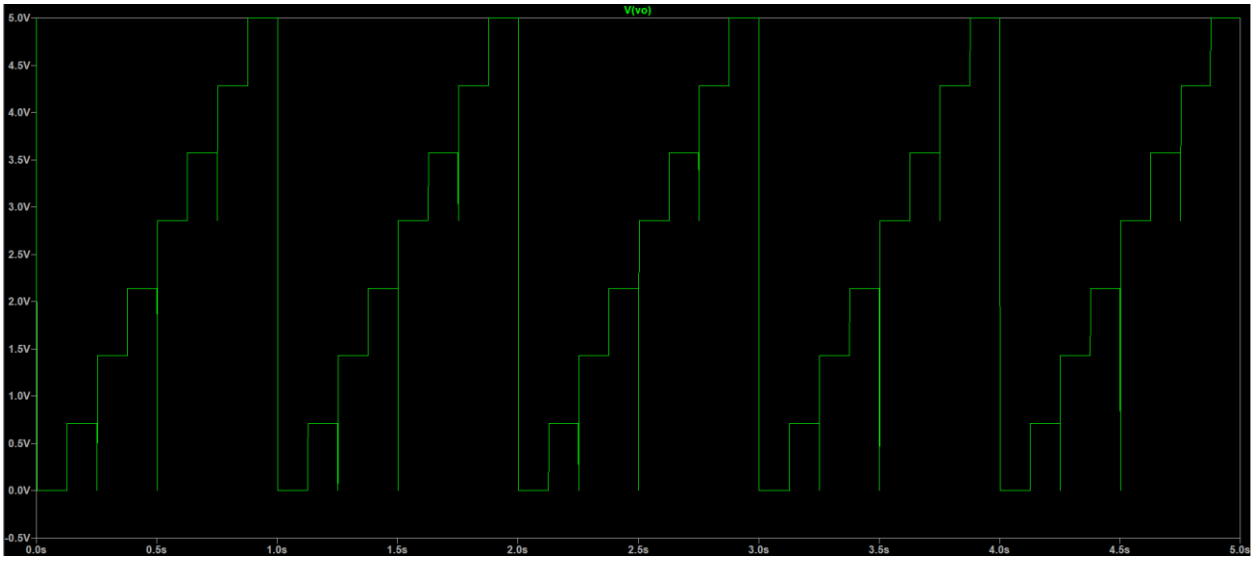

Figure 2: Circuit Output

The constructed circuit adopts a configuration akin to the traditional summing amplifier setup used with operational amplifiers. In this arrangement, three synchronized square wave inputs—each toggling between 0V (Low) and 5V (High)—were applied. To ensure every possible digital input combination occurred uniquely over time, the frequencies of the signals were staggered such that each one operated at twice the frequency (or half the period) of the preceding input.

One of the primary challenges encountered was determining the appropriate resistor ratios to achieve accurate analog output levels. As derived in the calculations section, the ideal voltage relationship was established as:

$$V_o = \frac{4V_A + 2V_B + V_C}{7}$$

To realize this behavior, resistors of 1 kΩ, 2 kΩ, 4 kΩ, and 10 kΩ were implemented. It was observed through testing that the resistor connecting the output voltage to the inverting input of the Op-Amp had no significant impact on the final output and was thus selected arbitrarily.

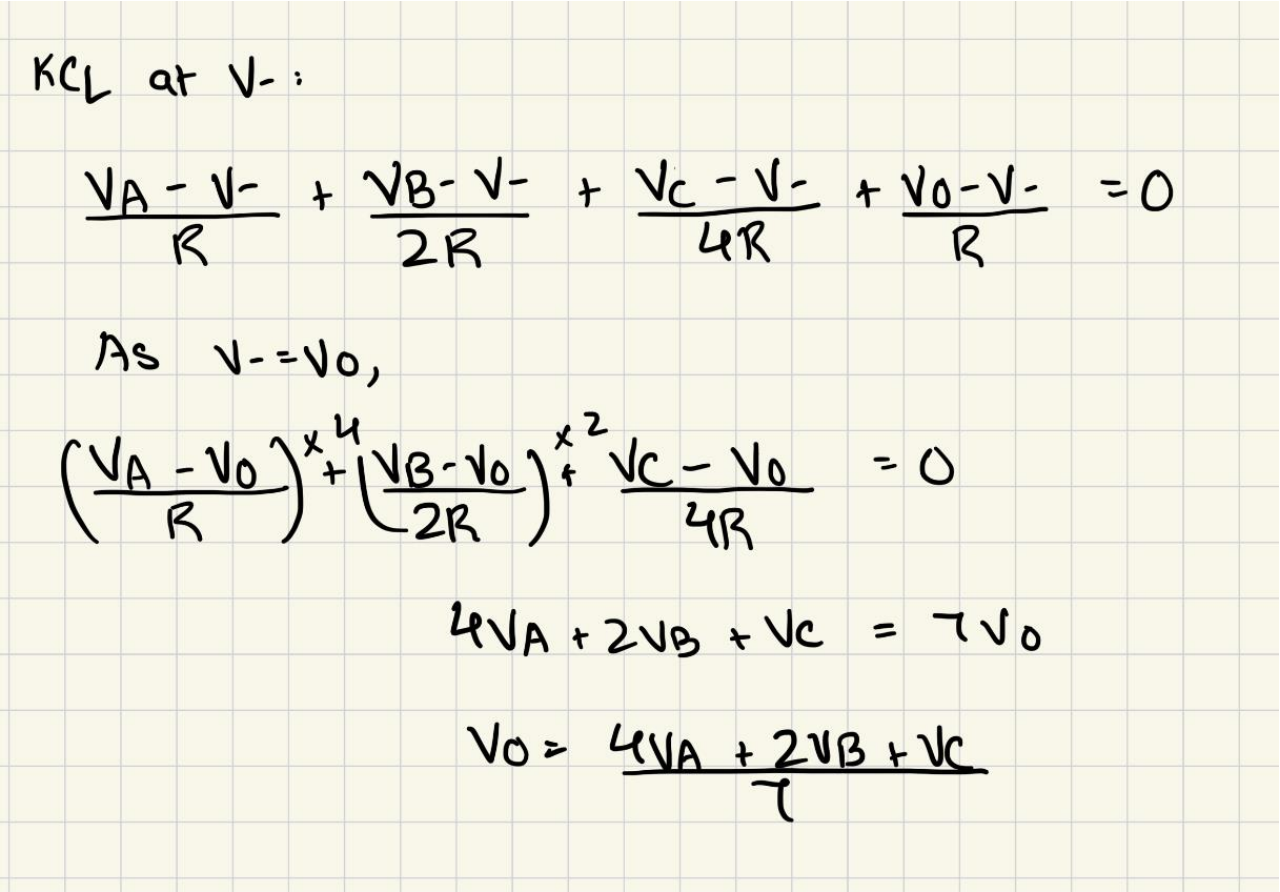

Figure 3: Calculations

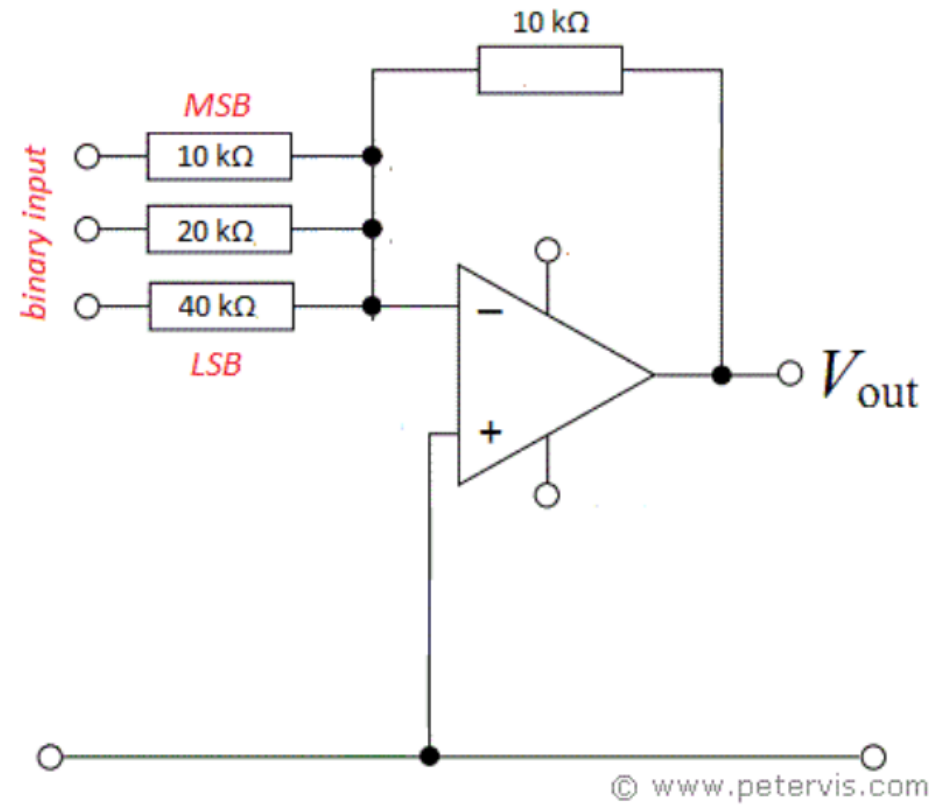

Figure 4: Design from the internet

This is a 3 input inverting summing amplifier with weighted inputs to make a 3-bit DAC circuit. This design was taken from an online education learning website (petervis) [1].

During the physical testing phase, a key limitation arose due to the AD2 device's inability to simultaneously generate more than two independent voltage waveforms, whereas the DAC design necessitated three distinct input signals. To address this constraint, a workaround was implemented: inputs B and C were driven by the available pulse waveforms, while input A was manually adjusted by toggling between static voltage levels. This method, known as Static Level testing, allowed for systematic observation of the circuit's response to all possible input combinations despite the hardware restriction.

Measurement and Analysis

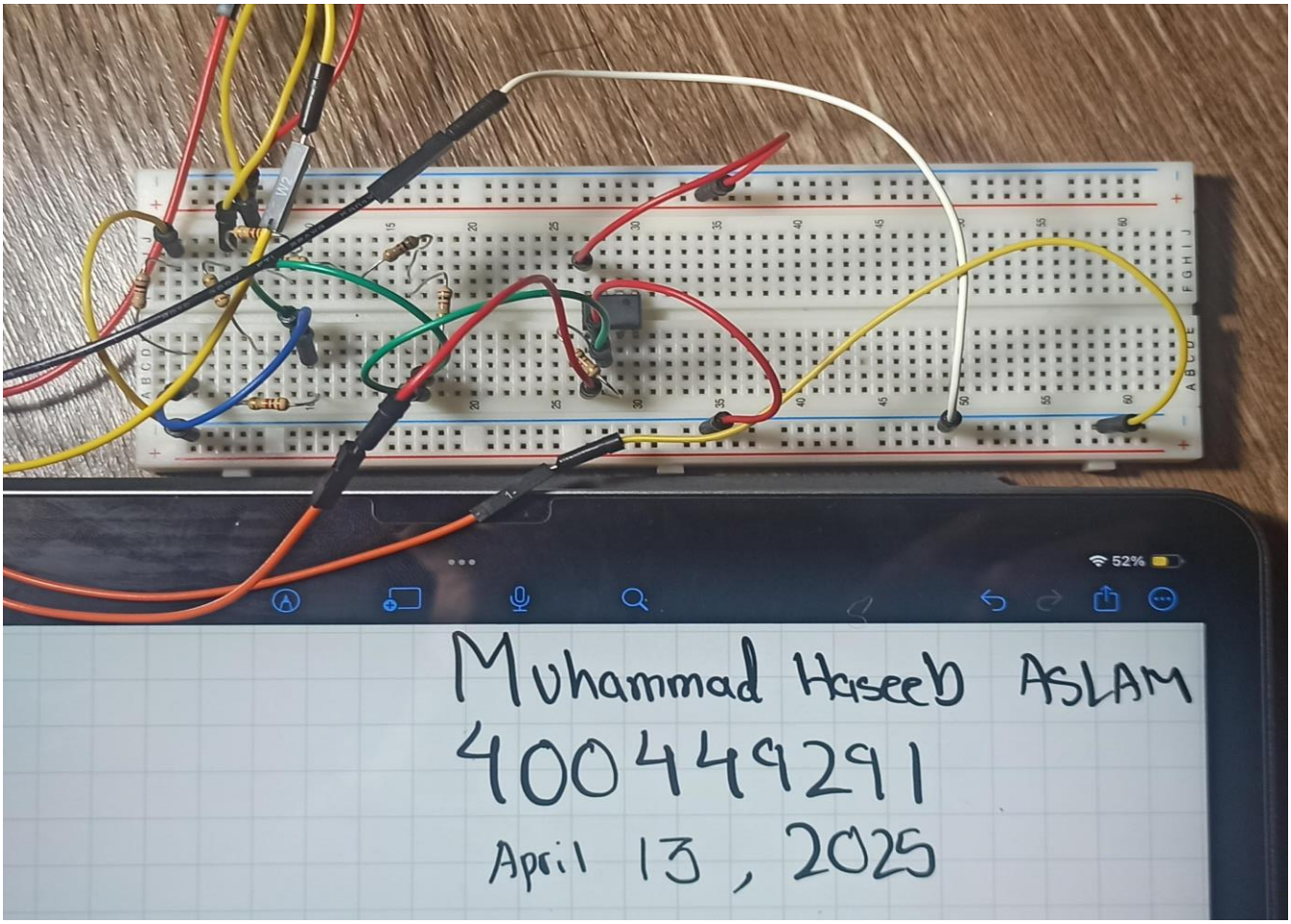

Figure 4: Real Circuit

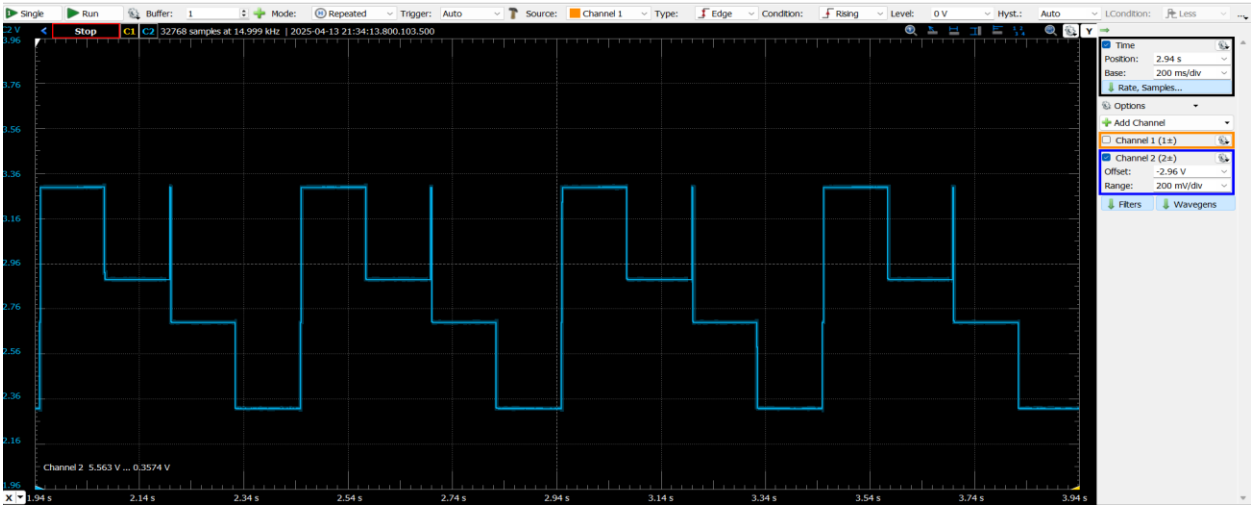

Figure 5: Output when input A is High

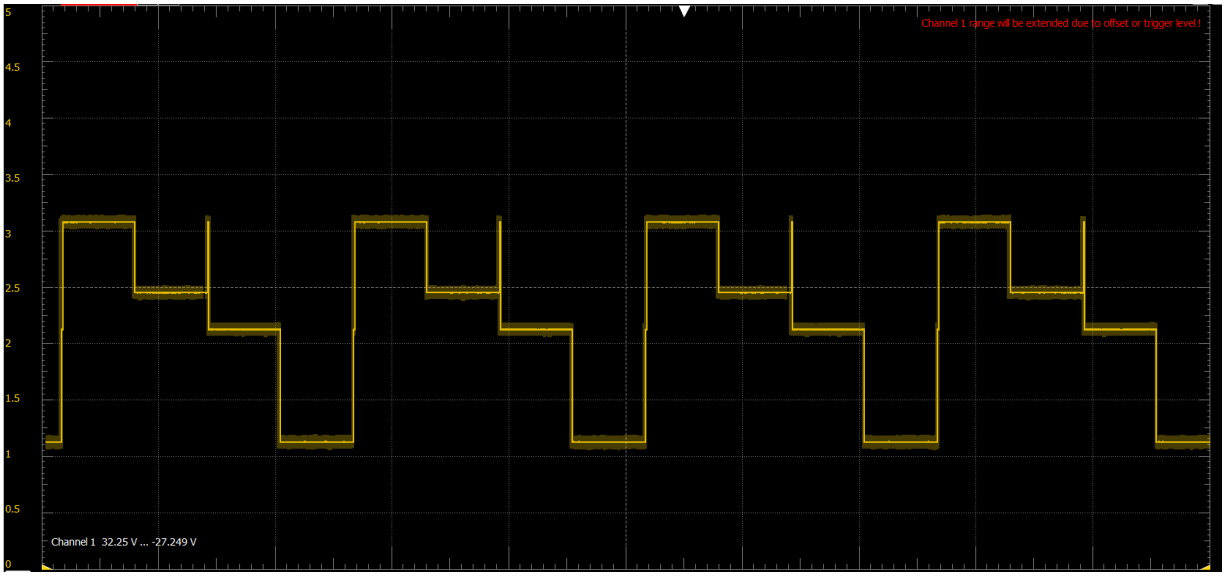

Figure 6: Output when input A is low

Here's a deeply rephrased version of your paragraph, with a proper calculation of the **maximum gain error** at the end:

Upon examining the overall shape of the output voltage graph, it is evident that while the voltage increments between digital steps are somewhat uneven, the trend still aligns with the expected behavior of a Digital-to-Analog Converter. However, a significant discrepancy emerges in the output voltage range. Specifically, the maximum observed output VmaxV_{\text{max}} was 3.30 V—considerably lower than the ideal 5 V full-scale value—and the minimum output VminV_{\text{min}} was 1.12 V instead of the expected 0 V. This compression of the output range indicates a **gain error**, which reflects how much the DAC's actual output range deviates from the ideal. The gain error is calculated using the formula:

$$\text{Gain Error} = \frac{Vmeasured - Vexpected}{Vexpected} * 100\%$$

For the digital input `111`, the expected output (for a full-scale 5V system) is 5.00 V, while the measured output was only 3.30 V. Plugging in these values:

$$\text{Gain Error} = \frac{3.3 - 5}{5} * 100\% = -34.0\%$$

Thus, the maximum gain error was approximately **–34.0%**, occurring at the `111` input code. This indicates that the DAC significantly underperformed at the upper end of its output range, likely due to limitations in the resistor network or supply constraints.

To calculate the **maximum Differential Non-Linearity (DNL)**, we begin by determining the actual voltage step between two adjacent digital input codes. In this case, we analyze the transition from digital code `110` to `111`. The measured analog output voltages are Vactual(110) = 2.88V and Vactual(111) = 3.30 V, giving us a step size of $\Delta V = 3.30 - 2.88 = 0.42$ V. Since this is a 3-bit DAC, the total number of output levels is 2^3 = 8, and the ideal Least Significant Bit (LSB) voltage step over a 0 – 5 V range is calculated as VLSB = $\frac{5}{7} \approx 0.714$ V. Using the DNL formula,

$$DNL = \frac{\Delta V}{V_{LSB}} - 1 = \frac{0.42}{0.714} - 1 = -0.412$$

This result means that the voltage step at this specific transition is approximately 0.412 LSB smaller than the ideal step size.

To measure the **offset error** of the DAC, we begin by examining the analog output corresponding to the lowest possible digital input—`000`. In an ideal 3-bit DAC with a 0–5 V range, this input should produce exactly 0 V. However, any deviation from this ideal value is defined as the **offset error**, which quantifies how much the entire output curve is shifted vertically from its intended position.

The offset error is calculated using the formula:

Offset Error=Vmeasured(000)

In this experiment, the measured output voltage for the digital input `000` was **1.12 V**, while the expected output was **0 V**. Substituting into the equation:

Offset Error=1.12 V−0 V=1.12 V

This result indicates a substantial offset error of **+1.12 V**, suggesting that the entire output range of the DAC is shifted upward by this amount. This error may stem from improper grounding, a misconfigured Op-Amp reference point, or inherent bias in the resistor network.

In essence, **offset error** is a measure of the DAC's ability to accurately represent the lowest output voltage. A large offset means that even when the digital input is zero, the DAC still outputs a significant voltage, which affects the accuracy of all subsequent outputs in the range.

Discussion

As previously observed, the actual voltage output range of the DAC was significantly compressed compared to the theoretical 0–5 V scale. With a measured output topping out at only 3.30 V, the system exhibited a **34% deviation** from the ideal full-scale value. Several contributing factors may account for this discrepancy:

1. **Resistor Tolerance Variability**: Even small manufacturing deviations from nominal resistor values can disrupt the delicate voltage-weighting ratios required for accurate DAC output, resulting in reduced gain.
2. **Non-Ideal Op-Amp Behavior**: Real-world Op-Amps introduce imperfections such as finite open-loop gain, input offset voltages, and limited output swing, all of which may skew the intended voltage levels.
3. **Digital Input Fluctuations**: Minor inconsistencies in the logic high/low levels or timing of input signals can propagate through the summing circuit, causing output instability or inaccuracy.
4. **Pre-DAC Circuit Distortions**: Any imperfections in the circuits that condition or feed signals into the DAC—such as buffers or voltage dividers—can introduce unintended voltage shifts, further amplifying gain errors.
5. **Measurement Tool Limitations**: Oscilloscope probes, signal analyzers, or data acquisition systems with calibration drift, noise, or insufficient precision can result in misleading voltage readings.
6. **Power Supply Irregularities**: Unstable or fluctuating supply voltages can impair Op-Amp performance, particularly its ability to reach output extremes, thereby capping the output voltage range.
7. **Thermal Sensitivity**: Heat affects resistor values and semiconductor performance. Temperature-dependent shifts in component characteristics can degrade precision over time or during long usage.

To address such sources of error, one should emphasize tight-tolerance components, robust power supply filtering, accurate signal generation, and systematic calibration protocols. Through careful design refinement and rigorous testing, the DAC's accuracy and stability can be significantly improved.

The DAC was intentionally built around a minimalist architecture that balances practical implementation with functional fidelity. A **resistor-based summing amplifier** was chosen for its clarity, accessibility, and educational value. This configuration offers a direct and intuitive method for converting multiple digital signals into a single, weighted analog output.

Prioritizing simplicity helped streamline the design process, making it easier to assemble, test, and troubleshoot using the resources and components available. The resistor network provided a modular structure, allowing for easy scaling or modification based on the number of bits or precision required.

By favoring this elegant approach, the project ensured not only that fundamental DAC behavior could be effectively demonstrated, but also that the system remained adaptable for future enhancements. The design promotes both learning and experimentation, offering a solid foundation for deeper exploration into analog signal processing and mixed-signal circuit design.

An alternative design using an R-2R ladder network offers improved precision and scalability compared to a weighted resistor summing amplifier, as it relies on only two resistor values, minimizing errors due to tolerance variation. Additionally, the R-2R ladder simplifies layout and is more consistent in performance across different bit resolutions.

References:

[1] Baker, R. J. (2005). *CMOS: Circuit Design, Layout, and Simulation* (2nd ed.). IEEE Press.