CO326 - Assignment 03

WRITE A SHORT FUNCTIONAL DESCRIPTION OF FOLLOWING ICS

74LS374: 3 STATE OCTAL D TYPE TRANSPARENT

According to the <u>Documentation of DM74LS374 : 3 State Octal D-Type Transparent Latches and Edge-Triggered Flip-Flops</u> designed for driving highly capacitive or relatively low impedance loads. Do not require additional interfaces or pull up components. They have the capability of connecting directly to and driving bus lines.

There are 8 latches or D flipflops in the IC. Having transparent D latches refers to enable G is high the Q output will follow the D data input. 8 latches are edge triggered for the positive edge of the clock. Internal operations in the latches and flipflops are not interfered to the output controls.

74LS244: 3 STATE OCTAL BUFFER/ LINE DRIVER

According to the <u>Documentation of DM74LS244</u>: 3 State Octal Buffer/<u>Line Driver</u> the implementation done to improve the performance in and PC board density of the circuit. Capable of connecting more similar types of ICs due to higher fanout. Improved noise rejection will be key functionality of the device helps identified the 3 states more efficient and having a higher accuracy.

This buffer is capable of isolating the input and the output. Like they are not interfered by each other. And also the line driver will improve the transmission of data.

74LS138:1 OF 8 DECODER / DEMULTIPLEXER

According to the <u>Documentation of 74LS138</u>: 1-OF-8 <u>DECODER/DEMULTIPLEXER</u> the implementation of the IC ensures the speed of the device in a higher manner by allowing bipolar memory addressing for selecting addresses. Schottky barrier ensures the speeding of the device as well as improving the compatibility of the device for TTL logic ICs

74LS245: OCTAL BIDIRECTIONAL TRANSCIEVER WITH 3 STATE INPUT OUTPUT

According to the <u>Documentation of 74LS245Octal bidirectional</u> transciever with 3 state input output ICs are designed for asynchronous two way communication between data busses. This implementation of the IC capable of isolating busses by checking pin outputs. (Reserved pins such DIR for input and OE(bar) for output.