German-Jordanian University
School of Electrical Engineering and Information Technology
Department of Computer Engineering

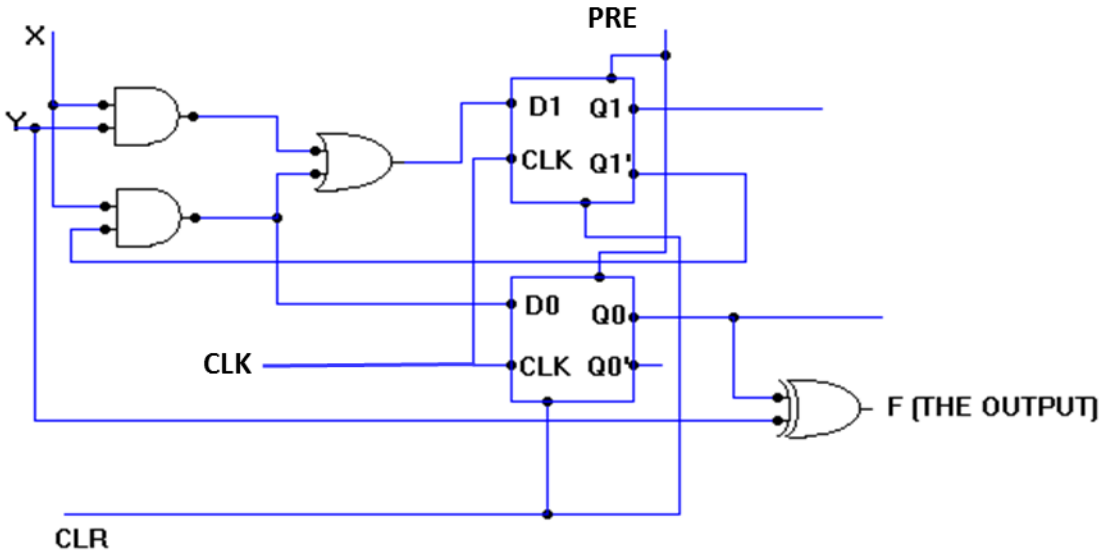
CE2120 - Digital Systems Lab
Lab 10

I. Objectives

The objective of this lab is to construct and analyze synchronous sequential circuits using state table and state transition diagram.

II. Preparations

1. Given the sequential circuit below:



   a. Determine whether the circuit above is a Mealy or a Moore machine.
   b. Construct the state transition table of this state machine.
   c. Construct the state graph of this state machine.

2. Draw the logic diagram of a 3-bit parallel in parallel out register with mode selection inputs S_0 and S_1. The register operates according to the following function table.

S_0	S_1	Register operation
0	0	No change
0	1	Complement outputs
1	0	Clear register to 0
1	1	Load parallel data

Use D-flip flops, 4:1 Multiplexers, and any combinational circuit that is required to implement the operations specified above. Identify your inputs, outputs, and control signals labels clearly.

III. Lab work

In this experiment:

a. Setup the circuits in part 1 on your breadboard and check its operation.
b. Setup the circuits in part 2 on your breadboard and check its operation.