German-Jordanian University
School of Electrical Engineering and Information Technology
Department of Computer Engineering

CE2120-Digital Systems Lab
Lab 9

I. Objectives

The objective of this lab is to become familiar with latches and clocked flip-flops, and building one F.F. using other type of F.F.'s.

II. Preparations

1. A characteristic equation gives the next state of a latch in terms of the inputs and the current state. Derive the characteristic equation for the J-K and the D latches, then find the following for both J-K and D latches:
    a. Build the next state table.
    b. Using the next state table in part a, construct a k-map for each latch and find its characteristic equation.
    c. Draw the logic circuit of each latch.

2. Convert a clocked D flip-flop (74LS74) to a clocked T flip-flop.
    a. Derive an expression for D in terms of T and Q.
    b. Draw the logic diagram of the circuit.

3. Convert a clocked D flip-flop (74LS74) to a clocked JK flip-flop.
    a. Derive an expression for D in terms of J, k and Q.
    b. Draw the logic diagram of the circuit.

4. Design a 3-bit synchronous counter 0➔1➔2➔4➔7 and back to zero. Obtain the state transition table and the K-Map's for each flip-flop input. Use JK flip-flop (74LS76, if not available use 74LS73). Draw the logic diagram of the counter

III. Lab work

In this experiment:

a. Setup the circuits in part 1 on your breadboard and check its operation.
b. Setup the circuits in part 2 on your breadboard and check its operation.
c. Setup the circuit in part 3, on your breadboard and check its operation.
d. Setup the circuit in part 4, on your breadboard and check its operation.