Digital Dice Roller: Theory of Operation

The circuit consists of two primary components: the **internal Dice_Roller module** and the **top-level Digital_Dice module**. The operations are detailed as follows:

1. Shared Clock Divider

- **Purpose**: A 24-bit counter (`slow_clock`) generates slower clock signals from the system clock for human-readable dice updates.
- **Implementation**: The slower signals (`slow_clock(23)` for Dice 1, `slow_clock(22)` for Dice 2) control the dice rolling frequency.
- **Design Choice**: Using a single clock divider for both dice minimizes hardware usage.

2. Dice_Roller (Internal Module)

- **Purpose**: Encapsulates the logic for rolling a single dice with values cycling from 1 to 6.
- **Implementation**: A counter increments on the slower clock when `roll` is active and resets to 1 if the counter reaches 6 or `reset` is triggered.
- **Design Choice**: This modular design ensures reusability, enabling integration of multiple dice.

3. Multiplexing Logic

- **Purpose**: Shares the 7-segment display between the two dice.
- **Implementation**: A 16-bit counter (`multiplexer_swap_clock`) alternates between displaying Dice 1 and Dice 2 values on the 7-segment display every 2000 cycles. The `digit_select` signal determines which dice value is shown.
- **Design Choice**: Multiplexing reduces hardware requirements by sharing the display.

Key Signals

Signal Name	Purpose
`reset`	Resets dice values and counters.
`roll`	Activates dice rolling.
`double_roll`	Enables rolling of the second dice.
`slow_clock`	Slower clock signals for dice updates.
`multiplexer_swap_clock`	Alternates display between Dice 1 and Dice 2.
`digit_select`	Indicates which dice value is currently displayed.
`dice1_value`, `dice2_value`	Values of the first and second dice, respectively.