Hashish Yenugula

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Education

Indian Institute of Technology, Hyderabad — Hyderabad, India
Bachelors in Electrical Engineering; CGPA: 8.94/10 — *Aug 2020 - June 2024*

Publications

Study of gate current in advanced MOS architectures
Gauhar, G.A., Chenchety, A., Yenugula, H., Georgiev, V., Asenov, A., Badami, O., Solid-State Electronics (2022)

Experience

Qualcomm — Banaglore, India
Founding Member — *Jun 2024 - Present*

- Working in SoC Integration team. Hands on clock divergence and SoC partition for design optimization

DriveEz — Hyderabad, India
Founding Member — *Aug 2023 - Present*

- Co-founded DrivEz, a startup with a mission to organize driving schools in India. Working on operations, research, and strategies. Secured 1st place in a prestigious competition hosted by ISB, Hyderabad

ACSIED Lab - SmartKosh Technologies — IIT Hyderabad, India
Incubation at IIT Hyderabad - Digital Design Intern — *Sep 2023 - Nov 2023*

- Worked on Battery Management System (BMS) on configuring and documentation of ARM M3 processor within the SSE-050 subsystem provided by ARM.

Qualcomm — Bangalore, India
Interim Engineering Intern - SoC Integration — *Jan 2023 - June 2023*

- Worked on integration of IP cores for two SoCs - including connectivity of major IPs like CPU and MMU.
- Used multiple stages of checks on the final design and understood thorough validation of integration.
- Experience with protocols like AHB, APB, AXI, Q-channel interface.
- Automated Qualcomm's in-house tool for generating SoC UPF and CPF by developing Python scripts. Additionally, developed an algorithm to generate YAML files based on input clock frequency YAML file using Python.

KNM Tech — IIT Hyderabad, India
Incubation at IIT Hyderabad - Analog Design Intern — *Sep 2022 - Nov 2022*

- Played a pivotal role in the testing of piezoelectric accelerometers by utilizing separately ordered components. Successfully assembled a prototype, showcasing proficiency in PCB design.

Projects

- Implemented CORDIC division, sine and cosine values, Newton-Raphson method, and an FIR filter in Verilog.
- Designed an AMBA AHB-APB master-slave interface in Verilog.

Relevant Courses

Analog and Digital Electronics: Digital Systems, Analog Electronics Lab, Intro to VLSI Technology, Semiconductor Device Modeling, Digital IC Design

Signal Processing: Signals and Systems, Digital Signal Processing, Communication Systems, Concentration Inequalities, Topics in Data Storage

Core Fundamentals: Circuit and Network Analysis, Semiconductor Device Fundamentals, Control Systems, Engineering Electromagnetics, EM Wave Propagation, Electrical Circuits Lab, Electronic Devices and Circuits Lab

Skills

Programming Languages: Verilog, System Verilog, C/C++, Python, MATLAB

Simulation Tools: Cadence Power Intent, NgSpice, LtSpice, KiCAD, ABACUS (nanohub)