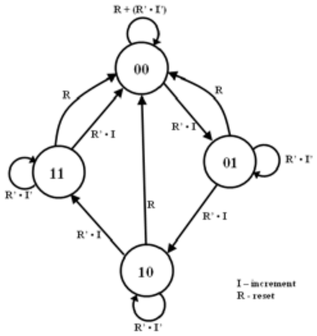
David DeGraw
Lab 8: 4x7 Segment Controller
3/10/2015



I	Q1	Q0	Q1+	Q0+
0	0	0	0	0
0	0	1	0	1
0	1	0	1	0
0	1	1	1	1
1	0	0	0	1
1	0	1	1	0
1	1	0	1	1
1	1	1	0	0

Q1+	inc		
Q1Q0		0	1
	00	0	0
	01	0	1
	11	1	0
	10	1	1

$Q1+ = (Q1'Q0) + (I'Q1) + (IQ1'Q0)$

Q0+	inc		
Q1Q0		0	1
	00	0	1
	01	1	0
	11	1	0
	10	0	1

$Q0+ = (I'Q0) + (IQ0')$

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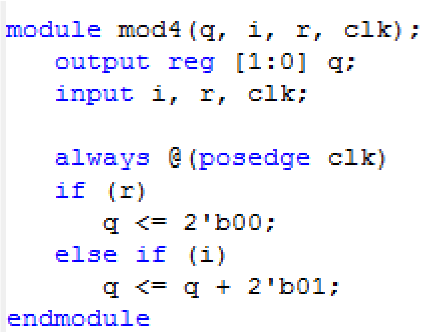
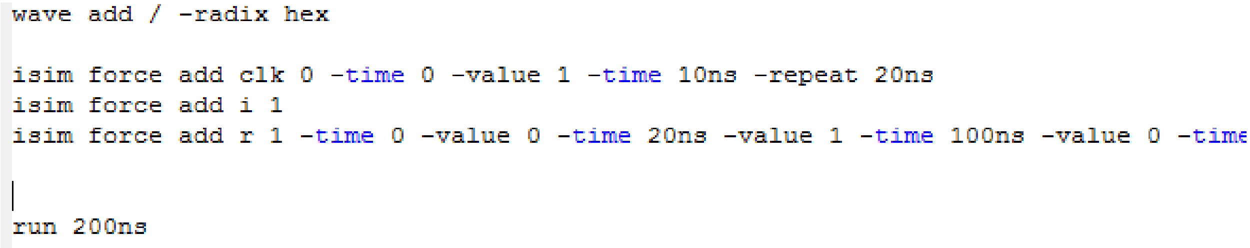
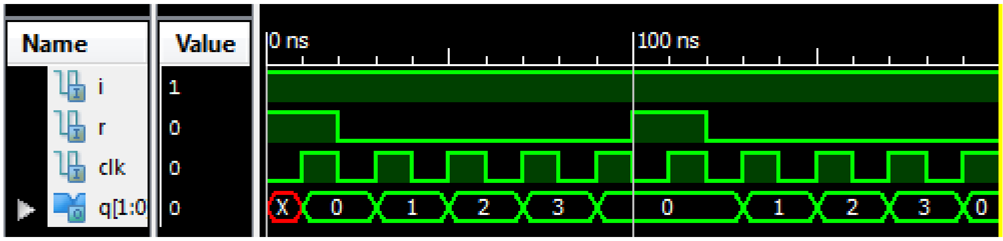
MOD4:



```
module mod4(q, i, r, clk);
   output reg [1:0] q;
   input i, r, clk;

   always @(posedge clk)
   if (r)
      q <= 2'b00;
   else if (i)
      q <= q + 2'b01;
endmodule
```



```
wave add / -radix hex

isim force add clk 0 -time 0 -value 1 -time 10ns -repeat 20ns
isim force add i 1
isim force add r 1 -time 0 -value 0 -time 20ns -value 1 -time 100ns -value 0 -time

|
run 200ns
```



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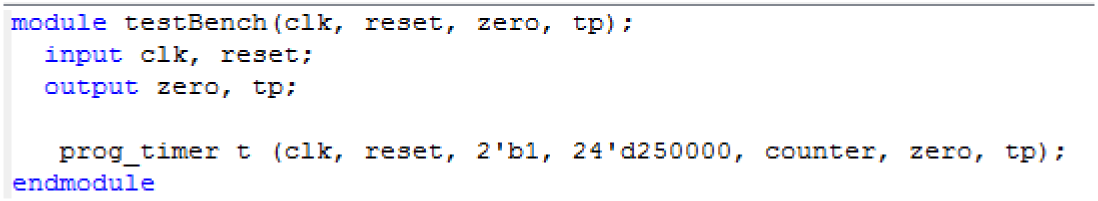
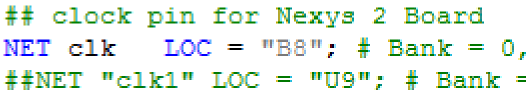
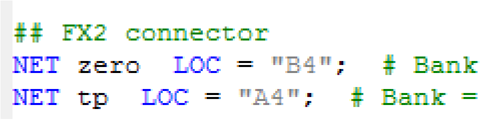
Programmable Timer:



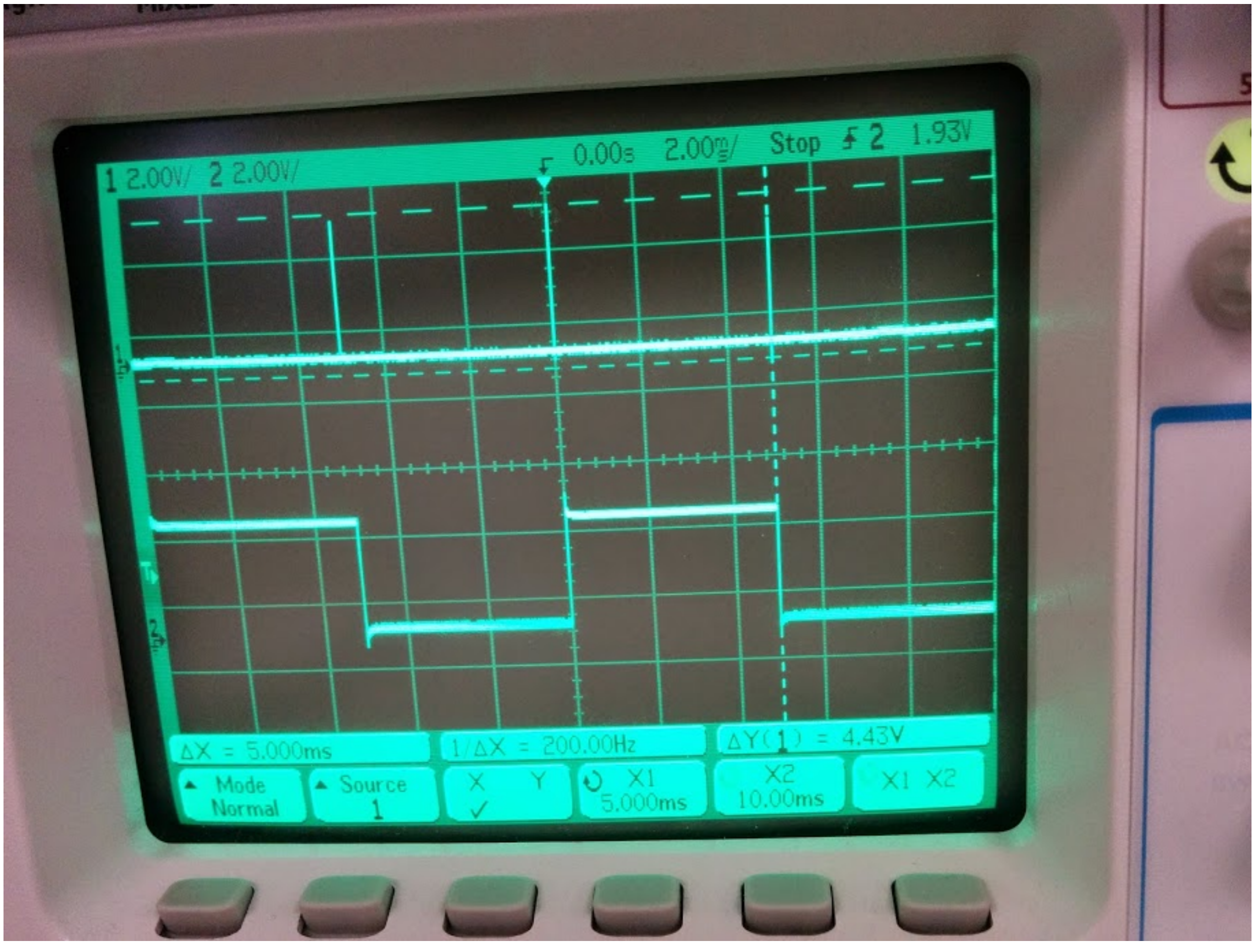
```
module testBench(clk, reset, zero, tp);
  input clk, reset;
  output zero, tp;

   prog_timer t (clk, reset, 2'b1, 24'd250000, counter, zero, tp);
endmodule
```



```
## clock pin for Nexys 2 Board
NET clk   LOC = "B8"; # Bank = 0,
##NET "clk1" LOC = "U9"; # Bank =
```



```
## FX2 connector
NET zero  LOC = "B4";  # Bank
NET tp  LOC = "A4";  # Bank =
```



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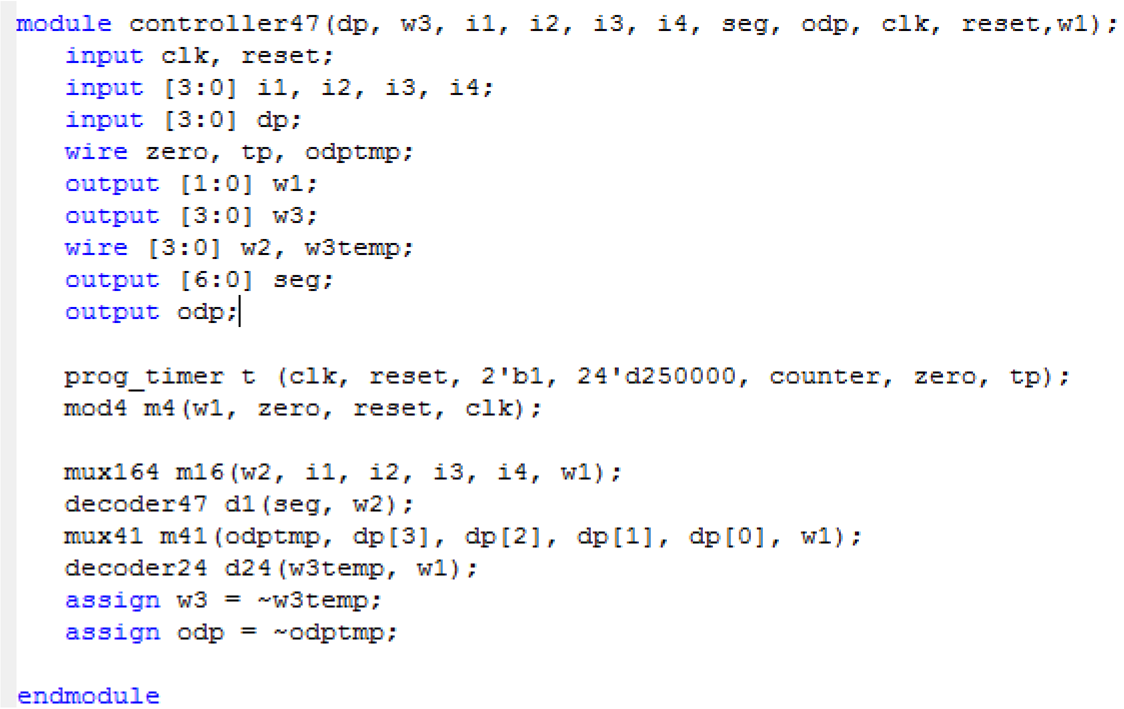
4x7 & Test Bench:

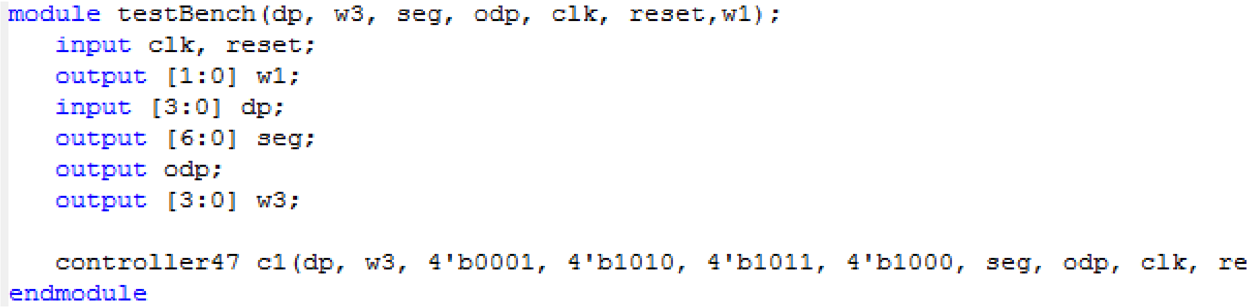


```
module controller47(dp, w3, i1, i2, i3, i4, seg, odp, clk, reset,w1);
   input clk, reset;
   input [3:0] i1, i2, i3, i4;
   input [3:0] dp;
   wire zero, tp, odptmp;
   output [1:0] w1;
   output [3:0] w3;
   wire [3:0] w2, w3temp;
   output [6:0] seg;
   output odp;

   prog_timer t (clk, reset, 2'b1, 24'd250000, counter, zero, tp);
   mod4 m4(w1, zero, reset, clk);

   mux164 m16(w2, i1, i2, i3, i4, w1);
   decoder47 d1(seg, w2);
   mux41 m41(odptmp, dp[3], dp[2], dp[1], dp[0], w1);
   decoder24 d24(w3temp, w1);
   assign w3 = ~w3temp;
   assign odp = ~odptmp;

endmodule
```



```
module testBench(dp, w3, seg, odp, clk, reset,w1);
   input clk, reset;
   output [1:0] w1;
   input [3:0] dp;
   output [6:0] seg;
   output odp;
   output [3:0] w3;

   controller47 c1(dp, w3, 4'b0001, 4'b1010, 4'b1011, 4'b1000, seg, odp, clk, re
endmodule
```

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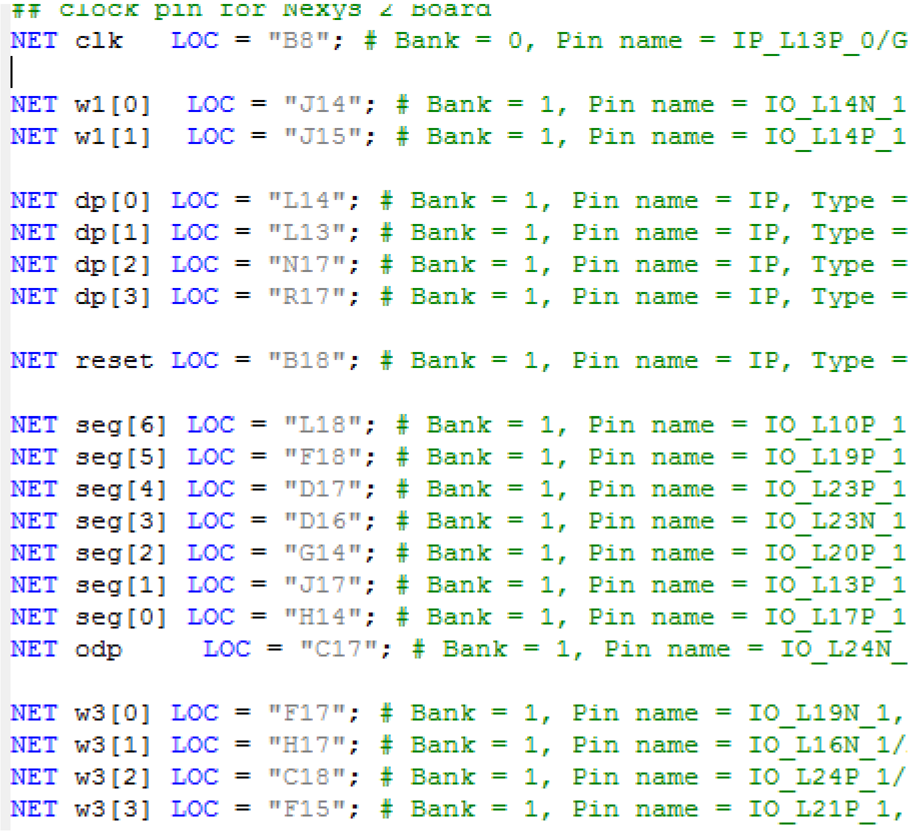

```
## Clock pin for Nexys 2 Board
NET clk   LOC = "B8"; # Bank = 0, Pin name = IP_L13P_0/G

NET w1[0]  LOC = "J14"; # Bank = 1, Pin name = IO_L14N_1
NET w1[1]  LOC = "J15"; # Bank = 1, Pin name = IO_L14P_1

NET dp[0] LOC = "L14"; # Bank = 1, Pin name = IP, Type =
NET dp[1] LOC = "L13"; # Bank = 1, Pin name = IP, Type =
NET dp[2] LOC = "N17"; # Bank = 1, Pin name = IP, Type =
NET dp[3] LOC = "R17"; # Bank = 1, Pin name = IP, Type =

NET reset LOC = "B18"; # Bank = 1, Pin name = IP, Type =

NET seg[6] LOC = "L18"; # Bank = 1, Pin name = IO_L10P_1
NET seg[5] LOC = "F18"; # Bank = 1, Pin name = IO_L19P_1
NET seg[4] LOC = "D17"; # Bank = 1, Pin name = IO_L23P_1
NET seg[3] LOC = "D16"; # Bank = 1, Pin name = IO_L23N_1
NET seg[2] LOC = "G14"; # Bank = 1, Pin name = IO_L20P_1
NET seg[1] LOC = "J17"; # Bank = 1, Pin name = IO_L13P_1
NET seg[0] LOC = "H14"; # Bank = 1, Pin name = IO_L17P_1
NET odp     LOC = "C17"; # Bank = 1, Pin name = IO_L24N_

NET w3[0] LOC = "F17"; # Bank = 1, Pin name = IO_L19N_1,
NET w3[1] LOC = "H17"; # Bank = 1, Pin name = IO_L16N_1/
NET w3[2] LOC = "C18"; # Bank = 1, Pin name = IO_L24P_1/
NET w3[3] LOC = "F15"; # Bank = 1, Pin name = IO_L21P_1,
```

Anomalies:

I had my segments in reverse order which was a really confusing bug.