In this PRAM simulation

The cells dimensions in @D schematic design:

Top Electrode (W): height (10 nm), Weight (20 nm)

Bottom electrode (W): height (5 nm), Weight (10 nm)

C-GST Layer (Phase change layer) : height (20 nm), Weight (20 nm)

Mos2 mono layer under C-GST besides heater : height (5 nm), Weight (1 nm)

Heater (TiN): height (10 nm), Weight (5 nm)

Si2N4 dielectric Layer: (height 60 nm, weight (25 nm)

RESET State applied Voltage (1.2V) : Temperature at C-GST Layer 0.98 at ns: 954K

SET State applied Voltage (0.8V) : Temperature at C-GST Layer at 0.7 ns: 461 K

Material Properties :

TiN :

Material type:

Solid

Material Contents

Property	Variable	Value	Unit	Property group
Electrical conductivity	sigma_is...	1.5e6	S/m	Basic
Heat capacity at constant pressure	Cp	540	J/(kg·K)	Basic
Relative permittivity	epsilonr_i...	20	1	Basic
Density	rho	5200	kg/m^3	Basic
Thermal conductivity	k_iso ; kii...	30	W/(m·K)	Basic

Fig. 1: TiN material properties

Tungsten (W):

Material

Material Contents

Property	Variable	Value	Unit	Property group
Thermal conductivity	k_iso ; kii...	170	W/(m·K)	Basic
Heat capacity at constant pressure	Cp	133.9776	J/(kg·K)	Basic
Electrical conductivity	sigma_is...	2e7	S/m	Basic
Density	rho	19250	kg/m³	Basic
Relative permittivity	epsilonr_...	6.2438	1	Basic
Resistivity	res_iso ; r...	res_solid_1(...	Ω·m	Basic
Surface emissivity	epsilon_r...	epsilon(T[1...	1	Basic
Coefficient of thermal expansion	alpha_is...	(alpha_soli...	1/K	Basic
Seebeck coefficient	S_iso ; Sii...	7.5e-6	V/K	Basic

Fig. 2: W material properties

Si3N4:

Material

Material Contents

Property	Variable	Value	Unit	Property group
Thermal conductivity	k_iso ; kii...	k(T[1/K])[W...	W/(m·K)	Basic
Heat capacity at constant pressure	Cp	0.7e6	J/(kg·K)	Basic
Density	rho	rho(T[1/K])...	kg/m³	Basic
Relative permittivity	epsilonr_...	1	1	Basic
Electrical conductivity	sigma_is...	1e-16	S/m	Basic
Coefficient of thermal expansion	alpha_is...	(alpha_soli...	1/K	Basic
Seebeck coefficient	S_iso ; Sii...	50e-6	V/K	Basic
Tangent coefficient of thermal expansion	alphatan...	CTE_solid_...	1/K	Thermal expansion
Thermal strain	dL_iso ;...	(dL_solid_p...	1	Thermal expansion

Fig. 3: Si3N4 Material properties

Mos2 Mono Layer:

Material type:

Solid

Material Contents

Property	Variable	Value	Unit	Property group
Relative permittivity	epsilonr_...	3.3	1	Basic
Electrical conductivity	sigma_is...	10	S/m	Basic
Thermal conductivity	k_iso ; kii...	35	W/(m·K)	Basic
Density	rho	5060	kg/m³	Basic
Heat capacity at constant pressure	Cp	373	J/(kg·K)	Basic

Fig. 4: Mos2 monolayer material properties

C-GST amorphious state:

Material type:

Solid

Material Contents

Property	Variable	Value	Unit	Property group
Electrical conductivity	sigma...	4.5e3	S/m	Basic
Heat capacity at constant pres...	Cp	205	J/(kg·K)	Basic
Relative permittivity	epsilo...	25	1	Basic
Thermal conductivity	k_iso ;...	0.30	W/(m·...	Basic
Density	rho	6000	kg/m³	Basic
Resistivity	res_is...	0.33333...	Ω·m	Basic
Seebeck coefficient	S_iso ;...	90e-6	V/K	Basic

Fig. 5: C-GST material crystallization state properties

C-GST crystalline state:

Material type:

Solid

Material Contents

	Property	Variable	Value	Unit	Property group
☑	Electrical conductivity	sigma_is...	8e3	S/m	Basic
☑	Heat capacity at constant pressure	Cp	205	J/(kg·K)	Basic
☑	Relative permittivity	epsilonr_i...	35	1	Basic
☑	Thermal conductivity	k_iso ; kii...	0.30	W/(m·K)	Basic
☑	Density	rho	6300	kg/m^3	Basic
	Resistivity	res_iso ; r...	0.333333333...	Ω·m	Basic
	Seebeck coefficient	S_iso ; Sii...	90e-6	V/K	Basic

Fig. 6: C-GST material amorphous state properties

Multiphysics and equations used in this simulation:

1. Electric Current:

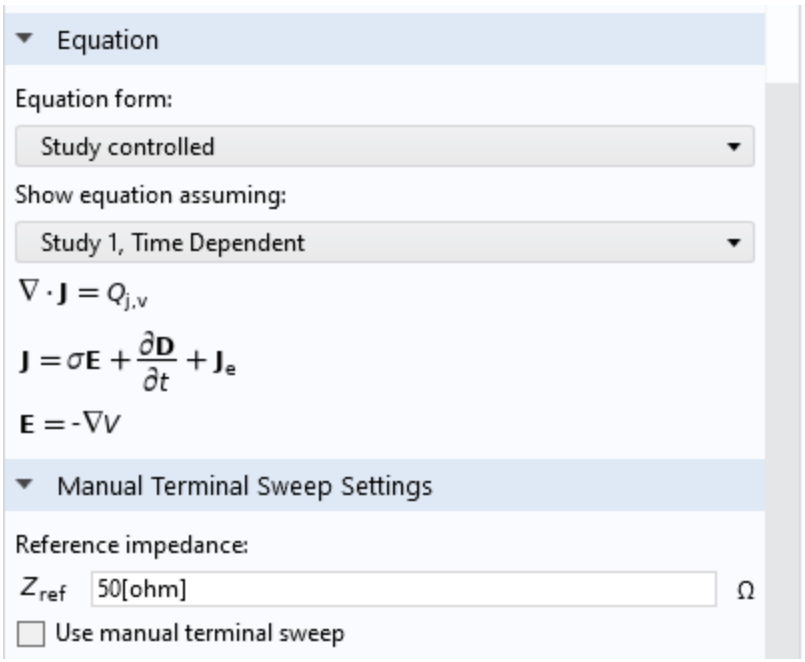


Fig. 7: Electric Current physics and equations

Electric Current 2: Electric insulation

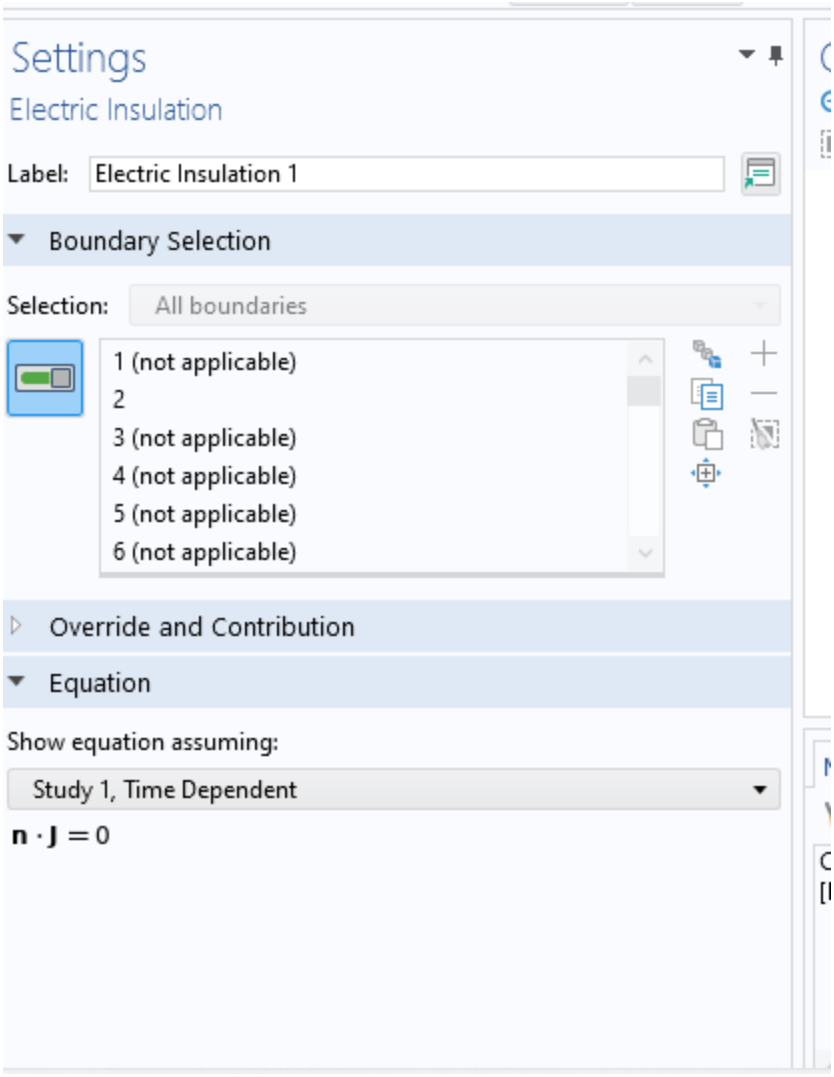


Fig. 8: Electric isolation physics and equations

2. Heat Transfer in solids:

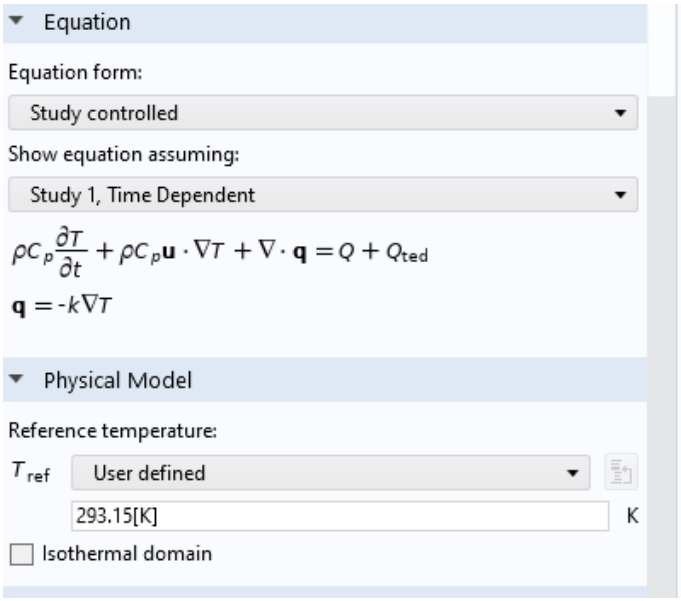


Fig. 9: Heat Transfer in solids physics and equations

Thermal insulation:
-n.q=0

Temperature:
$T=T_0$

Diffuse Surface:

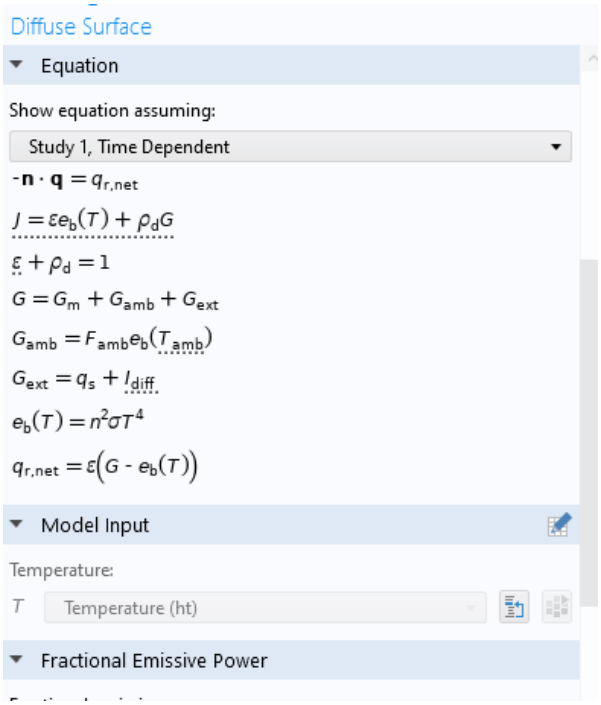


Fig. 10: Diffusive surface physics and equations

3. Electric Circuits: (Ground Node, Voltage Source, Resistor R_L, External I vs U) used

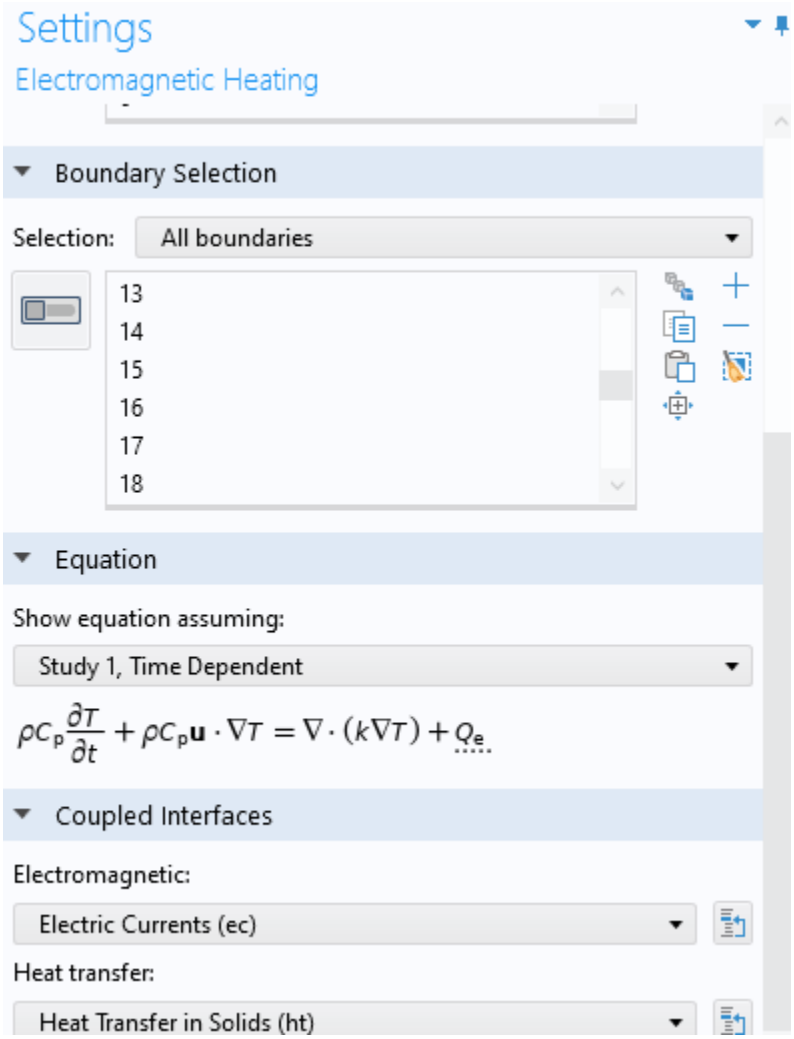


Fig. 11: Electric Circuits: (Ground Node, Voltage Source, Resistor R_L, External I vs U) used and equations

Study 1: Time dependent solver

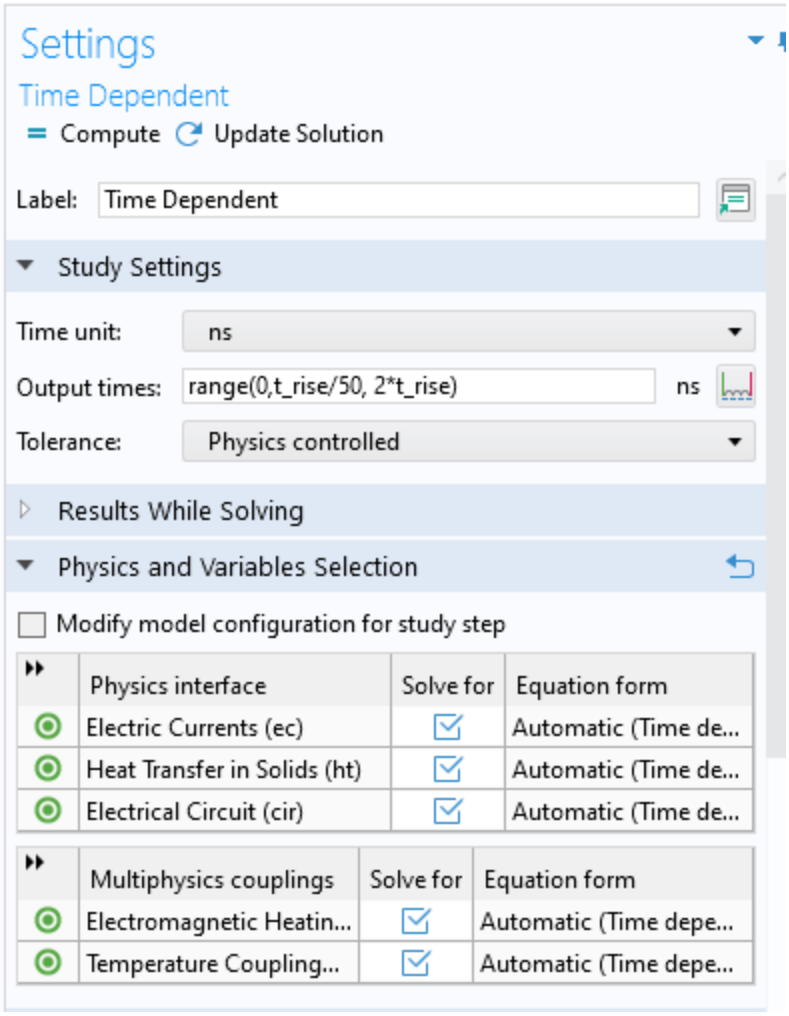


Fig. 12: Study 1: Time dependent solver

Results :

Electric potential crystallization State :

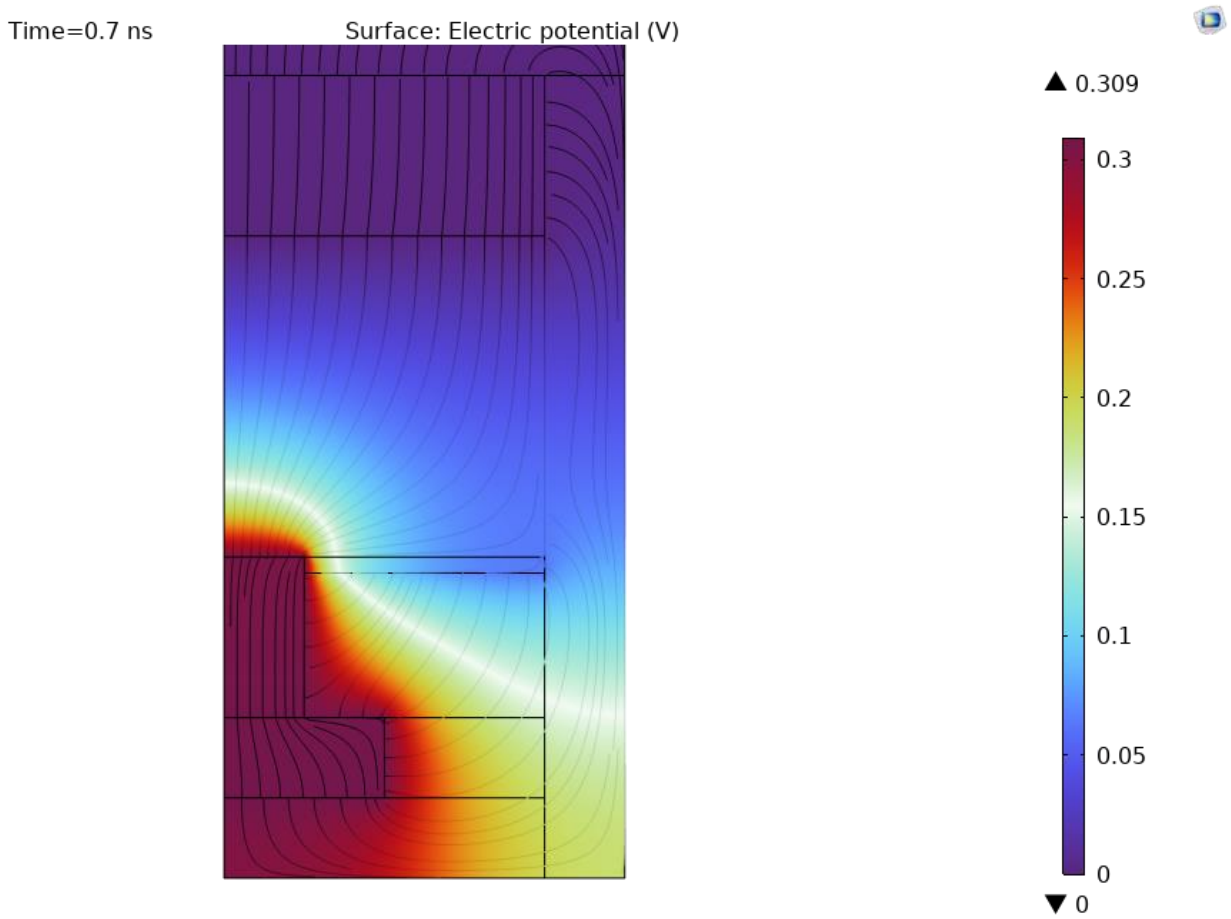


Fig. 13: Electric potential crystallization State at 0.8V applied voltage, R_L = 1K ohm, ti, time: 0.7 ns

Electric potential amorphous State :

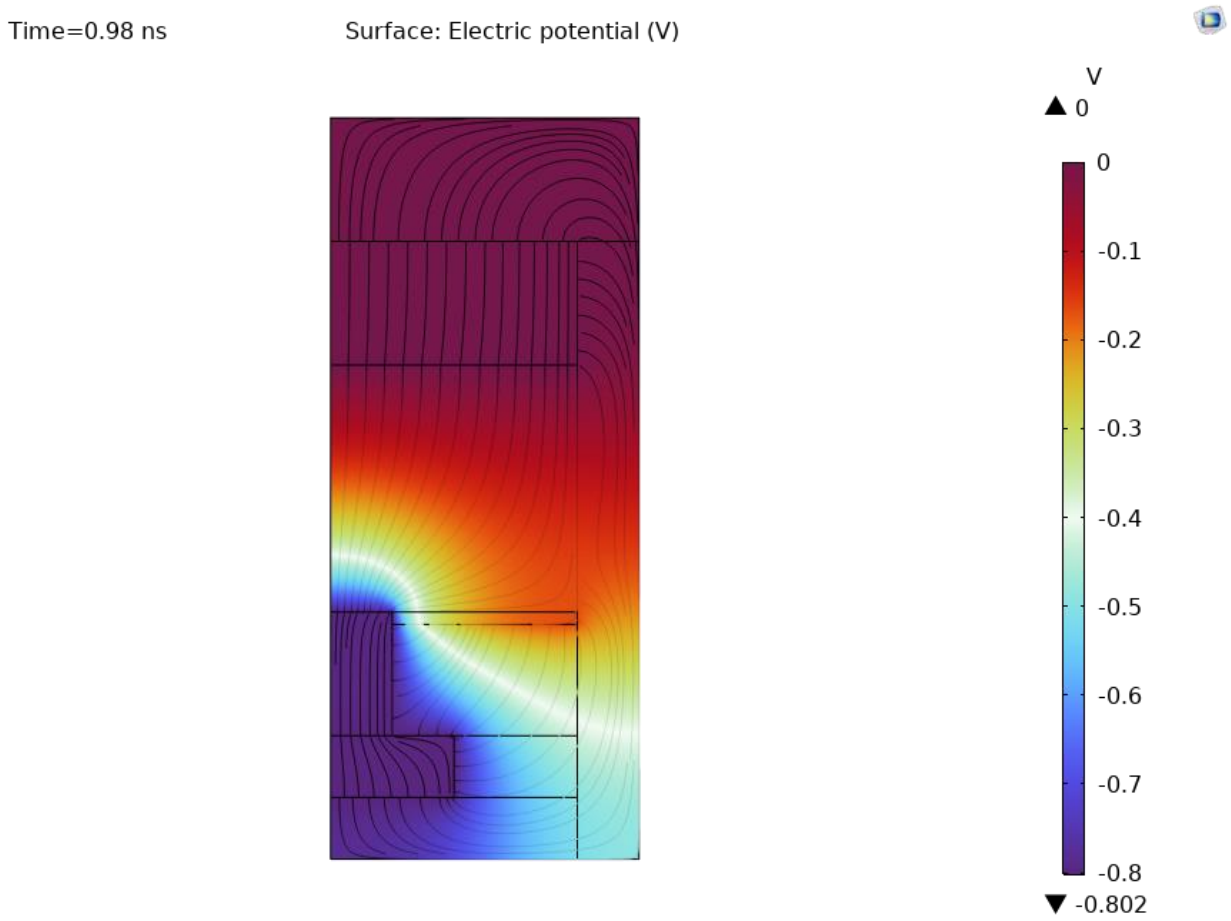


Fig. 14: Electric potential amorphous State at 1.2 V applied voltage, R_L = 1K ohm, ti, time: 0.98 ns

Electric field Norm crystallization stare:

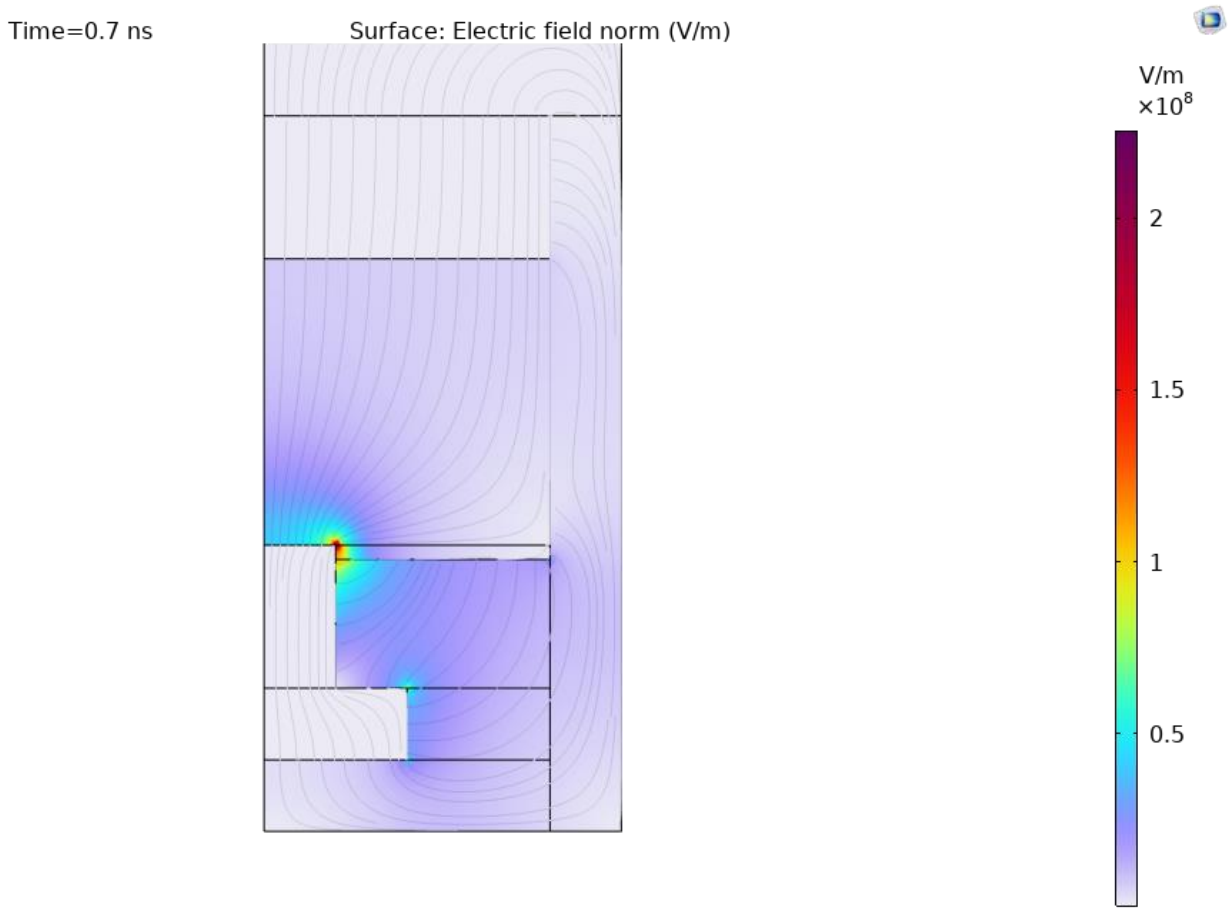


Fig. 15: Electric Field norm crystallization State at 0.8V applied voltage, R_L = 1K ohm, ti, time: 0.7 ns

Electric field Norm amorphous stare:

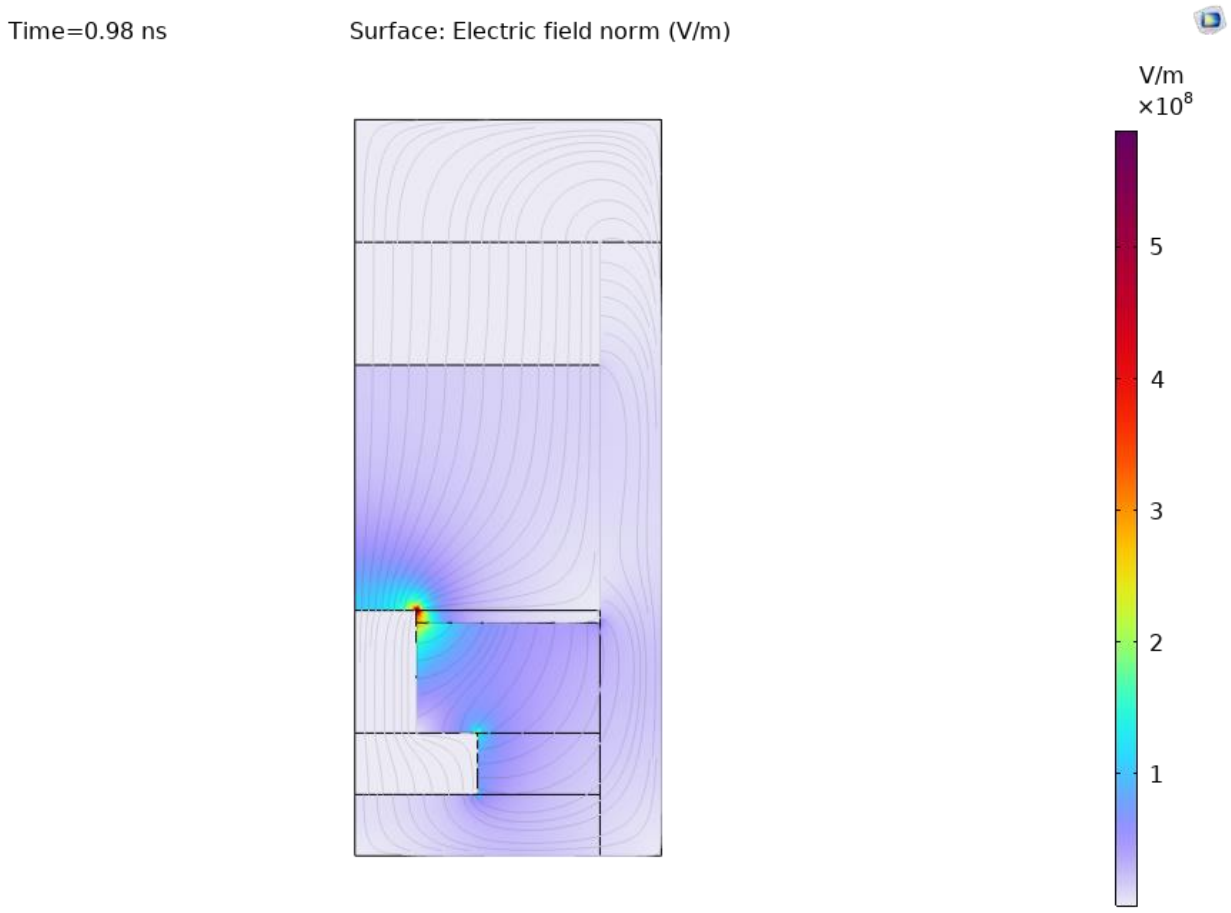


Fig. 16: Electric Field norm amorphous State at 1.2 V applied voltage, R_L = 1K ohm, ti, time: 0.98 ns

Isothermal Contour Crystalline State:

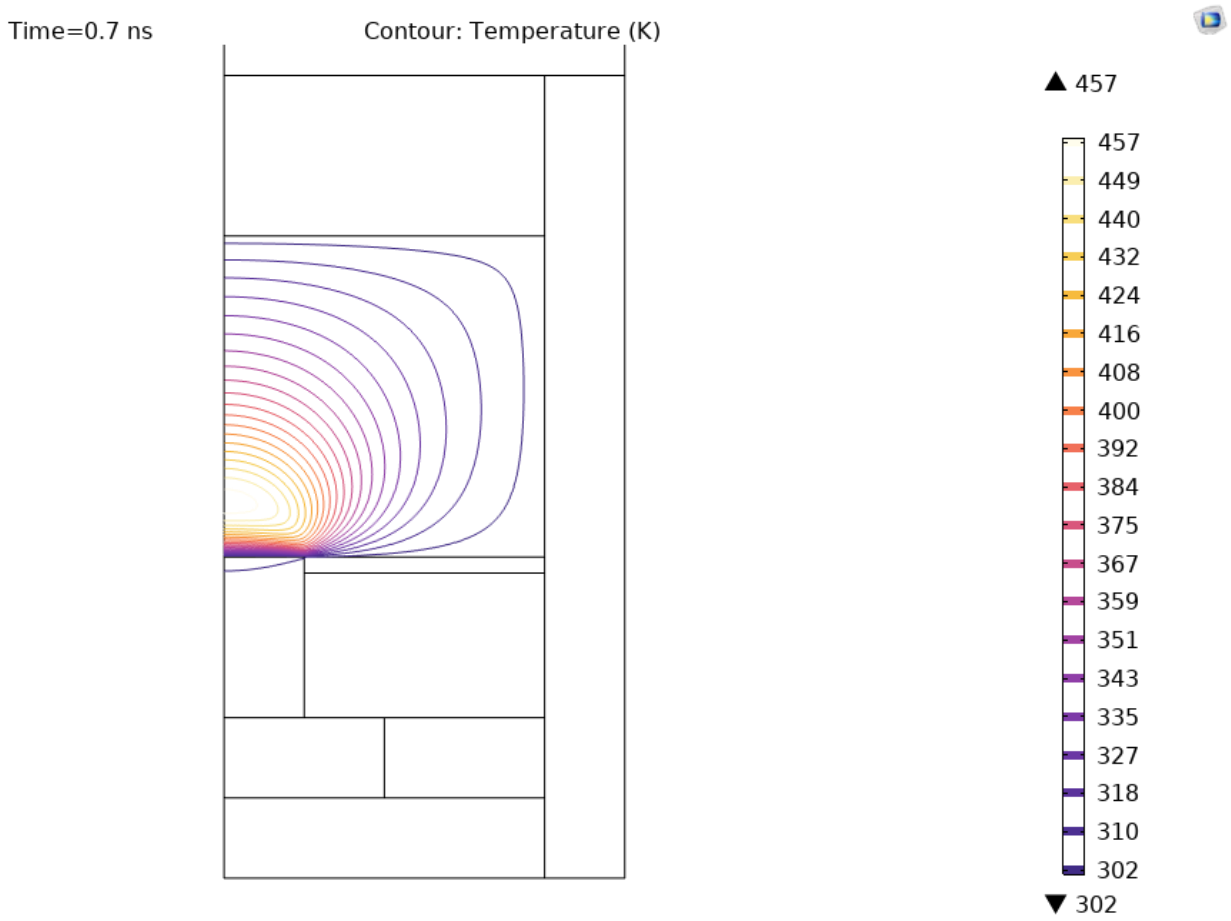


Fig. 17: Isothermal Contour (Temperature) Crystalline State at 1.2 V applied voltage, R_L = 1K ohm, ti, time: 0.98 ns

Isothermal Contour amorphous State:

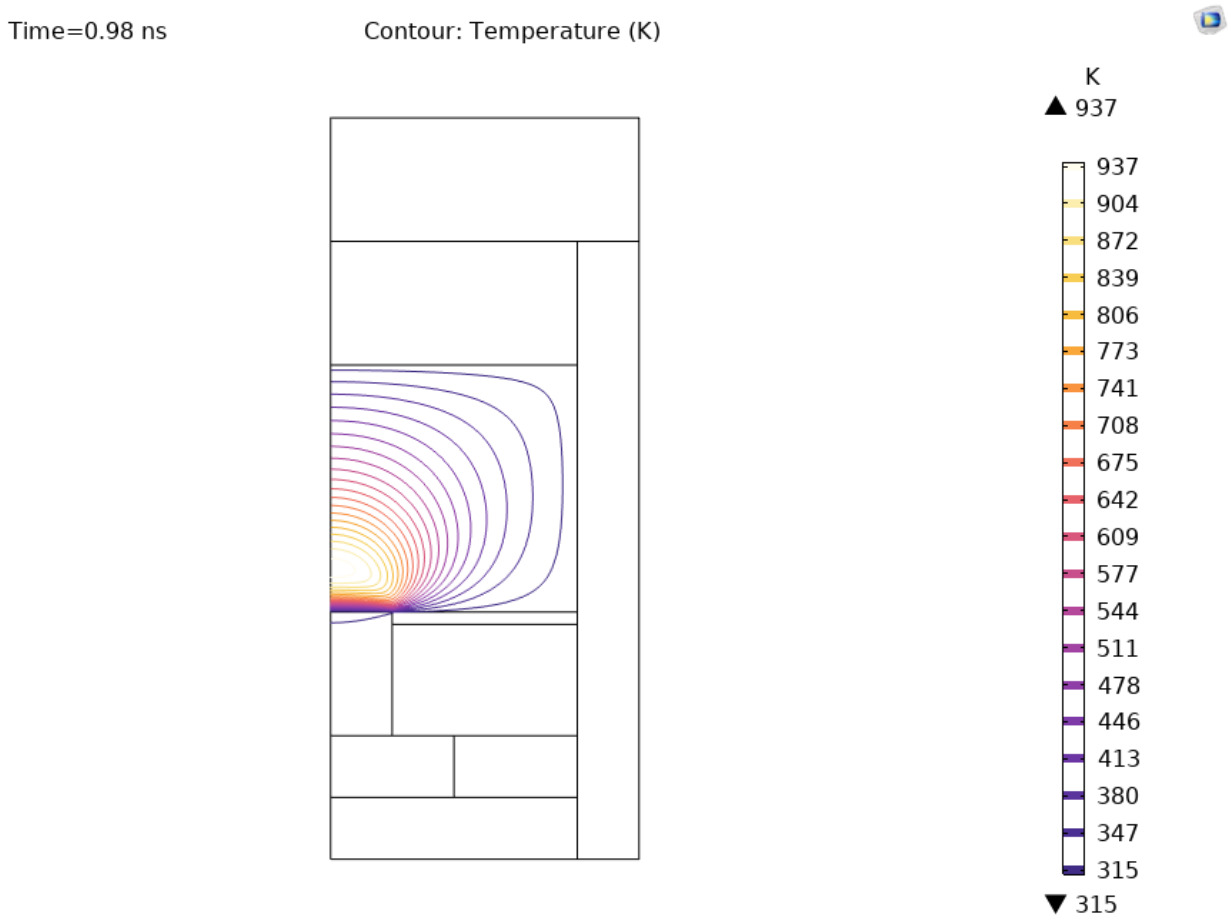
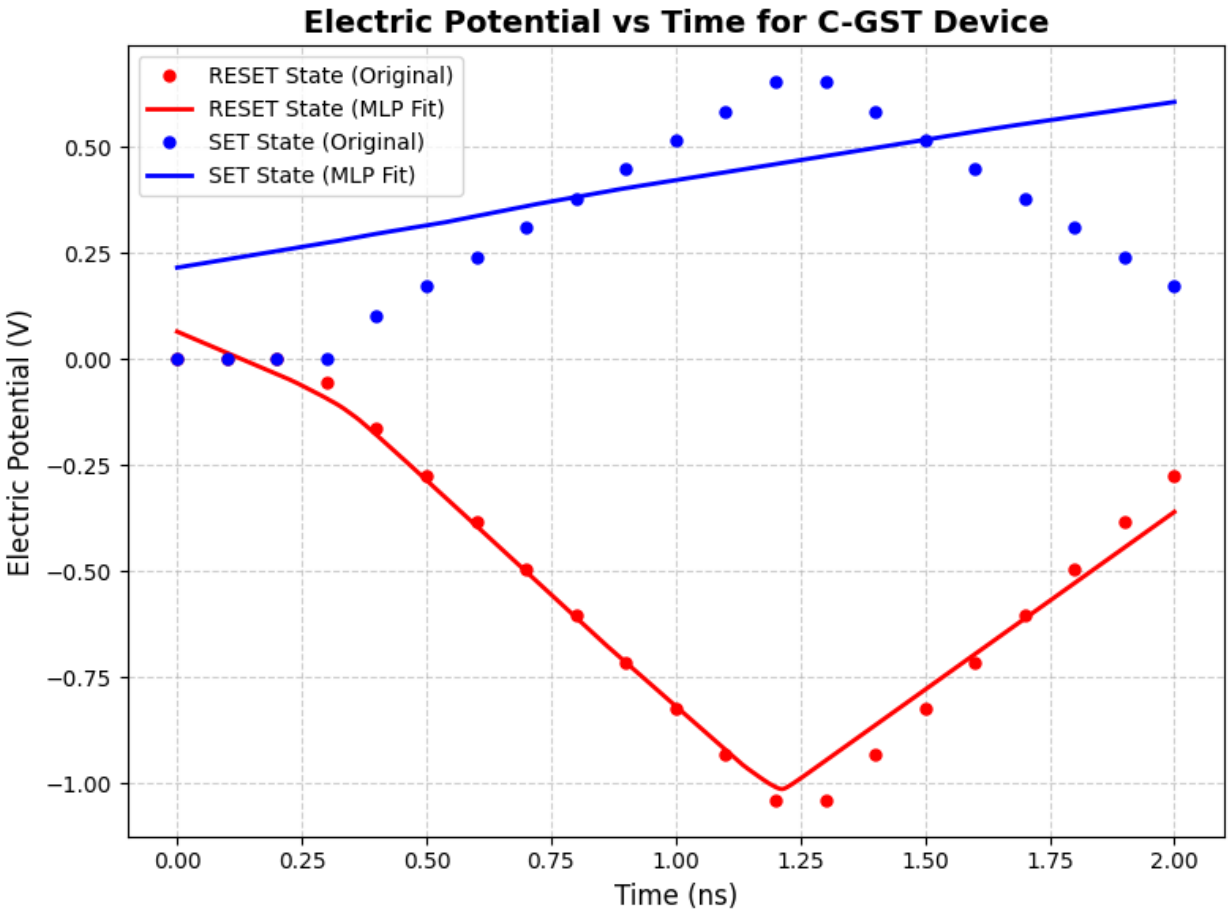


Fig. 18: Isothermal Contour (Temperature) amorphous State at 1.2 V applied voltage, R_L = 1K ohm, ti, time: 0.98 ns

The SET state (Crystalline done of the cell at 0.7 ns applied voltage 0.8 V, temperature at C-GST Layer: 461K)

The RESET state (Amorphous done of the cell at 0.98 ns applied voltage 1.2 V, temperature at C-GST Layer: 954K)

Figure : 19: Electric Potential (V) vs Time (ns))



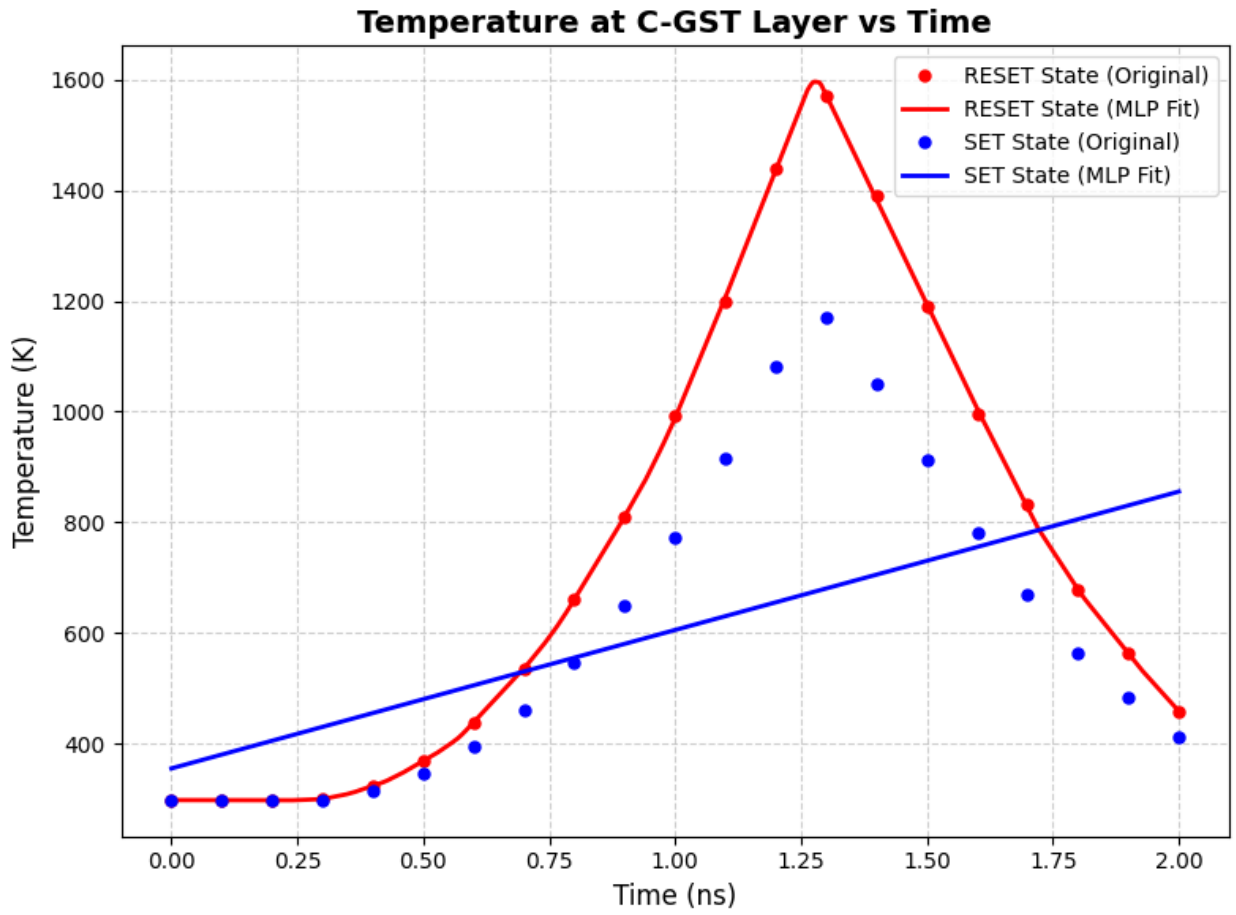
The Fig. 19 displays the temperature evolution at the C-GST layer over time (in nanoseconds) for both RESET and SET states, along with their respective MLP (Multi-Layer Perceptron) fits. For the RESET state, the original data points (red dots) show a rapid temperature increase, peaking around 1.3 ns at approximately 1580 K, followed by a sharp decline. The MLP fit (red line) closely follows this trend. In contrast, the SET state's original data (blue dots) exhibits a more gradual temperature increase, reaching around 1170 K at 1.3 ns and then decreasing. The MLP fit for the SET state (blue line) shows a smoother, almost linear increase from about 360 K to 860 K over the 2 ns duration.

Table 19: Electric Potential (V) vs Time (ns))

Time (ns)	Electric Potential (V) at RESET state for C-GST	Electric Potential (V) at SET state for C-GST
0	0.00E+00	0.00E+00
0.1	0.00E+00	0.00E+00
0.2	0.00E+00	0.00E+00
0.3	-5.49E-02	3.44E-05

0.4	-1.65E-01	1.03E-01
0.5	-2.74E-01	1.72E-01
0.6	-3.84E-01	2.41E-01
0.7	-4.94E-01	3.09E-01
0.8	-6.04E-01	3.78E-01
0.9	-7.14E-01	4.47E-01
1	-8.23E-01	5.15E-01
1.1	-9.33E-01	5.84E-01
1.2	-1.04E+00	6.53E-01
1.3	-1.04E+00	6.53E-01
1.4	-9.33E-01	5.84E-01
1.5	-8.23E-01	5.15E-01
1.6	-7.14E-01	4.47E-01
1.7	-6.04E-01	3.78E-01
1.8	-4.94E-01	3.09E-01
1.9	-3.84E-01	2.41E-01
2	-2.74E-01	1.72E-01

Fig. 20: Temperature at C-GST Layer (K) vs Time (ns))



The **Fig. 20** displays the temperature evolution at the C-GST layer over time (in nanoseconds) for both RESET and SET states, along with their respective MLP (Multi-Layer Perceptron) fits. For the RESET state, the original data points (red dots) show a rapid temperature increase, peaking around 1.3 ns at approximately 1580 K, followed by a sharp decline. The MLP fit (red line) closely follows this trend. In contrast, the SET state's original data (blue dots) exhibits a more gradual temperature increase, reaching around 1170 K at 1.3 ns and then decreasing. The MLP fit for the SET state (blue line) shows a smoother, almost linear increase from about 360 K to 860 K over the 2 ns duration.

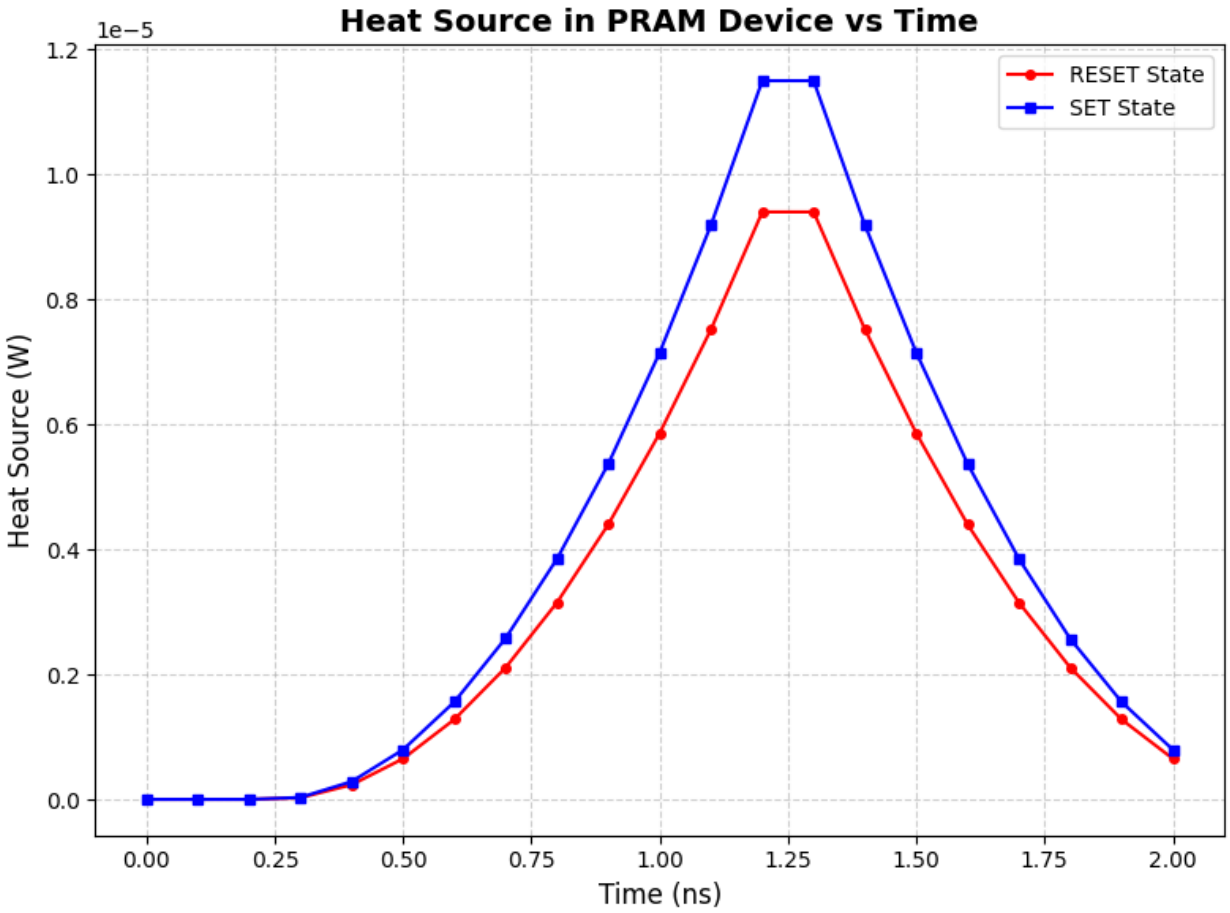
Table 20:

Temperature at C-GST Layer (K) vs Time (ns))

Time (ns)	Temperature at C-GST Layer (K) for RESET state	Temperature at C-GST Layer (K) for SET State
0	2.98E+02	2.98E+02
0.1	2.98E+02	2.98E+02
0.2	2.98E+02	2.98E+02

0.3	3.00E+02	2.99E+02
0.4	3.24E+02	3.16E+02
0.5	3.69E+02	3.46E+02
0.6	4.39E+02	3.95E+02
0.7	5.36E+02	4.61E+02
0.8	6.61E+02	5.46E+02
0.9	8.11E+02	6.49E+02
1	9.92E+02	7.73E+02
1.1	1.20E+03	9.16E+02
1.2	1.44E+03	1.08E+03
1.3	1.57E+03	1.17E+03
1.4	1.39E+03	1.05E+03
1.5	1.19E+03	9.13E+02
1.6	9.97E+02	7.82E+02
1.7	8.32E+02	6.69E+02
1.8	6.79E+02	5.63E+02
1.9	5.63E+02	4.83E+02
2	4.59E+02	4.13E+02

Fig.21: Heat Source for PRAM Device (W) vs Time (ns))



TheFig.21 illustrates the heat source (in Watts) within a PRAM (Phase-change Random Access Memory) device as a function of time (in nanoseconds) for both RESET and SET states. For the RESET state (red line with circles), the heat source starts near zero, rises sharply to a peak of approximately 9.4×10−6 W around 1.2 ns, and then rapidly decreases back to near zero by 2 ns. The SET state (blue line with squares) shows a similar trend but with a slightly delayed and higher peak of about 1.15×10−5 W around 1.3 ns, also returning to near zero by the end of the observed period.

Table 21:

Heat Source for PRAM Device (W) vs Time (ns))

Time (ns)	Heat Source for PRAM Device (W) at RESET state	Heat Source for PRAM Device (W) at SET state
0	0.00E+00	0.00E+00
0.1	0.00E+00	0.00E+00
0.2	0.00E+00	0.00E+00

0.3	2.61E-08	3.18E-08
0.4	2.34E-07	2.86E-07
0.5	6.51E-07	7.95E-07
0.6	1.28E-06	1.56E-06
0.7	2.11E-06	2.58E-06
0.8	3.15E-06	3.85E-06
0.9	4.40E-06	5.37E-06
1	5.86E-06	7.15E-06
1.1	7.52E-06	9.19E-06
1.2	9.40E-06	1.15E-05
1.3	9.40E-06	1.15E-05
1.4	7.52E-06	9.19E-06
1.5	5.86E-06	7.15E-06
1.6	4.40E-06	5.37E-06
1.7	3.15E-06	3.85E-06
1.8	2.11E-06	2.57E-06
1.9	1.28E-06	1.56E-06
2	6.51E-07	7.95E-07

Fig. 22: Electric Field norm (V/m) vs Time (ns))

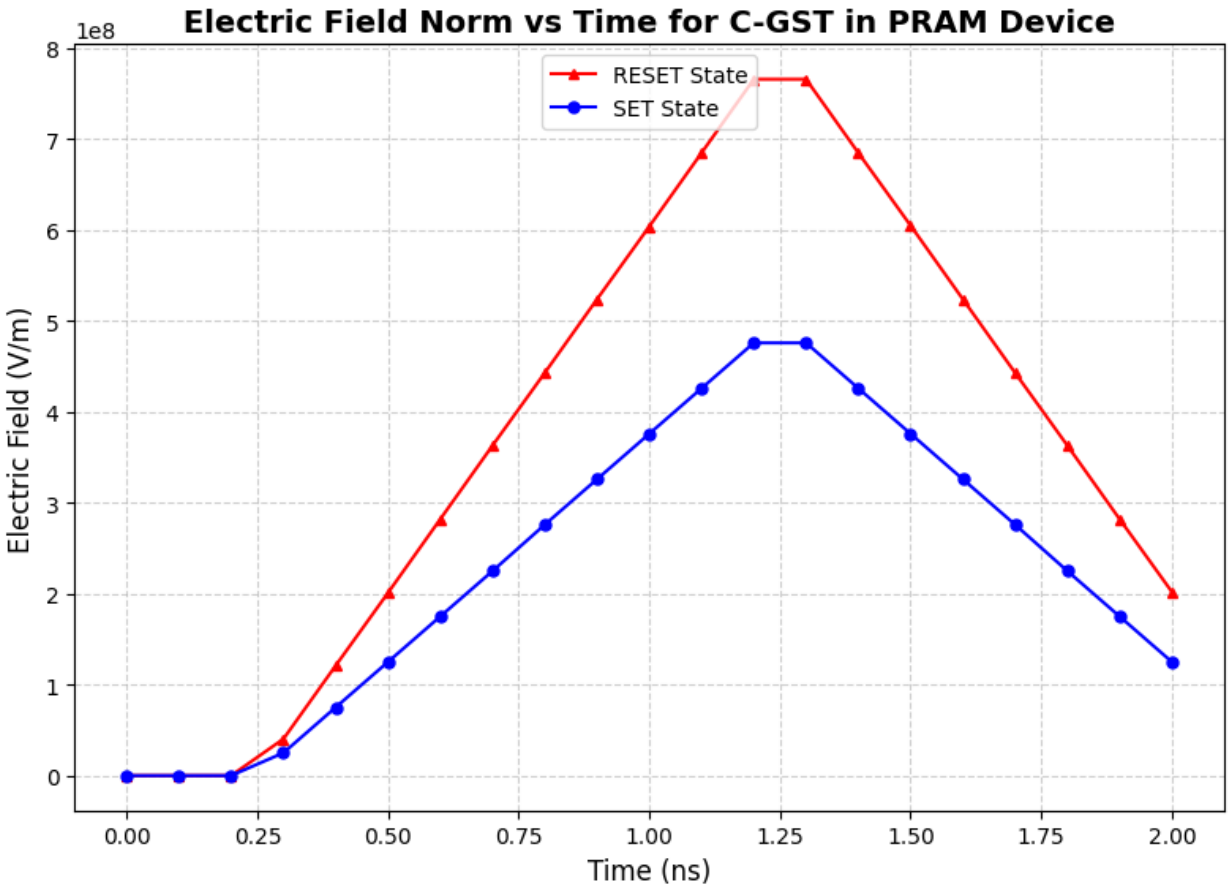


Fig. 22: Electric Field norm (V/m) vs Time (ns))

The **Fig. 22** presents the electric field norm (in V/m) over time (in nanoseconds) for the C-GST (Germanium-Antimony-Tellurium) material within a PRAM device, comparing the RESET and SET states. The RESET state (red line with triangles) exhibits a rapid increase in the electric field, reaching a plateau of approximately 7.6×108 V/m between 1.2 ns and 1.3 ns, followed by a sharp decline to about 2×108 V/m at 2 ns. Conversely, the SET state (blue line with circles) shows a more gradual increase, peaking at around 4.8×108 V/m at 1.3 ns, and then decreasing to approximately 1.25×108 V/m at the end of the 2 ns interval.

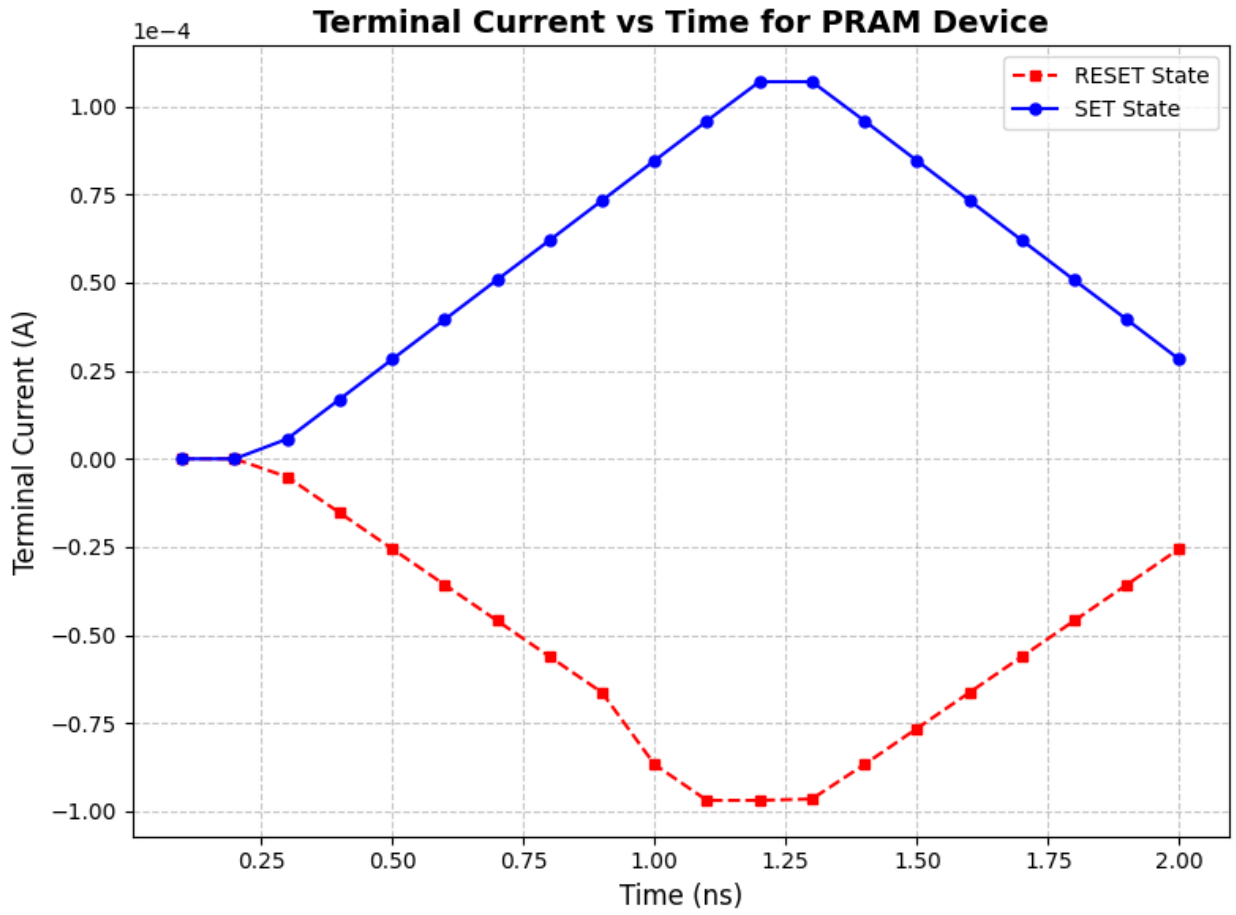
Table 22:

Electric Field norm (V/m) vs Time (ns))

Time (ns)	Electric Field (V/m) at RESET state for C-GST	Electric Field (V/m) at SET state for C-GST
0	0.00E+00	0.00E+00
0.1	0.00E+00	0.00E+00
0.2	0.00E+00	0.00E+00

0.3	4.03E+07	2.50E+07
0.4	1.21E+08	7.51E+07
0.5	2.01E+08	1.25E+08
0.6	2.82E+08	1.75E+08
0.7	3.63E+08	2.25E+08
0.8	4.43E+08	2.76E+08
0.9	5.24E+08	3.26E+08
1	6.04E+08	3.76E+08
1.1	6.85E+08	4.26E+08
1.2	7.66E+08	4.76E+08
1.3	7.66E+08	4.76E+08
1.4	6.85E+08	4.26E+08
1.5	6.05E+08	3.76E+08
1.6	5.24E+08	3.26E+08
1.7	4.43E+08	2.76E+08
1.8	3.63E+08	2.25E+08
1.9	2.82E+08	1.75E+08
2	2.02E+08	1.25E+08

Fig. 23: Terminal Current (A) for PRAM Device vs pulse (ns)



The **Fig. 23** displays the terminal current (in Amperes) over time (in nanoseconds) for a PRAM device in both RESET and SET states. The RESET state (red dashed line with squares) shows a negative current initially, reaching a minimum of approximately −9.7×10−5 A around 1.2 ns, before increasing to about −2.5×10−5 A at 2 ns. The SET state (blue solid line with circles) exhibits a positive current, increasing to a maximum of roughly 1.05×10−4 A around 1.3 ns, and then decreasing to approximately 2.8×10−5 A at the end of the 2 ns period.

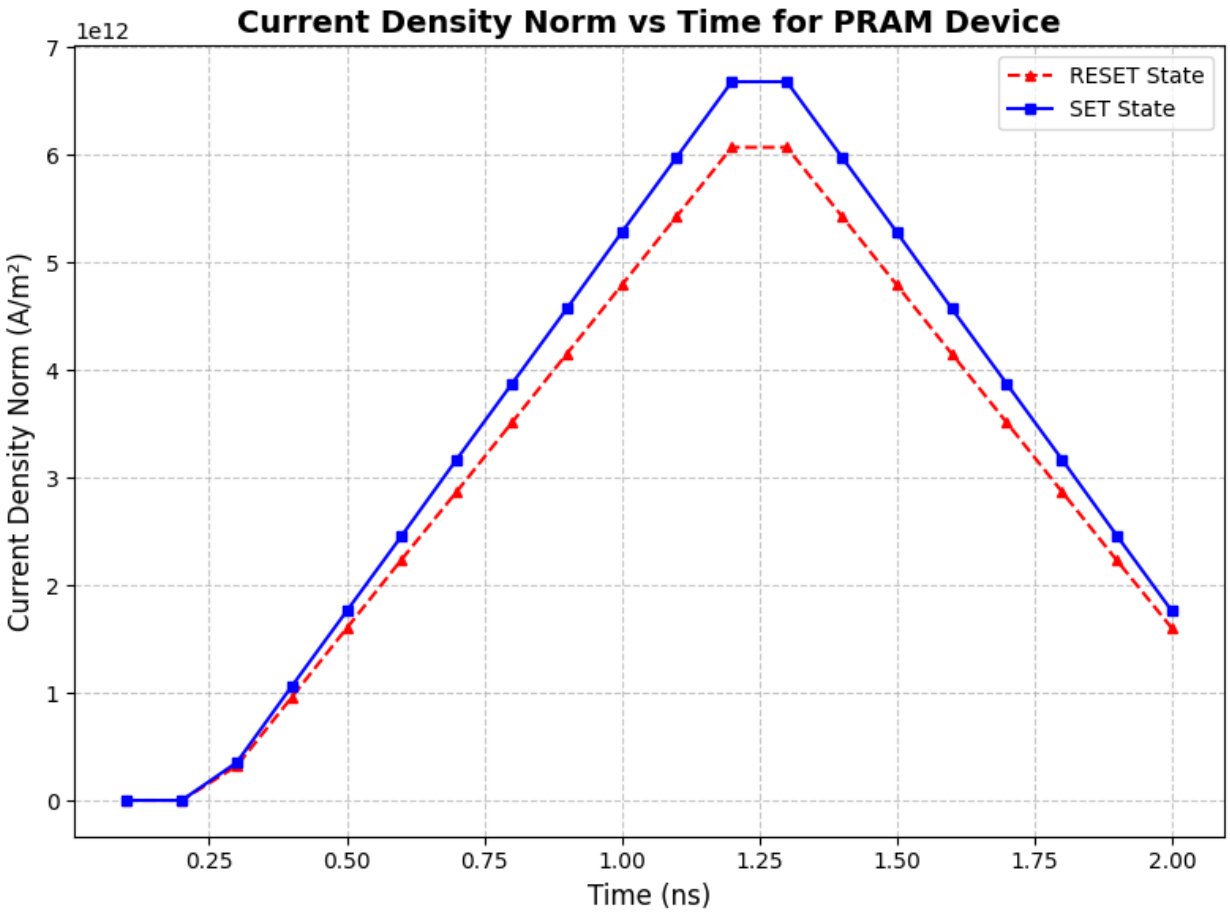
Table 23:

Terminal Current (A) for PRAM Device vs pulse (ns)

Time (ns)	Terminal Current (A) at RESET state	Terminal Current (A) at SET state
0.1	0.00E+00	0.00E+00
0.2	0.00E+00	0.00E+00
0.3	-5.11E-06	5.64E-06
0.4	-1.53E-05	1.69E-05

0.5	-2.55E-05	2.82E-05
0.6	-3.57E-05	3.95E-05
0.7	-4.59E-05	5.08E-05
0.8	-5.61E-05	6.20E-05
0.9	-6.63E-05	7.33E-05
1	-8.67E-05	8.46E-05
1.1	-9.69E-05	9.59E-05
1.2	-9.69E-05	1.07E-04
1.3	-9.65E-05	1.07E-04
1.4	-8.67E-05	9.59E-05
1.5	-7.65E-05	8.46E-05
1.6	-6.63E-05	7.33E-05
1.7	-5.61E-05	6.20E-05
1.8	-4.59E-05	5.07E-05
1.9	-3.57E-05	3.95E-05
2	-2.55E-05	2.82E-05

Fig. 24: Current Density Norm (A/(m^2))) vs Time (ns))



The **Fig. 24** shows the current density norm (in A/m²) as a function of time (in nanoseconds) for a PRAM device in both the RESET and SET states. For the RESET state (red dashed line with triangles), the current density increases to a peak of approximately 6.1×1012 A/m² around 1.2 ns and then decreases to about 1.6×1012 A/m² at 2 ns. The SET state (blue solid line with squares) exhibits a similar trend, reaching a higher peak of about 6.7×1012 A/m² around 1.3 ns and then falling to approximately 1.75×1012 A/m² at the end of the 2 ns period.

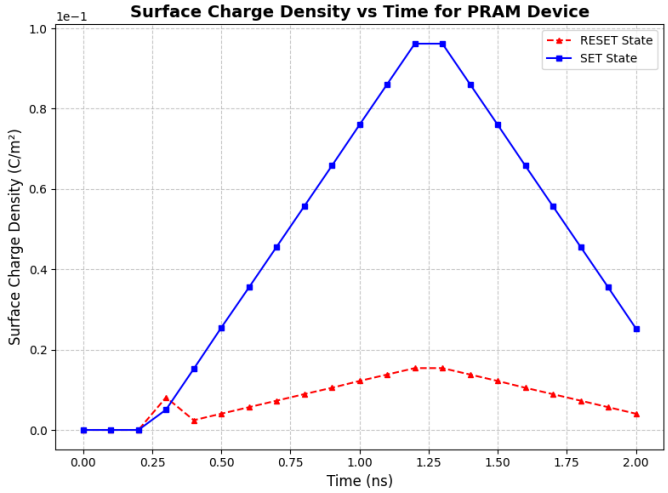
Table 24:

Current Density Norm (A/(m^2))) vs Time (ns))

Time (ns)	Current Density Norm (A/(m^2))) at RESET state	Current Density Norm (A/(m^2))) at SET state
0.1	0.00E+00	0.00E+00
0.2	0.00E+00	0.00E+00
0.3	3.20E+11	3.52E+11
0.4	9.58E+11	1.06E+12

0.5	1.60E+12	1.76E+12
0.6	2.24E+12	2.46E+12
0.7	2.87E+12	3.17E+12
0.8	3.51E+12	3.87E+12
0.9	4.15E+12	4.57E+12
1	4.79E+12	5.28E+12
1.1	5.43E+12	5.98E+12
1.2	6.07E+12	6.68E+12
1.3	6.07E+12	6.68E+12
1.4	5.43E+12	5.98E+12
1.5	4.79E+12	5.28E+12
1.6	4.15E+12	4.57E+12
1.7	3.51E+12	3.87E+12
1.8	2.87E+12	3.17E+12
1.9	2.23E+12	2.46E+12
2	1.60E+12	1.76E+12

Fig. 25: Surface Charge Density (C/(m^2))) vs Time (ns))



The **Fig. 25** illustrates the surface charge density (in C/m²) over time (in nanoseconds) for a PRAM device in both the RESET and SET states. For the RESET state (red dashed line with triangles), the surface charge density increases to a peak of approximately 1.6×10−1 C/m² around 1.3 ns and then decreases to about 4×10−2 C/m² at 2 ns. The SET state (blue solid line with squares) shows a more pronounced increase, reaching a peak of roughly 9.6×10−1 C/m² around 1.3 ns, before decreasing to approximately 2.5×10−1 C/m² at the end of the 2 ns interval.

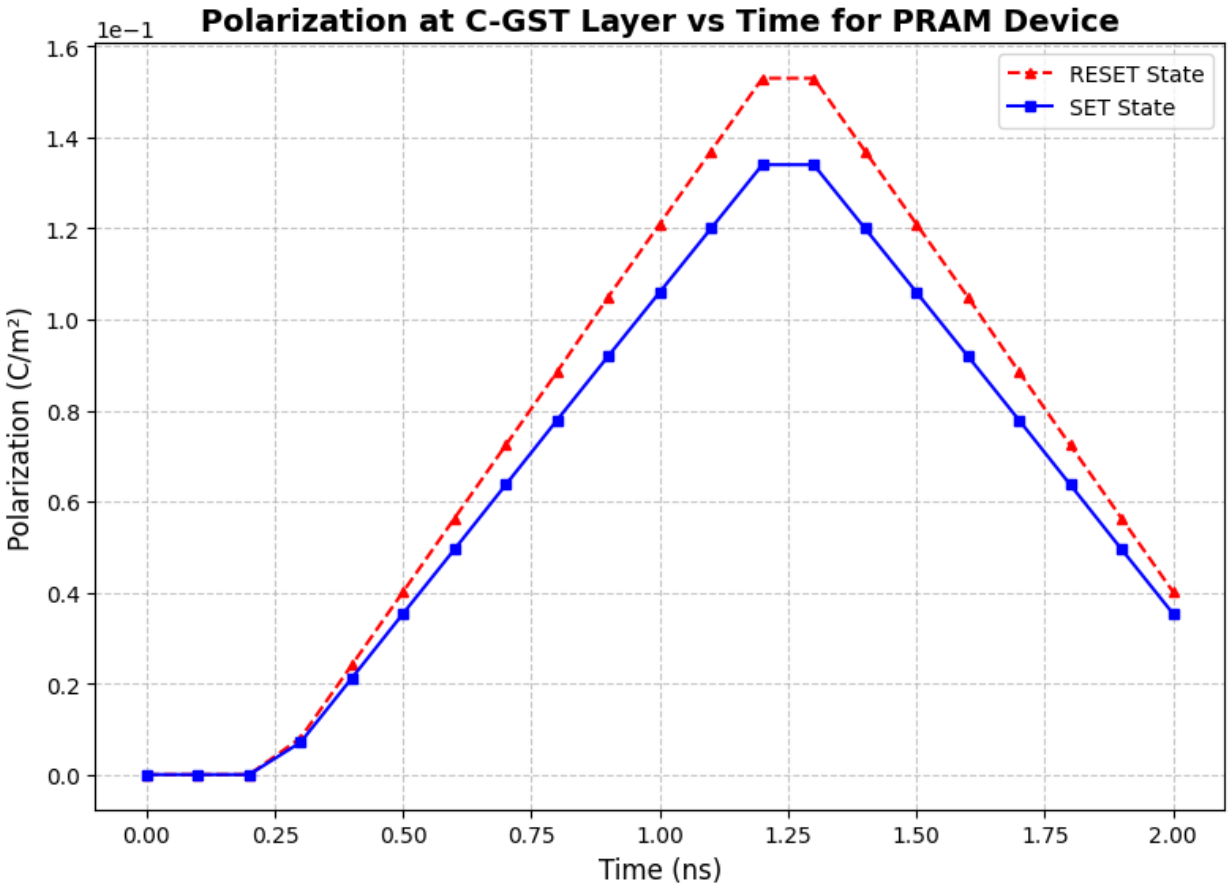
Table 25:

Surface Charge Density (C/(m^2))) vs Time (ns))

Time (ns)	Surface Charge Density (C/(m^2))) at RESET state	Surface Charge Density (C/(m^2))) at SET state
0	0.00E+00	0.00E+00
0.1	0.00E+00	0.00E+00
0.2	0.00E+00	0.00E+00
0.3	8.12E-03	5.06E-03
0.4	2.43E-03	1.52E-02
0.5	4.05E-03	2.55E-02
0.6	5.67E-03	3.55E-02
0.7	7.29E-03	4.56E-02
0.8	8.92E-03	5.57E-02
0.9	1.05E-02	6.58E-02
1	1.22E-02	7.60E-02
1.1	1.38E-02	8.61E-02
1.2	1.54E-02	9.62E-02
1.3	1.54E-02	9.62E-02
1.4	1.38E-02	8.61E-02
1.5	1.22E-02	7.60E-02
1.6	1.05E-02	6.58E-02
1.7	8.91E-03	5.57E-02
1.8	7.29E-03	4.56E-02
1.9	5.67E-03	3.55E-02

2	4.05E-03	2.53E-02

Fig. 26: Polarization (C/(m^2))) at C-GST layer vs Time (ns)



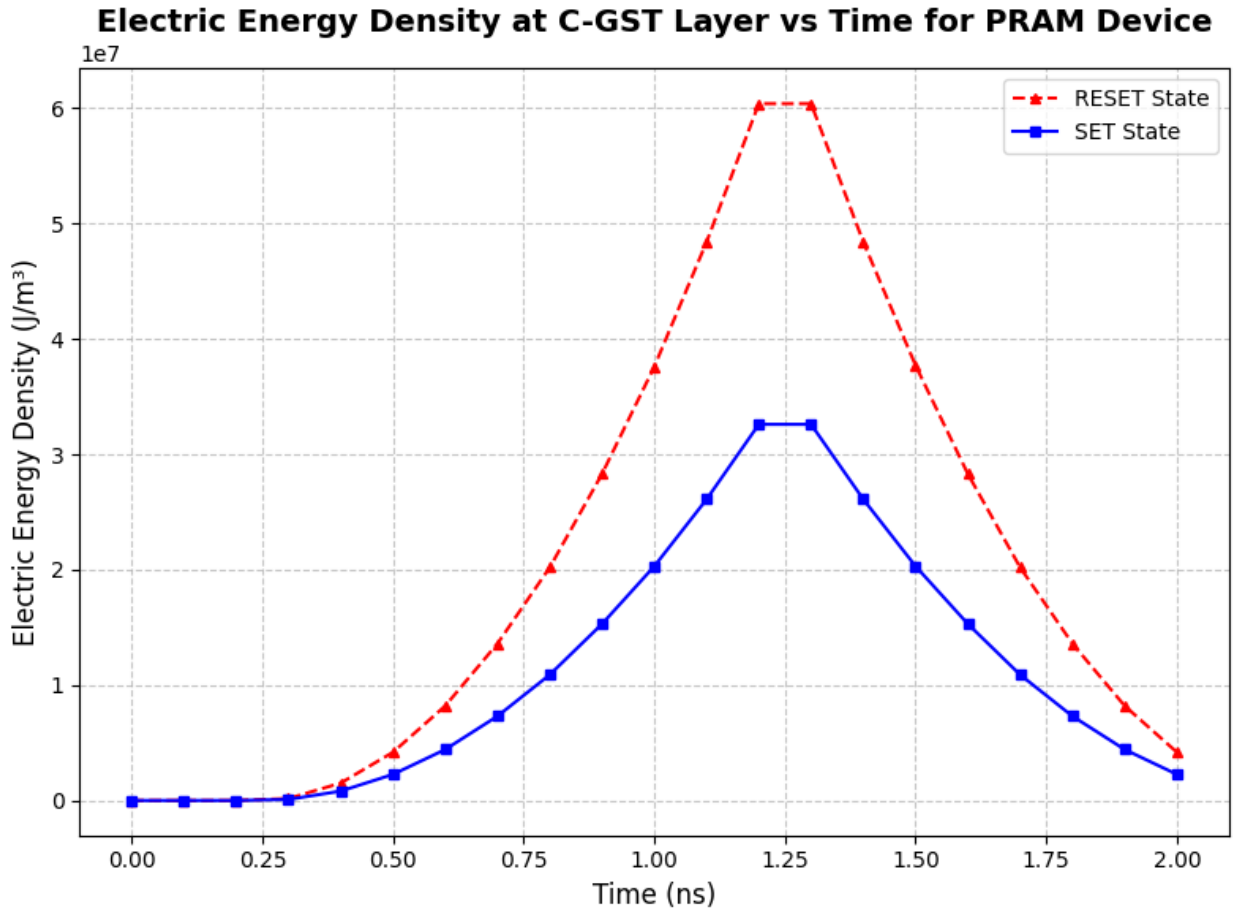
The **Fig. 26** shows the polarization (in C/m²) at the C-GST layer over time (in nanoseconds) for a PRAM device in both the RESET and SET states. For the RESET state (red dashed line with triangles), the polarization increases to a peak of approximately 1.55×10−1 C/m² around 1.3 ns and then decreases to about 4×10−2 C/m² at 2 ns. The SET state (blue solid line with squares) exhibits a more gradual increase, reaching a plateau of roughly 1.35×10−1 C/m² between 1.2 ns and 1.3 ns, before decreasing to approximately 3.5×10−2 C/m² at the end of the 2 ns period.

Table 26:

Polarization (C/(m^2))) at C-GST layer vs Time (ns)

Time (ns)	Polarization (C/(m^2))) at C-GST layer at RESET state	Polarization (C/(m^2))) at C-GST layer at SET state
0	0.00E+00	0.00E+00
0.1	0.00E+00	0.00E+00
0.2	0.00E+00	0.00E+00
0.3	8.05E-03	7.08E-03
0.4	2.41E-02	2.12E-02
0.5	4.02E-02	3.54E-02
0.6	5.63E-02	4.95E-02
0.7	7.24E-02	6.37E-02
0.8	8.85E-02	7.79E-02
0.9	1.05E-01	9.20E-02
1	1.21E-01	1.06E-01
1.1	1.37E-01	1.20E-01
1.2	1.53E-01	1.34E-01
1.3	1.53E-01	1.34E-01
1.4	1.37E-01	1.20E-01
1.5	1.21E-01	1.06E-01
1.6	1.05E-01	9.20E-02
1.7	8.85E-02	7.79E-02
1.8	7.24E-02	6.37E-02
1.9	5.63E-02	4.95E-02
2	4.02E-02	3.54E-02

Fig. 27: Electric Energy Density (J/(m^3))) at C-GST layer vs Time (ns)



The **Fig. 27** shows the electric energy density (in J/m³) at the C-GST layer over time (in nanoseconds) for a PRAM device in both the RESET and SET states. For the RESET state (red dashed line with triangles), the electric energy density increases to a peak of approximately 6.1×107 J/m³ around 1.3 ns and then decreases to about 3×106 J/m³ at 2 ns. The SET state (blue solid line with squares) exhibits a more gradual increase, reaching a peak of roughly 3.3×107 J/m³ around 1.3 ns, before decreasing to approximately 2.5×106 J/m³ at the end of the 2 ns period.

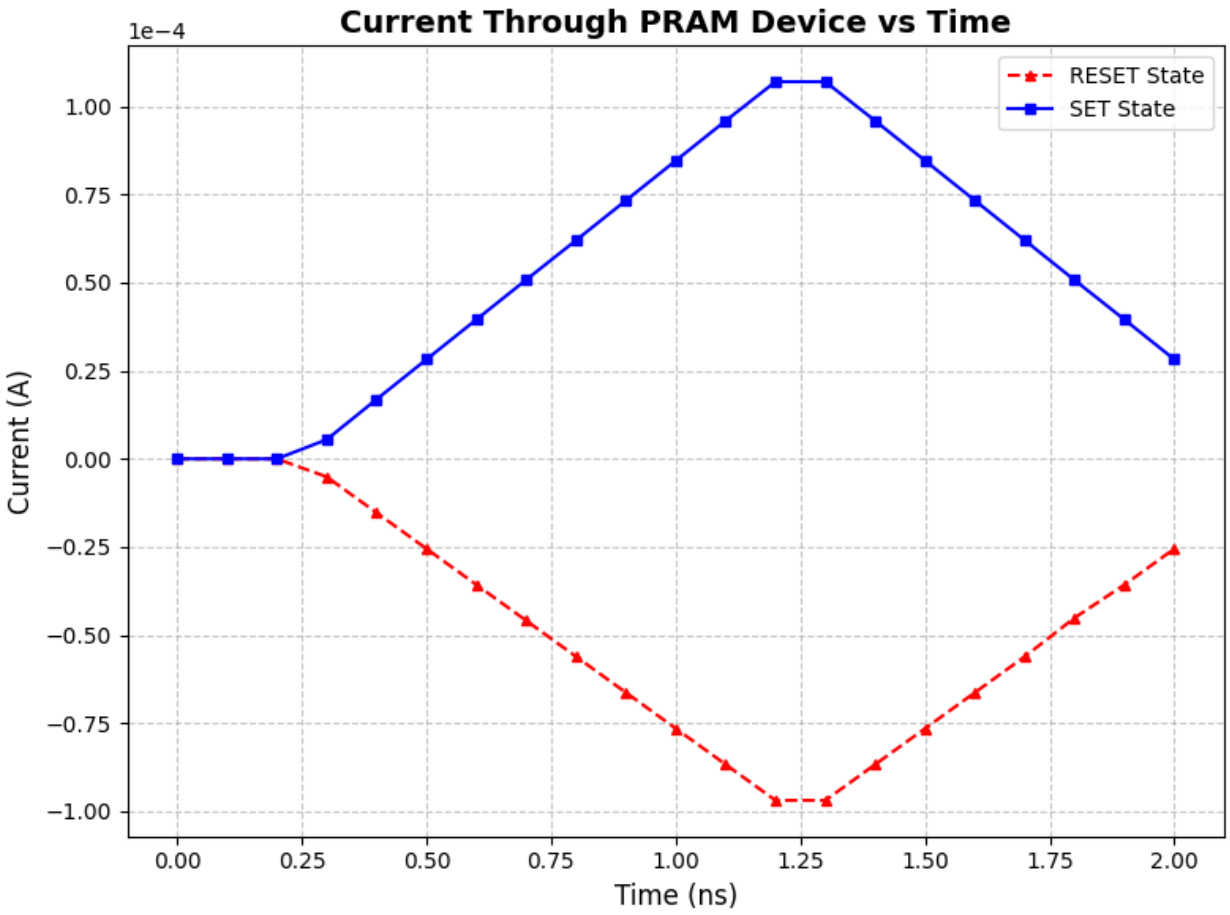
Table 27:

Electric Energy Density (J/(m^3))) at C-GST layer vs Time (ns)

Time (ns)	Electric Energy Density (J/(m^3))) at C-GST layer at RESET state	Electric Energy Density (J/(m^3))) at C-GST layer at SET state
0	0.00E+00	0.00E+00

0.1	0.00E+00	0.00E+00
0.2	0.00E+00	0.00E+00
0.3	1.67E+05	9.02E+04
0.4	1.51E+06	8.12E+05
0.5	4.18E+06	2.26E+06
0.6	8.20E+06	4.42E+06
0.7	1.36E+07	7.31E+06
0.8	2.02E+07	1.09E+07
0.9	2.83E+07	1.53E+07
1	3.76E+07	2.03E+07
1.1	4.84E+07	2.61E+07
1.2	6.04E+07	3.26E+07
1.3	6.04E+07	3.26E+07
1.4	4.84E+07	2.61E+07
1.5	3.77E+07	2.03E+07
1.6	2.83E+07	1.53E+07
1.7	2.02E+07	1.09E+07
1.8	1.36E+07	7.31E+06
1.9	8.20E+06	4.42E+06
2	4.18E+06	2.26E+06

Fig. 28: Current Through Device (A) PRAM vs Time (ns))



The **Fig. 28** illustrates the current (in Amperes) through a PRAM device over time (in nanoseconds) for both the RESET and SET states. The RESET state (red dashed line with triangles) shows a negative current, reaching a minimum of approximately −9.7×10−5 A around 1.2 ns, and then increasing to about −2.5×10−5 A at 2 ns. The SET state (blue solid line with squares) exhibits a positive current, increasing to a maximum of roughly 1.05×10−4 A around 1.3 ns, before decreasing to approximately 2.8×10−5 A at the end of the 2 ns interval.

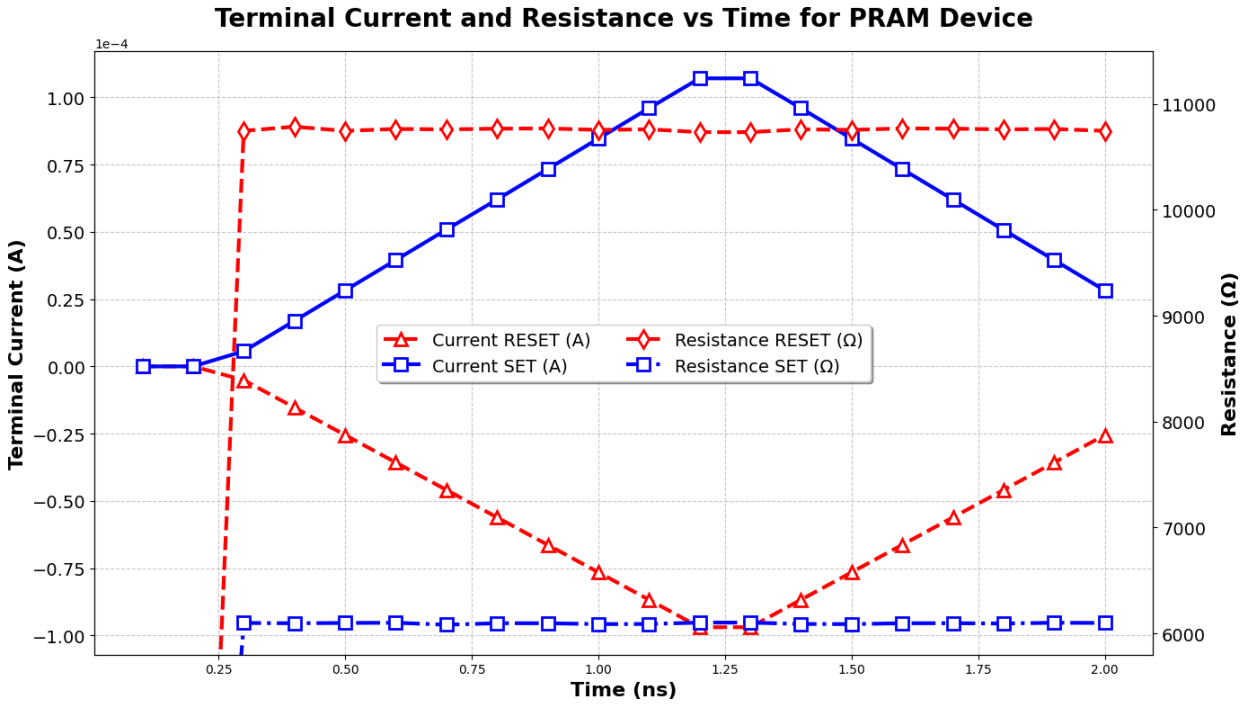
Table 28:

Current Through Device (A) PRAM vs Time (ns))

Time (ns)	Current Through Device (A) at RESET state	Current Through Device (A) at SET state
0	0.00E+00	0.00E+00
0.1	0.00E+00	0.00E+00
0.2	0.00E+00	0.00E+00
0.3	-5.11E-06	5.47E-06

0.4	-1.53E-05	1.69E-05
0.5	-2.55E-05	2.82E-05
0.6	-3.57E-05	3.95E-05
0.7	-4.59E-05	5.08E-05
0.8	-5.61E-05	6.20E-05
0.9	-6.63E-05	7.33E-05
1	-7.65E-05	8.46E-05
1.1	-8.67E-05	9.59E-05
1.2	-9.69E-05	1.07E-04
1.3	-9.69E-05	1.07E-04
1.4	-8.67E-05	9.59E-05
1.5	-7.65E-05	8.46E-05
1.6	-6.63E-05	7.33E-05
1.7	-5.61E-05	6.20E-05
1.8	-4.51E-05	5.07E-05
1.9	-3.57E-05	3.95E-05
2	-2.55E-05	2.82E-05

Fig. 29: Terminal Current (A) for PRAM Device vs pulse (ns) Vs Resistance (ohm)



The **Fig. 29** displays the terminal current (in Amperes) and resistance (in Ohms) over time (in nanoseconds) for a PRAM device in both RESET and SET states, utilizing a dual y-axis. The left y-axis shows the current, while the right y-axis represents the resistance. For the RESET state, the current (red dashed line with triangles) is initially negative, reaching a minimum of approximately −9.7×10−5 A around 1.2 ns, and then increases to about −2.5×10−5 A at 2 ns. The corresponding resistance (red dashed line with diamonds) starts high at around 1.1×104 Ω, drops sharply to about 8×103 Ω, and then remains relatively constant. In the SET state, the current (blue solid line with squares) is positive, peaking at roughly 1.05×10−4 A around 1.3 ns, and then decreasing to approximately 2.8×10−5 A at 2 ns. The resistance for the SET state (blue dotted line with filled squares) starts low at approximately 6×103 Ω and remains relatively stable throughout the observed period.

Table 29:

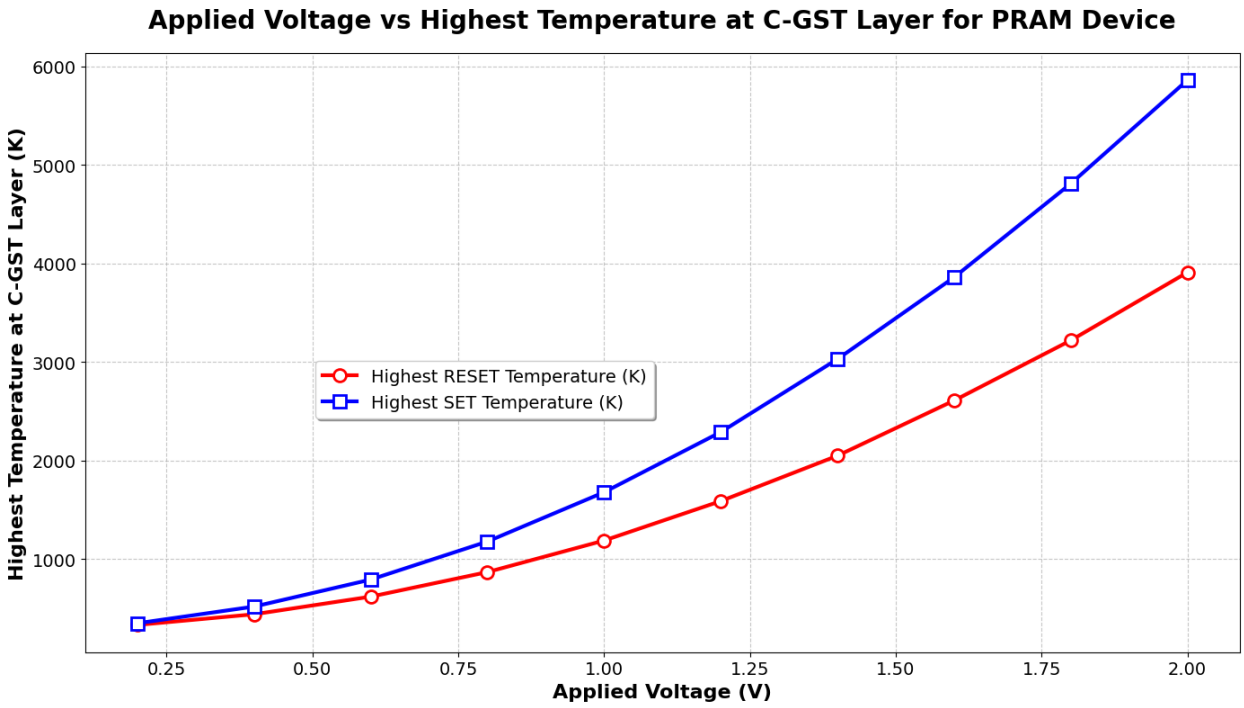
Terminal Current (A) for PRAM Device vs pulse (ns) Vs Resistance (ohm)

Time (ns) Terminal Current (A) at RESET state Terminal Voltage (V) at RESET state Resistance (ohm) at RESET State Terminal Current (A) at SET state Terminal Voltage (V) at SET state Resistance (ohm) at SET State

0.1		0.00E+00			0				
	0		0.00E+00			0			
	0								
0.2		0.00E+00			0				
	0		0.00E+00			0			
	0								
0.3		-5.11E-06			-0.0549				
	1.074560E+04		5.64E-06			0.0344			
	6099.29								
0.4		-1.53E-05			-0.165				
	1.078431E+04		1.69E-05			0.103			
	6096.45								
0.5		-2.55E-05			-0.274				
	1.074510E+04		2.82E-05			0.172			
	6099.29								
0.6		-3.57E-05			-0.384				
	1.076302E+04		3.95E-05			0.241			
	6101.27								
0.7		-4.59E-05			-0.494				
	1.075904E+04		5.08E-05			0.309			
	6082.68								
0.8		-5.61E-05			-0.604				
	1.076562E+04		6.20E-05			0.378			
	6096.77								
0.9		-6.63E-05			-0.714				
	1.076802E+04		7.33E-05			0.447			
	6096.59								
1		-7.65E-05			-0.823				
	1.075425E+04		8.46E-05			0.515			
	6088.53								
1.1		-8.67E-05			-0.933				
	1.075975E+04		9.59E-05			0.584			
	6089.68								
1.2		-9.69E-05			-1.04				
	1.073270E+04		1.07E-04			0.653			
	6102.8								

1.3	1.073270E+04	-9.69E-05	1.07E-04	-1.04	0.653
	6102.8				
1.4	1.075975E+04	-8.67E-05	9.59E-05	-0.933	0.584
	6089.68				
1.5	1.075425E+04	-7.65E-05	8.46E-05	-0.823	0.515
	6088.53				
1.6	1.076802E+04	-6.63E-05	7.33E-05	-0.714	0.447
	6096.59				
1.7	1.076562E+04	-5.61E-05	6.20E-05	-0.604	0.378
	6096.77				
1.8	1.075904E+04	-4.59E-05	5.07E-05	-0.494	0.309
	6094.28				
1.9	1.076302E+04	-3.57E-05	3.95E-05	-0.384	0.241
	6101.27				
2	1.074510E+04	-2.55E-05	2.82E-05	-0.274	0.172
	6099.29				

Fig. 29: Applied Voltage(V) for PRAM Device vs Highest Temperature at C-GST Layer



The **Fig. 30** illustrates the relationship between the applied voltage (in Volts) and the highest temperature reached at the C-GST layer (in Kelvin) for a PRAM device in both RESET and SET states. As the applied voltage increases from 0.2 V to 2.0 V, the highest temperature for both states also increases. The highest temperature for the RESET state (red line with circles) rises from approximately 350 K to 3950 K. Similarly, for the SET state (blue line with squares), the highest temperature increases from roughly 380 K to 5900 K over the same voltage range, consistently exhibiting a higher peak temperature compared to the RESET state for a given applied voltage.

Table 30:

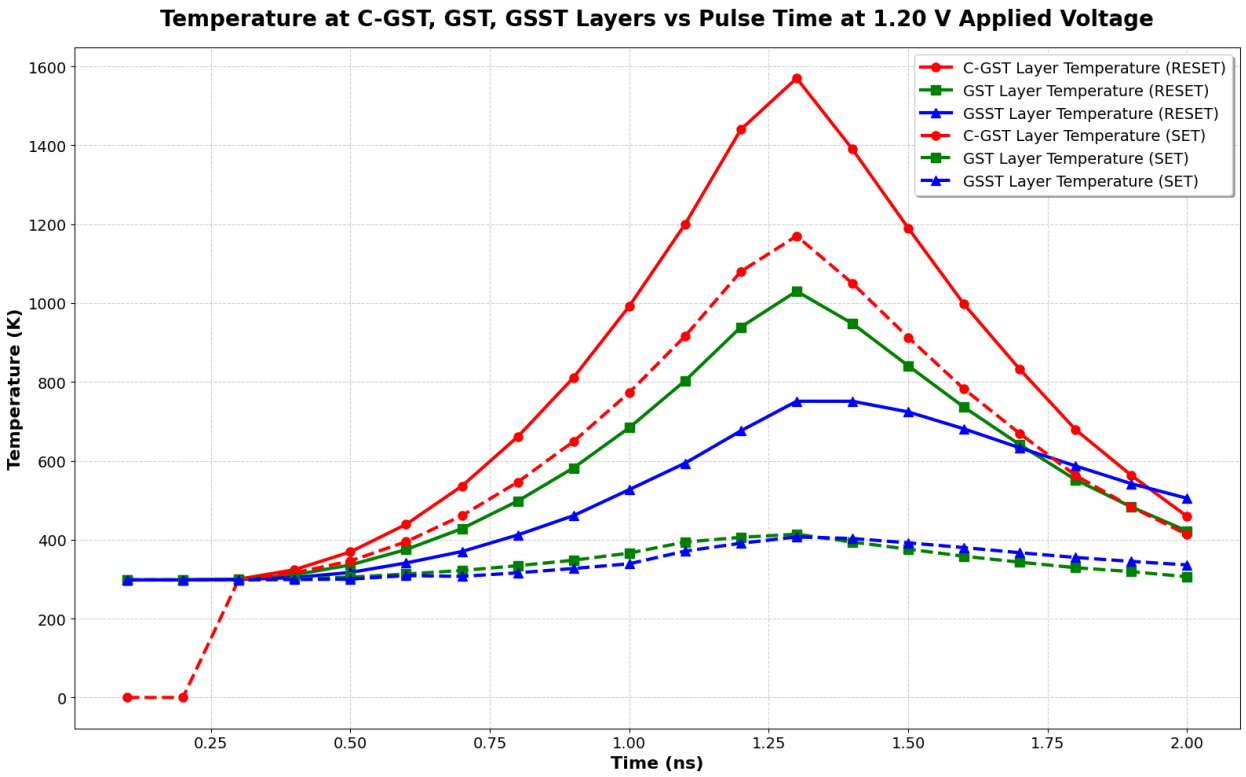
Applied Voltage(V) for PRAM Device vs Highest Temperature at C-GST Layer

Applied Voltage (V)	Highest RESET Temperature at C-GST Layer	Highest SET Temperature at C-GST Layer
0.2	3.34E+02	351
0.4	4.42E+02	520

0.6		6.21E+02
	794	
0.8		8.70E+02
	1.18E+03	
1		1.19E+03
	1.68E+03	
1.2		1.59E+03
	2.29E+03	
1.4		2.05E+03
	3.03E+03	
1.6		2.61E+03
	3.86E+03	
1.8		3.22E+03
	4.81E+03	
2		3.91E+03
	5.86E+03	

""

Fig. 31: Temperature at C-GST, GST, GSST Layer (K) for PRAM Device vs pulse (ns) at 1.20V Applies Voltage



The **Fig. 31** shows the temperature (in Kelvin) at the C-GST, GST, and GSST layers as a function of pulse time (in nanoseconds) at a fixed applied voltage of 1.20 V, for both RESET and SET states. For the RESET state, the C-GST layer (red circles and solid line) reaches the highest peak temperature of approximately 1580 K around 1.3 ns, while the GST layer (green squares and solid line) peaks at about 1040 K, and the GSST layer (blue triangles and solid line) reaches around 760 K at a slightly later time. In the SET state, the C-GST layer (red circles and dashed line) reaches a lower peak temperature of about 1170 K, the GST layer (green squares and dashed line) peaks at roughly 410 K, and the GSST layer (blue triangles and dashed line) reaches approximately 400 K, all occurring around 1.3 ns. Generally, the RESET state exhibits significantly higher temperatures across all layers compared to the SET state at this applied voltage.

Table 31:

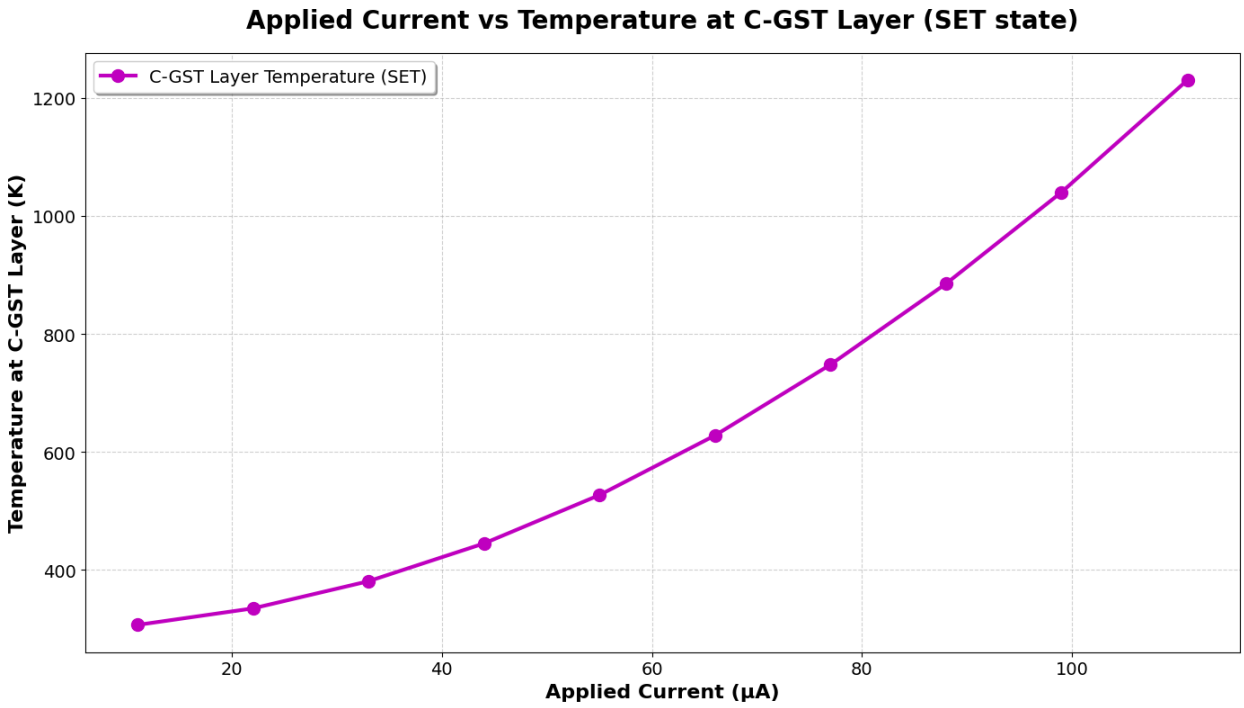
Temperature at C-GST, GST, GSST Layer (K) for PRAM Device vs pulse (ns) at 1.20V Applies Voltage

Time (ns) Temperature of C-GST Layer (K) at RESET state Temperature of C-GST Layer (K) at SET state Temperature of GST Layer (K) at RESET State Temperature of GST Layer (K) at SET State Temperature of GSST Layer (K) at RESET State Temperature of GSST Layer (K) at SET State

0.1				2.98E+02					0.00E+00
			298					298	
	298						298		
0.2				2.98E+02					0.00E+00
			298					298	
	298						298		
0.3				3.00E+02					2.99E+02
			299					298	
	299						298		
0.4				3.24E+02					3.16E+02
			311					301	
	304						299		
0.5				3.69E+02					3.46E+02
			336					305	
	317						300		
0.6				4.39E+02					3.95E+02
			375					313	
	341						309		
0.7				5.36E+02					4.61E+02
			428					322	
	370						307		
0.8				6.61E+02					5.46E+02
			498					334	
	412						316		
0.9				8.11E+02					6.49E+02
			582					348	
	461						327		
1				9.92E+02					7.73E+02
			6.84E+02					366	
	527						339		
1.1				1.20E+03					9.16E+02
			8.03E+02					3.94E+02	
		594					371		
1.2				1.44E+03					1.08E+03
			9.39E+02					4.06E+02	
		676					391		

1.3		1.57E+03		1.17E+03	
	1.03E+03			4.14E+02	
	751			407	
1.4		1.39E+03		1.05E+03	
	9.48E+02			3.94E+02	
	751			403	
1.5		1.19E+03		9.13E+02	
	8.41E+02			3.76E+02	
	724			392	
1.6		9.97E+02		7.82E+02	
	7.36E+02			3.58E+02	
	681			380	
1.7		8.32E+02		6.69E+02	
	6.41E+02			3.43E+02	
	633			367	
1.8		6.79E+02		5.63E+02	
	5.52E+02			3.29E+02	
	587			355	
1.9		5.63E+02		4.83E+02	
	4.83E+02			3.19E+02	
	542			345	
2		4.59E+02		4.13E+02	
	4.22E+02			3.06E+02	
	505			336	

Fig. 32: Applied Current (uA) for PRAM Device vsTemperature at C-GST Layer (K)



The **Fig. 32** illustrates the relationship between the applied current (in microamperes, µA) and the temperature at the C-GST layer (in Kelvin) specifically for the SET state of a PRAM device. As the applied current increases from approximately 10 µA to 115 µA, the temperature at the C-GST layer also increases non-linearly, rising from about 310 K to approximately 1240 K. This indicates a strong positive correlation between the applied current and the resulting temperature within the C-GST layer during the SET operation of the PRAM device.

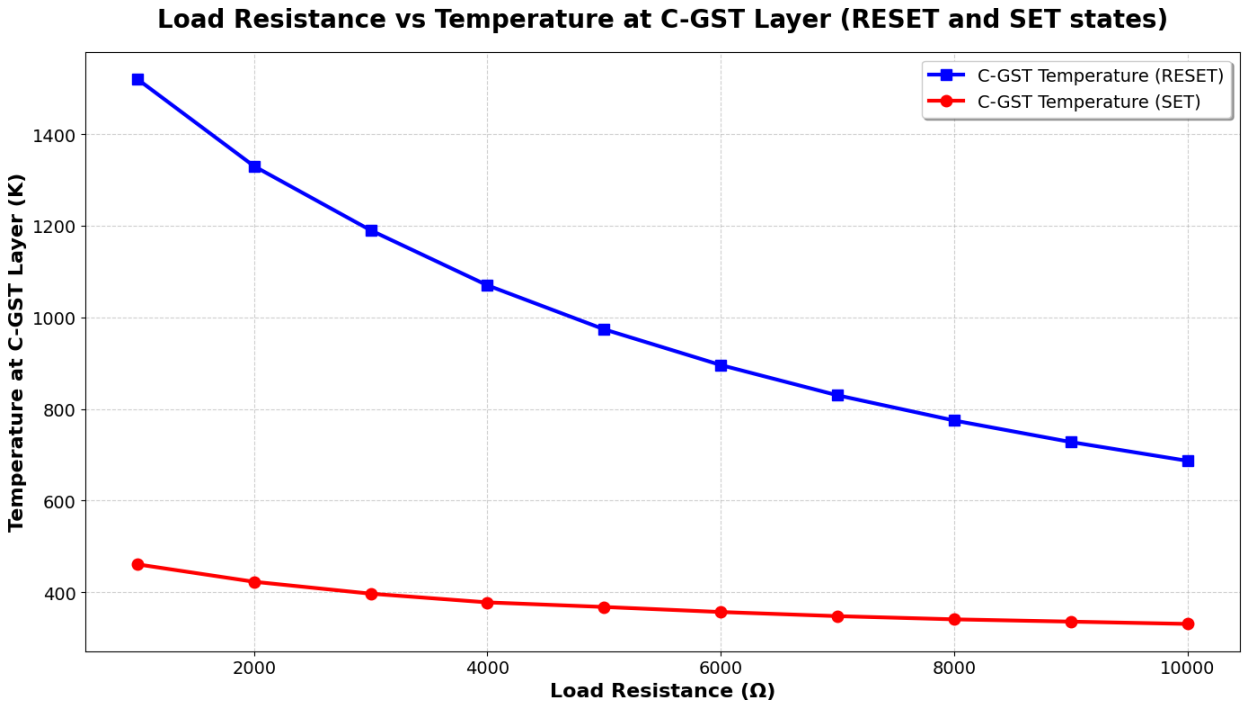
Table 32:

Applied Current (uA) for PRAM Device vsTemperature at C-GST Layer (K)

Applied Current (uA)	Temperature at C-GST Layer (K) for SET state
11	3.07E+02
22	3.35E+02
33	3.81E+02
44	4.45E+02
55	5.27E+02
66	6.28E+02
77	7.48E+02

88	8.85E+02
99	1.04E+03
111	1.23E+03

Fig. 33: Load Resistance (ohm) for PRAM Device vsTemperature at C-GST Layer (K)



The **Fig. 33** shows the relationship between the load resistance (in Ohms, Ω) and the temperature at the C-GST layer (in Kelvin) for both the RESET and SET states of a PRAM device. For the RESET state (blue line with squares), as the load resistance increases from 1000 Ω to 10000 Ω, the temperature at the C-GST layer decreases from approximately 1520 K to 690 K, indicating an inverse relationship. Similarly, for the SET state (red line with circles), the temperature also decreases with increasing load resistance, starting at about 460 K and falling to approximately 330 K over the same resistance range. Notably, for any given load resistance, the temperature in the RESET state is significantly higher than in the SET state.

Table 33:

Load Resistance (ohm) for PRAM Device vs Temperature at C-GST Layer (K)

Resistance (ohm)	Temperature at C-GST Layer (K) for SET state	Temperature at C-GST Layer (K) for RESET state
1000	1.52E+03	4.61E+02
2000	1.33E+03	4.23E+02
3000	1.19E+03	3.97E+02
4000	1.07E+03	3.78E+02
5000	9.74E+02	3.68E+02
6000	8.96E+02	3.57E+02
7000	8.30E+02	3.48E+02
8000	7.75E+02	3.41E+02
9000	7.28E+02	3.36E+02
10000	6.87E+02	3.31E+02