Computer Architecture ELE 475
Problem Set #1

This problem set is **ungraded and not collected**. We will release solutions two weeks after the problem set is released. Please stop by office hours if you have questions.

Problem #1 (10 Points): Compute the Clocks Per Instruction (CPI) of a machine which has an average CPI for ALU operations of 1.1, a CPI for branches/jumps of 3.0, and a hit rate of 60% in the cache. A hit in the cache takes 1 cycle pipelined and a cache miss takes 120 cycles. Assume 22% of instructions are loads, 12% are stores, 20% are branches/jumps and the balance are ALU operations.

Problem #2 (10 Points): You are a processor designer and have to make a decision between building a processor which executes at 1GHz and has an average CPI 1.2 and a processor which executes at 2GHz, but has a CPI of 2. Which is better to build and why?

Problem #3 (20 Points): Page C-82 in H&P5, Problem C.1 a,b,c,d,e,f,g

For problem 3: assume that branches are resolved in the decode stage and that the pipeline has no delay slots. Also, assume for part (d) that early pre-decode is used to determine and fetch the target of a branch in the fetch stage.

Problem #4 (10 Points): Page B-60 in H&P5, Problem B.2 a,b

Problem #5 (10 Points): Draw a circuit diagram for a 2-way set associative cache that can be indexed by bytes which has 8 blocks with a block size of 8-bytes. Show the tag-match logic and the output byte-select mux. Also, assume that it is a 32-bit machine and show the number of bits of the address which goes to each multiplexer and tag-comparator.

Problem #6 (10 Points): For the following code snippet, identify all of the RAW, WAW, and WAR hazards. Provide a list for each hazard. Hint, remember that you have to check more than neighbor instructions.

```
ADD R1, R2, R3
SUB R3, R4, R6
MUL R5, R4, R7
ADDIU R5, R5, 1
SUB R6, R3, R9
ANDI R2, R1, R9
```

Problem #7 (20 Points): Page C-85 in H&P5, Problem C.6 a,b,c,d,e

For problem 7: assume that only sources can use the new addressing mode.

Problem #8 (10 Points): Using graph B.9 on page H&P5 B-25 and table B.8 on page B-24. Which has a lower miss rate, a 256KB direct mapped cache or a 64-KB 8-way cache? Which of the three C's drives the previous result?