

A

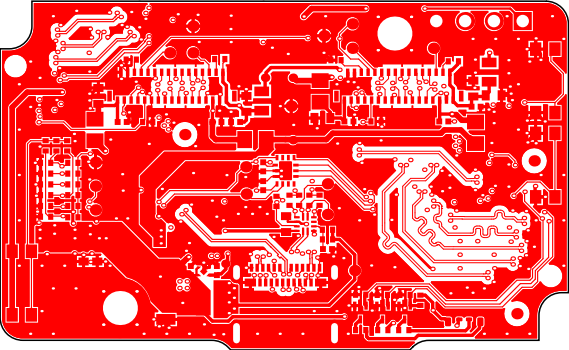
B

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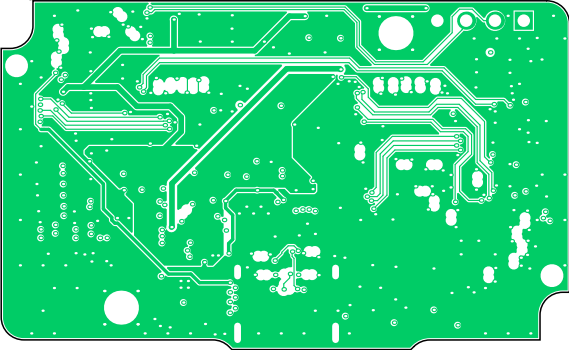
D

E

Top Copper (Scale 1.5:1)



Layer 3 (Scale 1.5:1)



FABRICATION NOTES:

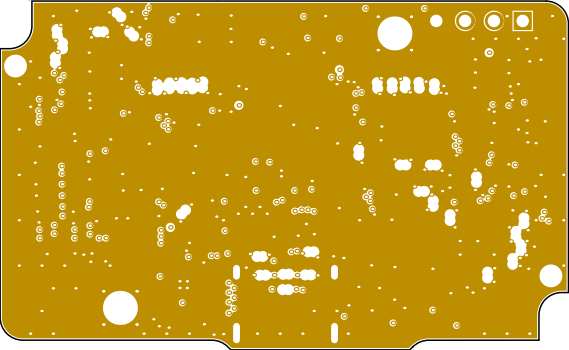
Fabricate per IPC-6011 & IPC-6012 CLASS 2  
Inspect per IPC-A-600 CLASS 2  
Test per IPC-TM-650

- \* PCB has 6 copper layers
- \* Copper thicknesses are finished and include base foil plus Cu plating on plated layers.
- \* PCB thickness: please refer to the Layer Stack Legend
- \* Min. trace width/clearance: 0.1mm/0.1mm
- \* Min. hole drill/ring: 8mil/16mil
- \* Soldermask gang relief is allowed for pads in same footprint, if footprint is NSMD.
- \* Silkscreen, non-conductive epoxy ink, color: white
- \* Solder mask color: black
- \* Remove silkscreen as needed to prevent ink on any exposed copper
- \* Surface finish: ENIG
- \* Hole dimensions are finished size, +/-3mil
- \* Linear board dimension tolerance: +/-10mil
- \* Bow, twist, warp not to exceed 0.75% of greatest diagonal span
- \* PCB shall be UL Recognized printed wiring board (ZPMV2), minimum flammability rating 94V-0
- \* PCB shall be marked with fabricator company or trade name, UL mark, and date code using legend ink on secondary side
- \* All PCBs shall be electrically tested for opens and shorts per gerber. Test marking shall be marked on second side.
- \* GM1 shall be used as PCB outline GKO can be ignored.

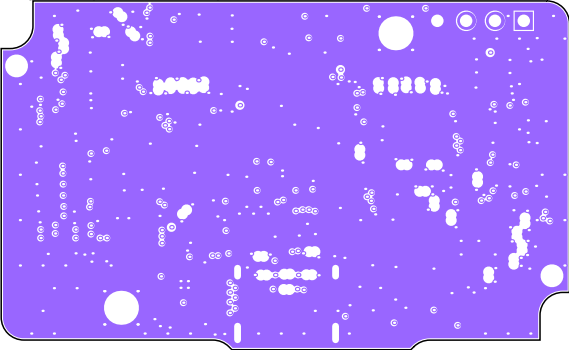
Fabricator shall panelize the PCB using mouse bites and tab routing. V-scoring not allowed.

Controlled impedance differential pairs shall be within +/-10% for 100ohm targets, and +/-10% for 90ohm targets. See Sheet 3 for transmission line details and location of 90ohm differential pairs.

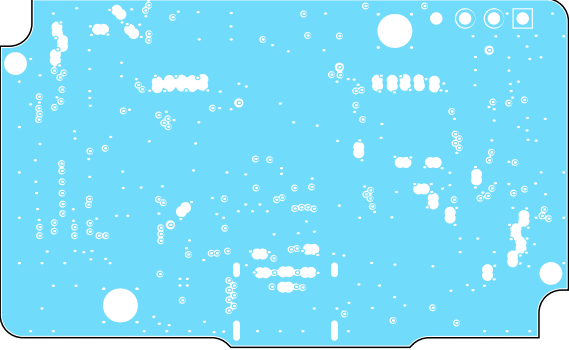
Layer 1 (Scale 1.5:1)



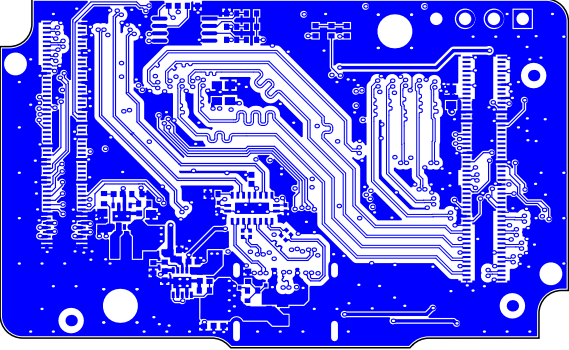
Layer 4 (Scale 1.5:1)



Layer 2 (Scale 1.5:1)



Bottom Layer (Scale 1.5:1)



Title: **DM2080**

Number: D0001093

Revision: R1M1  
E1

Date: 24. 11. 2022 Sheet: 1 of 3

Drawn by: David Malovrh

**LUXonjs**

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Layer Stack Legend

Layer	Thickness	Type	Gerber	Df	Dk
Top Overlay		Legend	GTO		
Top Mask	0.71mil(0.018mm)	Solder Mask	GTS		4,2
Top Copper	1.40mil(0.036mm)	Signal	GTL		
	<b>2.80mil(0.071mm)</b>	<b>Dielectric</b>		<b>0,018</b>	<b>3,8</b>
Layer 1	1.38mil(0.035mm)	Signal	G1		
	<b>4.60mil(0.117mm)</b>	<b>Dielectric</b>		<b>0,017</b>	<b>4,1</b>
Layer 2	1.38mil(0.035mm)	Signal	G2		
	<b>39.00mil(0.991mm)</b>	<b>Dielectric</b>		<b>0,02</b>	<b>4,6</b>
Layer 3	1.38mil(0.035mm)	Signal	G3		
	<b>4.60mil(0.117mm)</b>	<b>Dielectric</b>		<b>0,017</b>	<b>4,1</b>
Layer 4	1.38mil(0.035mm)	Signal	G4		
	<b>2.80mil(0.071mm)</b>	<b>Dielectric</b>		<b>0,018</b>	<b>3,8</b>
Bottom Layer	1.40mil(0.036mm)	Signal	GBL		
Bottom Solder	0.71mil(0.018mm)	Solder Mask	GBS		4,2
Bottom Overlay		Legend	GBO		
Total thickness: 63.53mil(1.614mm)					

Drill Table

Symbol	Count	Hole Size	Plated	Hole Tolerance
⊗	471	8.00mil(0.203mm)	Plated	
○	4	23.62mil(0.600mm)	Plated	
□	4	43.31mil(1.100mm)	Plated	
⊕	2	70.87mil(1.800mm)	Non-Plated	
◇	2	118.11mil(3.000mm)	Plated	
483 Total				

Title: <b>DM2080</b>	
Number: D0001093	Revision: R1M1 E1
Date: 24. 11. 2022	Sheet: 2 of 3
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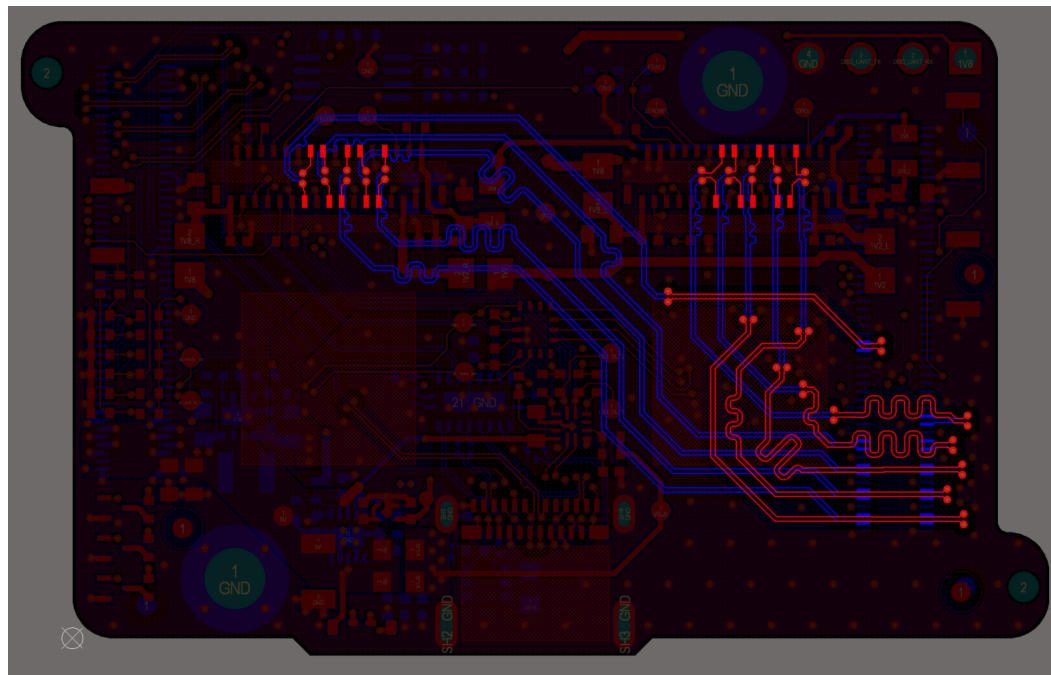
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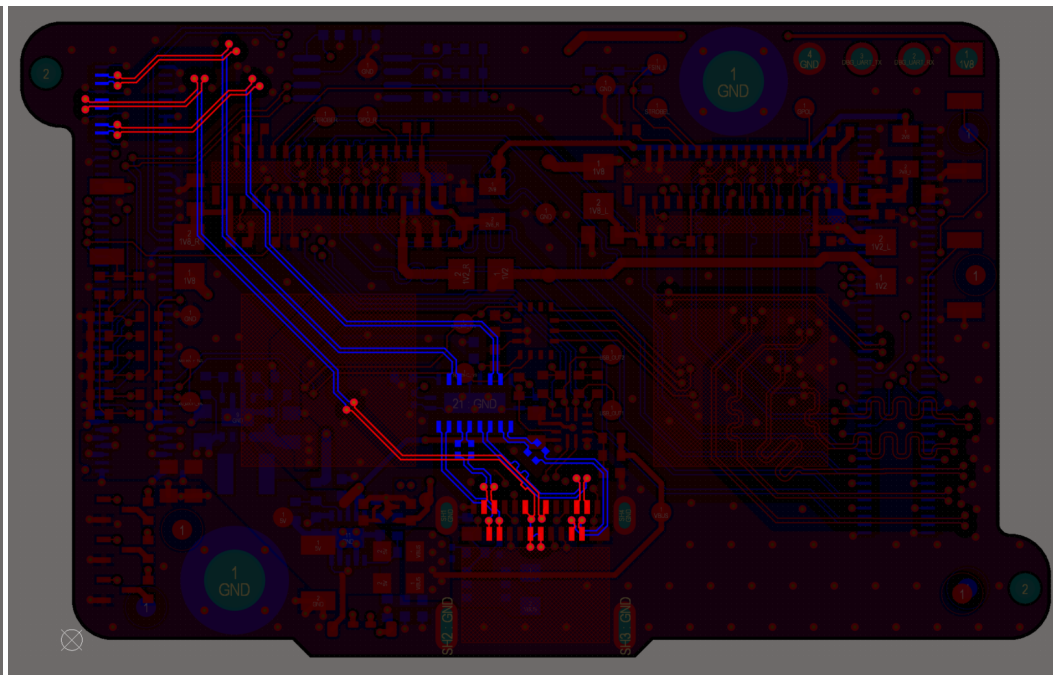
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E

100 OHM (+/-10%) DIFF PAIRS



90 OHM (+/-10%) DIFF PAIRS



Transmission Line Structure Table

Target Impedance	Trace layer	Lower Trace Width	Upper Trace Width	Gap	Reference layers
100	Top Copper	3.5mil(0.089mm)	2.7mil(0.068mm)	5.0mil(0.127mm)	Layer 1
90	Top Copper	4.0mil(0.102mm)	3.2mil(0.081mm)	4.0mil(0.102mm)	Layer 1
100	Bottom Layer	3.5mil(0.089mm)	2.7mil(0.068mm)	5.0mil(0.127mm)	Layer 4
90	Bottom Layer	4.0mil(0.102mm)	3.2mil(0.081mm)	4.0mil(0.102mm)	Layer 4

Title: **DM2080**Number: D0001093 Revision: R1M1  
E1

Date: 24. 11. 2022 Sheet: 3 of 3

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