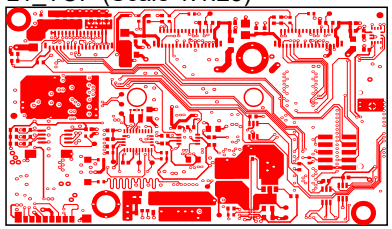
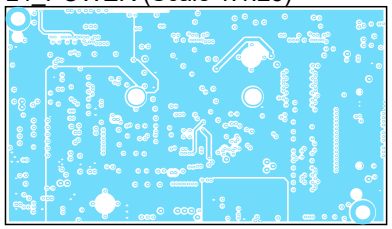
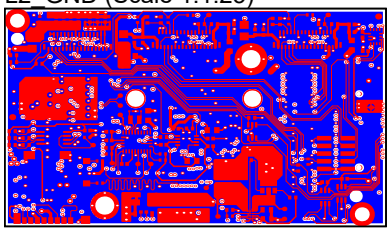
L1_TOP (Scale 1:1.25)



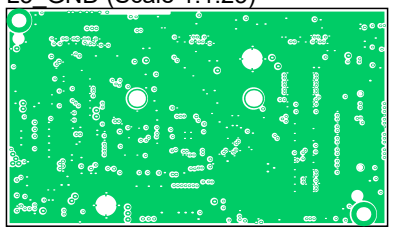
L4_POWER (Scale 1:1.25)



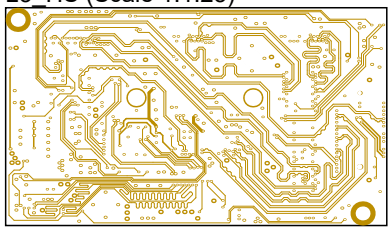
L2_GND (Scale 1:1.25)



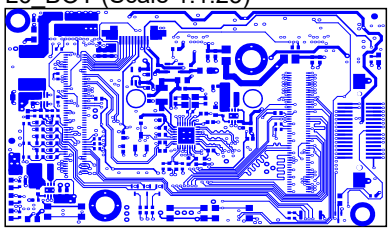
L5_GND (Scale 1:1.25)



L3_HS (Scale 1:1.25)



L6_BOT (Scale 1:1.25)



FABRICATION NOTES:

Fabricate per IPC-6011 & IPC-6012 CLASS 2
Inspect per IPC-A-600 CLASS 2
Test per IPC-TM-650

*** PCB has 6 copper layers**
*** Copper thicknesses are finished and include base foil plus Cu plating on plated layers.**
*** PCB thickness: please refer to the Layer Stack Legend**
*** Min. trace width/clearance: 4/4mil**
*** Min. hole drill/ring: 8mil/16mil**
*** All vias-in-pad shall be plugged and plated over (VIPPO)**
*** Soldermask gang relief is allowed for pads in same footprint, if footprint is NSMD.**
*** Silkscreen, non-conductive epoxy ink, color: white**
*** Remove slikscreen as needed to prevent ink on any exposed copper**
*** Surface finish: ENIG**
*** Hole dimensions are finished size, +/-3mil**
*** Linear board dimension tolerance: +/-10mil**
*** Bow, twist, warp not to exceed 0.75% of greatest diagonal span**
*** PCB shall be UL Recognized printed wiring board (ZPMV2), minimum flammability rating 94V-0**
*** PCB shall be marked with fabricator company or trade name, UL mark, and date code using legend ink on secondary side**
*** All PCBs shall be electrically tested for opens and shorts per gerber. Test marking shall be marked on secondard side.**
*** GM1 shall be used as PCB outline GKO can be ignnored.**

Fabricator shall panelize the PCB using mouse bites and tab routing. V-scoring not allowed.

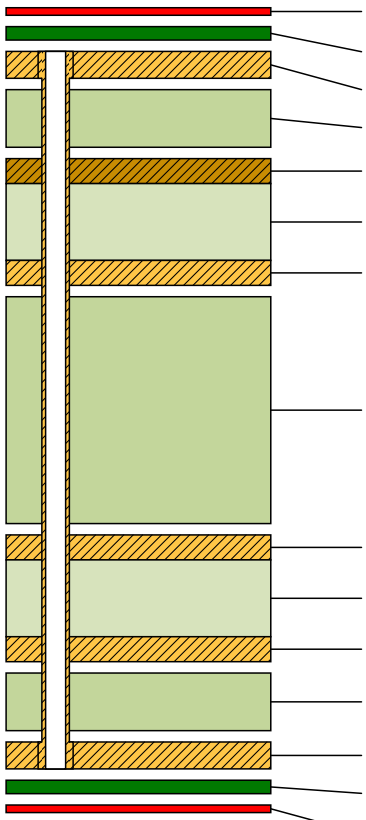
Controlled impedance differential pairs shall be within +/-10% of target impedance. See sheets below for more detail.

Title: ***EL2086***	LUXonjs
Number: D2088000 Revision: R0M0 E0	
Date: 19/05/2023 Sheet: 1 of 4	PROPRIETARY AND CONFIDENTIAL
Drawn by: Eason Lin	THE INFORMATION CONTAINED IN THIS DRAWING IS THE SOLE PROPERTY OF LUXONIS HOLDING CORPORATION. ANY REPRODUCTION IN PART OR AS A WHOLE WITHOUT THE WRITTEN PERMISSION IS PROHIBITED.

Drill Table

Symbol	Count	Hole Size	Plated	Hole Tolerance
◈	345	8.00mil(0.203mm)	Plated	
◎	155	10.00mil(0.254mm)	Plated	
☆	34	12.00mil(0.305mm)	Plated	
B	1	27.56mil(0.700mm)	Non-Plated	
○	1	35.43mil(0.900mm)	Non-Plated	
⊞	2	59.06mil(1.500mm)	Non-Plated	
□	2	90.55mil(2.300mm)	Plated	
✡	2	106.30mil(2.700mm)	Plated	
▽	2	118.11mil(3.000mm)	Plated	
	544 Total			

Layer Stack Legend



Layer	Thickness	Type	Gerber	Df	Dk
Top Overlay		Legend	GTO		
Top Mask	0.70mil(0.018mm)	Solder Mask	GTS		3.8
L1_TOP	1.40mil(0.036mm)	Signal	GTL		
	3.00mil(0.076mm)	*Dielectric*			*4.05*
L2_GND	1.30mil(0.033mm)	Internal Plane	GP1		
	4.00mil(0.102mm)	*Dielectric*			*4.5*
L3_HS	1.30mil(0.033mm)	Signal	G1		
	39.60mil(1.006mm)	*Dielectric*			*4.25*
L4_POWER	1.30mil(0.033mm)	Signal	G2		
	4.00mil(0.102mm)	*Dielectric*			*4.5*
L5_GND	1.30mil(0.033mm)	Signal	G3		
	3.00mil(0.076mm)	*Dielectric*			*4.05*
L6_BOT	1.40mil(0.036mm)	Signal	GBL		
Bottom Mask	0.70mil(0.018mm)	Solder Mask	GBS		3.8
Bottom Overlay		Legend	GBO		

Total thickness: 63.00mil(1.600mm)

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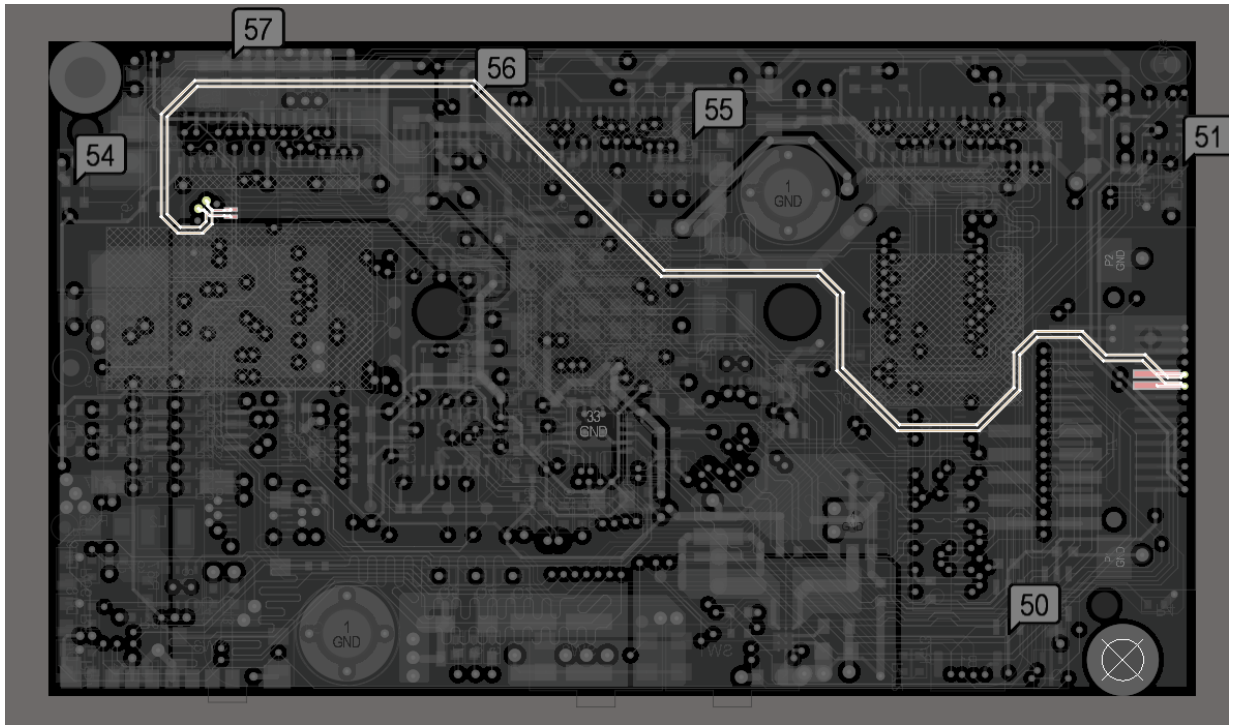
85 OHM (+/-10%) DIFF PAIRS

USB differential pairs



Transmission Line Structure Table

Impedance Id	Target Impedance	Calculated Impedance	Trace layer	Wide Trace Width	Gap	Reference layers	Clearance	Target Tolerance
2	85	90.02	L1_TOP	5.00mil	8.00mil	L2_GND	5.00mil	10%
5	85	80.94	L3_HS	5.50mil	8.00mil	L2_GND,L4_POWER	0.00mil	10%
9	85	90.02	L6_BOT	5.00mil	8.00mil	L5_GND	5.00mil	10%

Title: ***EL2086***	LUXonjs
Number: D2088000 Revision: R0M0 E0	
Date: 19/05/2023 Sheet: 3 of 4	PROPRIETARY AND CONFIDENTIAL
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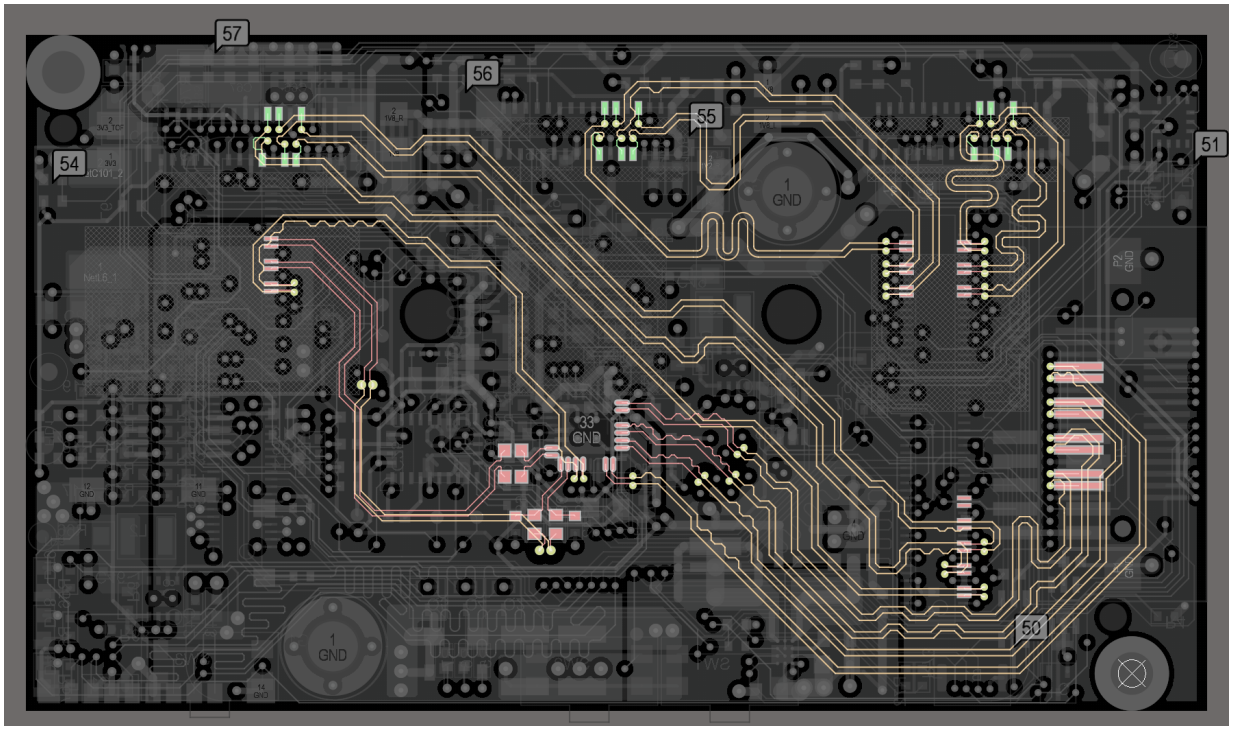
100 OHM (+/-10%) DIFF PAIRS



Transmission Line Structure Table

Impedance Id	Target Impedance	Calculated Impedance	Trace layer	Wide Trace Width	Gap	Reference layers	Clearance	Target Tolerance
1	100	104.76	L1_TOP	3.50mil	8.00mil	L2_GND	5.00mil	10%
4	100	93.48	L3_HS	4.00mil	9.00mil	L2_GND,L4_POWER	0.00mil	10%
8	100	104.76	L6_BOT	3.50mil	8.00mil	L5_GND	5.00mil	10%

Title: ***EL2086***	LUXonjs
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