MODULE INTERFACE

U_POWER_GEN
POWER_GEN.SchDoc
VDD_5V 3V3 2V8 1V8 1V8 1V2 3V3_VCSEL GND

U_BTB_CONN
BTB_CONN.SchDoc
VDD_5V 3V3 1V8 EXT_GPIO3 VBUS_SRC_EN FSYNC/SD0 STRB/SCK BOOT/WS USB ETH_DATA GND

U_ETH_PCIE_CTRL
ETH_PCIE_CTRL.SchDoc
3V3 1V8 ETH_DATA PCIe_CTR_1V8 SDS_DATA SDS_CLK GND

U_CONNECTOR_B
CONNECTOR_B.SchDoc
VDD_5V 1V8 EXT_FSYNC_1V8 IMU_CTRL EXT_GPIO3 VBUS_SRC_EN BOOT/WS_SEL FSYNC/SD0 STRB/SCK BOOT/WS USB RGB_LED BB_JTAG I2C4 I2C0 SOM_FSYNC PCIe_CTR_1V8 SDS_DATA SDS_CLK STRB CAM_R_PWM GND

U_CONNECTOR_A
CONNECTOR_A.SchDoc
MX_SPI0 EXT_FSYNC_1V8 MIPI_CAM_A CTL_CAM_A I2C1 BOOT/WS_SEL I2C2 MIPI_CAM_B CTL_CAM_B uSD_Card SOM_FSYNC 2485_WAKEUP 2485_PGOOD MODULE_nRST MIPI_CAM_C I2C3 GND

U_EEPROM
EEPROM.SchDoc
1V8 I2C0 GND

U_BOOT_JTAG_AUX
BOOT_JTAG_AUX.SchDoc
VDD_5V 3V3 1V8 I2C4 BB_JTAG RGB_LED uSD_Card 2485_WAKEUP 2485_PGOOD MODULE_nRST SOM_FSYNC I2C3 STRB GND

U_IMU
IMU.SchDoc
3V3 1V8 IMU_CTRL MX_SPI0 GND

U_TOF_VGA
TOF_VGA.SchDoc
3V3_VCSEL 1V8 3V3 MIPI_CAM_A CTL_CAM_A I2C1 STRB SOM_FSYNC GND

U_LEFT_CCM
LEFT_CCM.SchDoc
I2C2 MIPI_CAM_B CTL_CAM_B 2V8 1V8 1V2 SOM_FSYNC STRB GND

U_RIGHT_CCM
RIGHT_CCM.SchDoc
CTL_CAM_B MIPI_CAM_C I2C3 2V8 1V8 1V2 SOM_FSYNC STRB CAM_R_PWM GND

U_DOT_LED
DOT_LED
VDD_5V I2C2 STRB GND

U_Project_Information
Project_Information.SchDoc

MTG1 9774030943R GND
MTG2 9774030943R GND

FID1 FID2 FID3 FID4

Title	EL2086		Luxonis Holding 1925 Harmony Park Drive Westminster, CO 80234 United States
Size: Tabloid	Number: D2088000	Revision: R0M0E0	
Date: 19/05/2023	Time: 14:08:52	Sheet 1 of 14	
Drawn by: Eason Lin			

Cannot open file
C:\Users\BrianLuxonis\

Project: ***EL2086***
Current Revision: ***R0M0E0***

EL2086 *Revision History:*

Date	Revision	Reason for Change	Changes Implemented
22/Aug/2022	Iniital Release -> R0M0E0		

Title ***EL2086***			***Luxonis Holding*** ***1925 Harmony Park Drive*** ***Westminster, CO*** ***80234*** ***United States***	Cannot open file C:\Users\BrianLuxonis\
Size: Tabloid	Number:D2088000	Revision:R0M0E0		
Date: 19/05/2023 Time: 14:08:52		Sheet 2 of 14		
Drawn by: ***Eason Lin***				

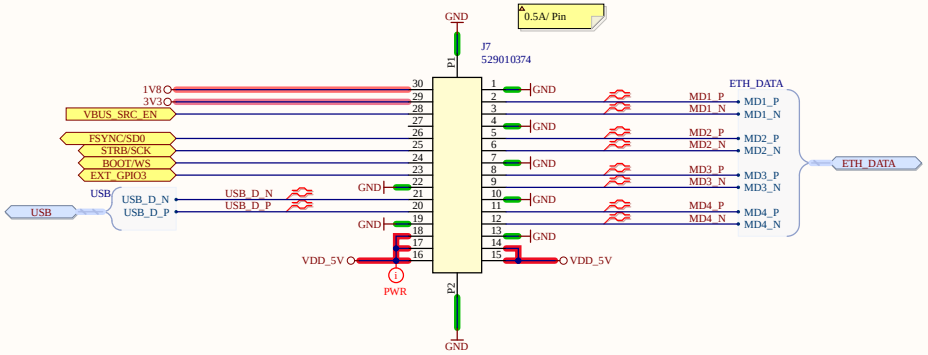
VDD_5V — VDD_5V

3V3 — 3V3

1V8 — 1V8

GND — GND

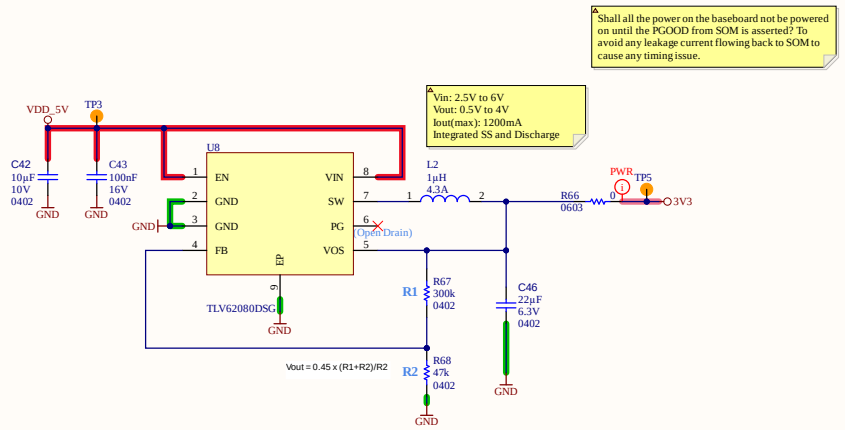
BTB CONNECTOR



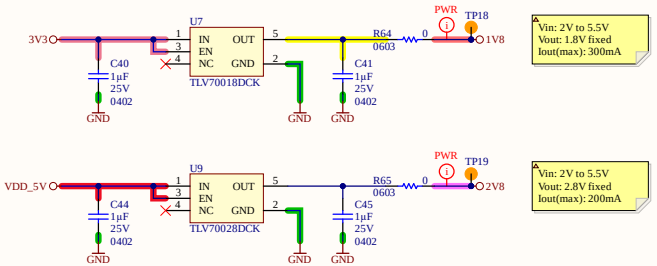
Title: EL2086			Luxonis Holding 1925 Harmony Park Drive Westminster, CO 80234 United States
Size: Tabloid	Number: D2088000	Revision: R0M0E0	Cannot open file C:\Users\BrianLuxonis\
Date: 19/05/2023 Time: 14:08:52	Sheet 3 of 14		
Drawn by: Eason Lin			

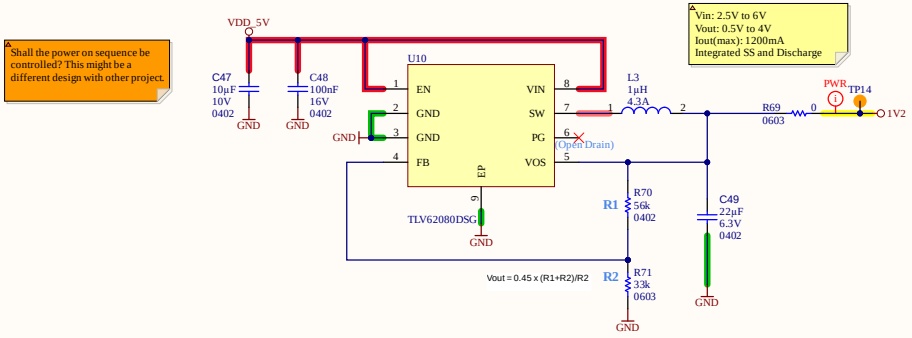
VDD_5V — VDD_5V
3V3 — 3V3
1V8 — 1V8
2V8 — 2V8
1V2 — 1V2
GND — GND
3V3_VCSEL — 3V3_VCSEL

3V3 Buck Converter

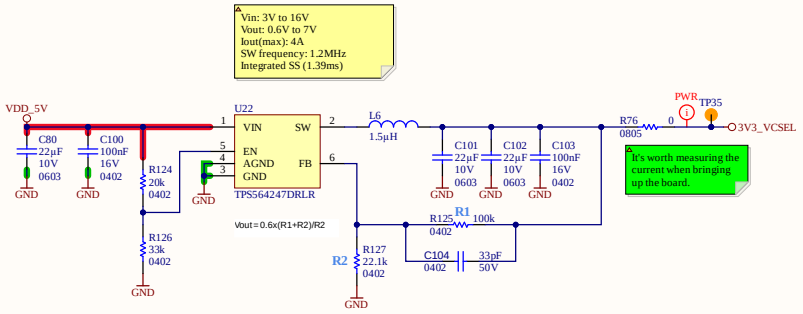


POWER FOR CAMERA MODULE

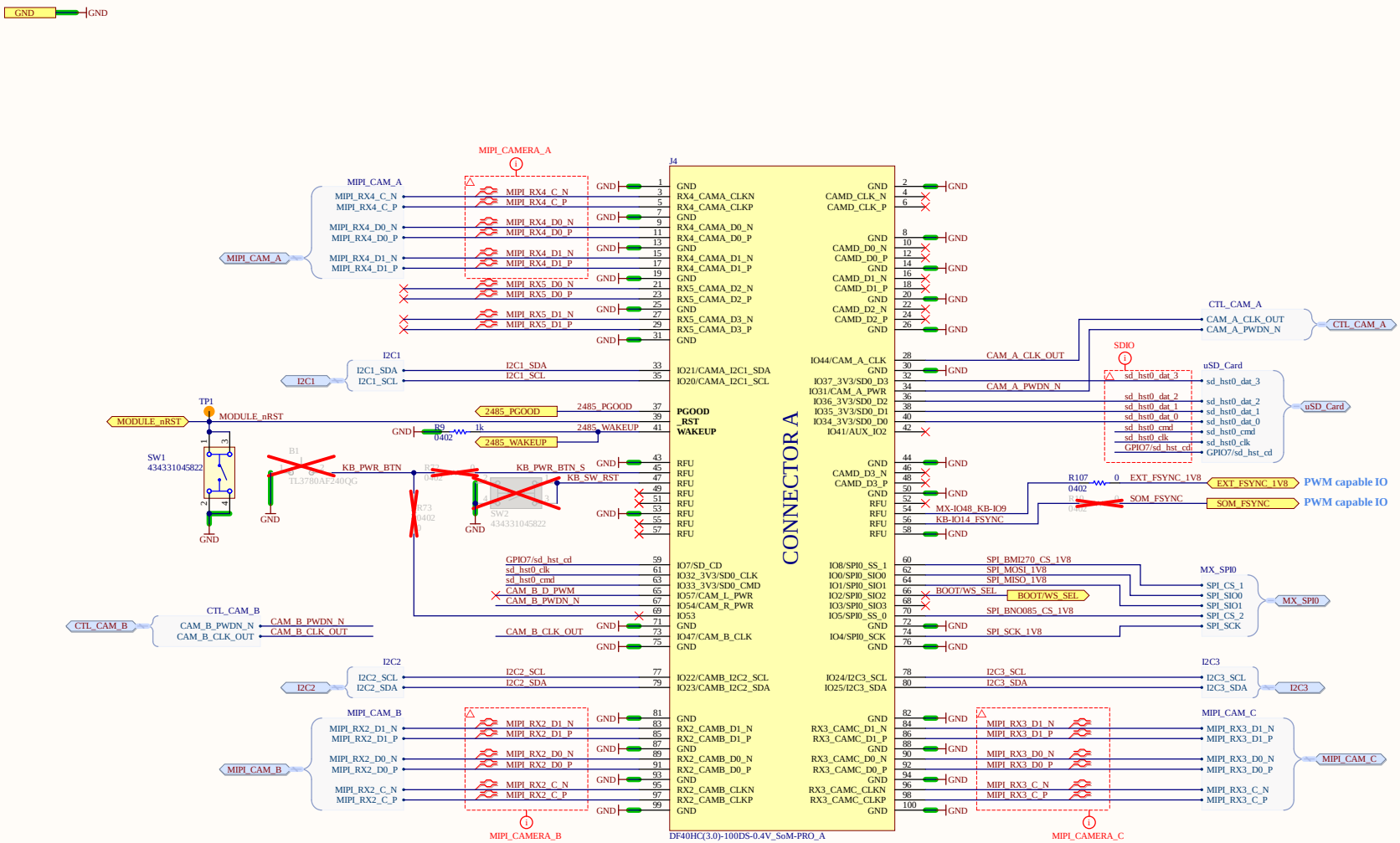




3V3_VCSEL Buck Converter

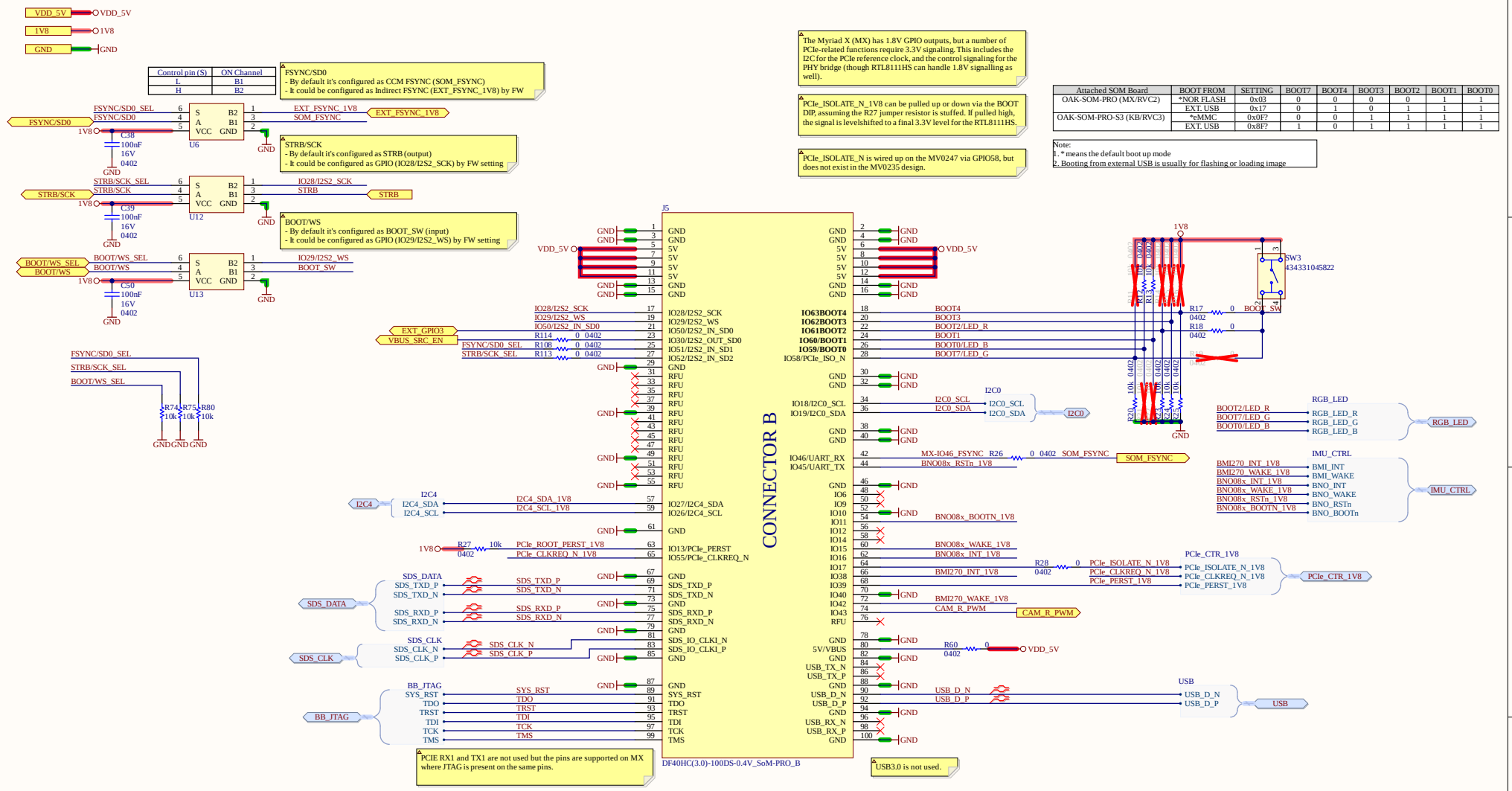


Title	EL2086		Luxonis Holding 1925 Harmony Park Drive Westminster, CO 80234 United States
Size: Tabloid	Number: D2088000	Revision: R0M0E0	Cannot open file C:\Users\BrianLuxonis\
Date: 19/05/2023	Time: 14:08:52	Sheet 4 of 14	
Drawn by: Eason Lin			

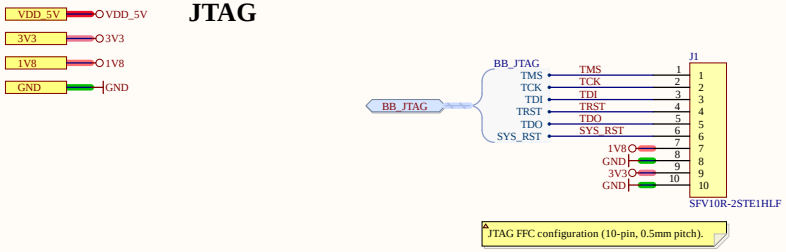


IMU SPI is length matched between connector and IMU. QSPI bus is length matched between connector and header pads.

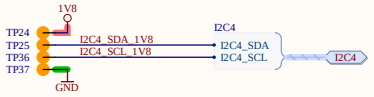
Title: EL2086			Luxonis Holding 1925 Harmony Park Drive Westminster, CO 80234 United States
Size: Tabloid	Number: D2088000	Revision: R0M0E0	Cannot open file C:\Users\BrianLuxonis\
Date: 19/05/2023 Time: 14:08:52	Sheet 5 of 14		
Drawn by: Eason Lin			


VDD_5V
1V8
GND
Control pin (S) | ON Channel
L | B1
H | B2
FSYNC/SD0
- By default it's configured as CCM FSYNC (SOM_FSYNC)
- It could be configured as Indirect FSYNC (EXT_FSYNC_1V8) by FW
STRB/SCK
- By default it's configured as STRB (output)
- It could be configured as GPIO (IO28/I2S2_SCK) by FW setting
BOOT/WS
- By default it's configured as BOOT_SW (input)
- It could be configured as GPIO (IO29/I2S2_WS) by FW setting
The Myriad X (MX) has 1.8V GPIO outputs, but a number of PCIe-related functions require 3.3V signaling. This includes the I2C for the PCIe reference clock, and the control signaling for the PHY bridge (though RTL8111HS can handle 1.8V signalling as well).
PCIe_ISOLATE_N_1V8 can be pulled up or down via the BOOT DIP, assuming the R27 jumper resistor is stuffed. If pulled high, the signal is levelshifted to a final 3.3V level for the RTL8111HS.
PCIe_ISOLATE_N is wired up on the MV0247 via GPIO58, but does not exist in the MV0235 design.
Attached SOM Board | BOOT FROM | SETTING | BOOT7 | BOOT4 | BOOT3 | BOOT2 | BOOT1 | BOOT0
OAK-SOM-PRO (MX/RVC2) | *NOR FLASH | 0x03 | 0 | 0 | 0 | 0 | 1 | 1
EXT. USB | 0x17 | 0 | 1 | 0 | 1 | 1 | 1
OAK-SOM-PRO-S3 (KB/RVC3) | *eMMC | 0x0F? | 0 | 0 | 1 | 1 | 1 | 1
EXT. USB | 0x8F? | 1 | 0 | 1 | 1 | 1 | 1
Note:
1. * means the default boot up mode
2. Booting from external USB is usually for flashing or loading image
CONNECTOR B
DF40HC(3.0)-100DS-0.4V_SoM-PRO_B
PCIE RX1 and TX1 are not used but the pins are supported on MX where JTAG is present on the same pins.
USB3.0 is not used.
Title EL2086
Size: Tabloid
Number:D2088000
Revision:R0M0E0
Date: 19/05/2023
Time: 14:08:52
Sheet 6 of 14
Drawn by: Eason Lin
Luxonis Holding
1925 Harmony Park Drive
Westminster, CO
80234
United States

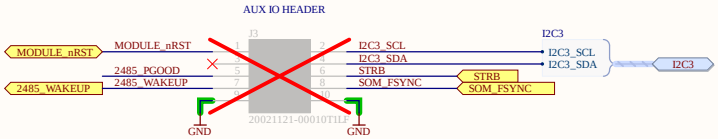
JTAG



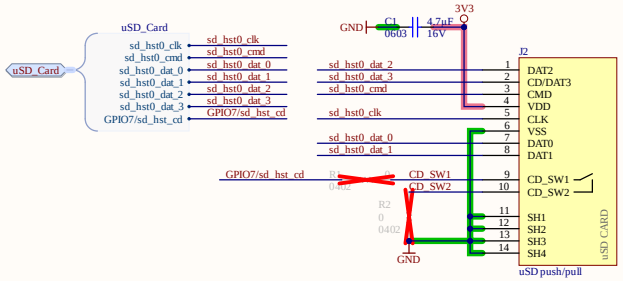
KB UART DEBUG



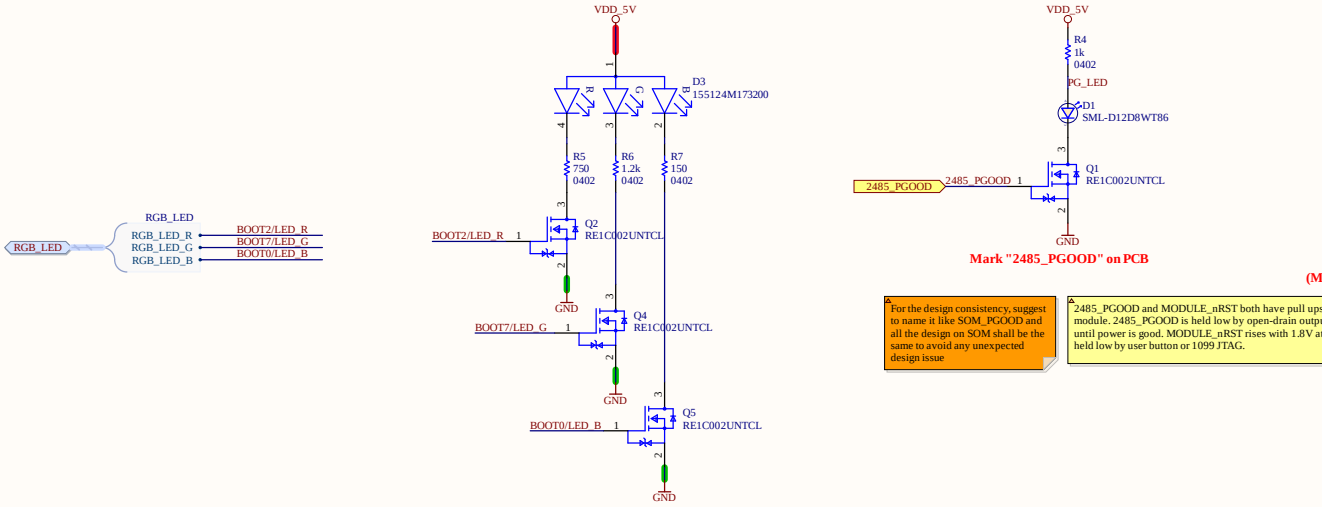
AUX IO HEADER



uSD SLOT

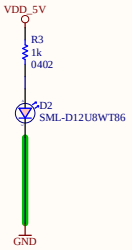


LED INDICATOR



Mark "2485_PGOOD" on PCB

Mark "nRST" on PCB
(MODULE_nRST is not used. Revmoe the circuitry.)



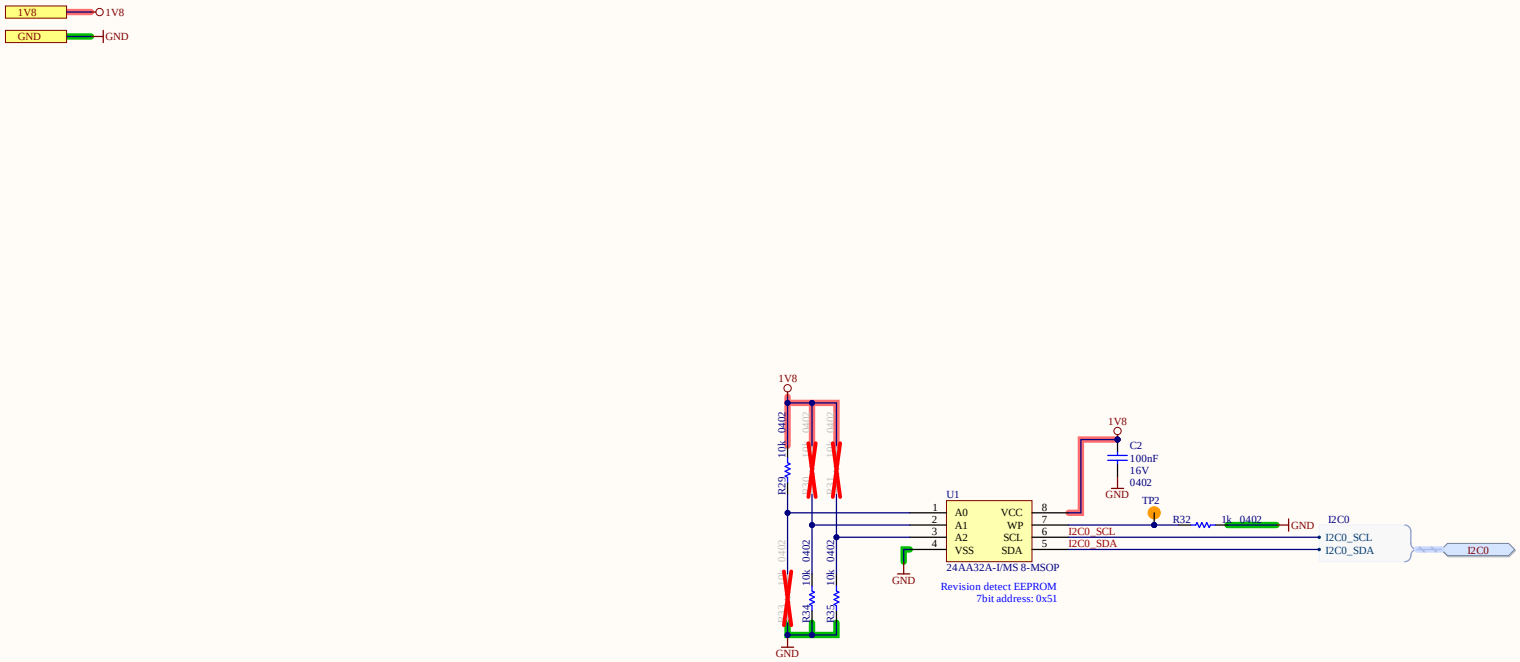
Mark "5V" on PCB

For the design consistency, suggest to name it like SOM_PGOOD and all the design on SOM shall be the same to avoid any unexpected design issue

2485_PGOOD and MODULE_nRST both have pull ups to 1.8V on 1099 module. 2485_PGOOD is held low by open-drain output on 1099 PMIC until power is good. MODULE_nRST rises with 1.8V at POR, but can be held low by user button or 1099 JTAG.

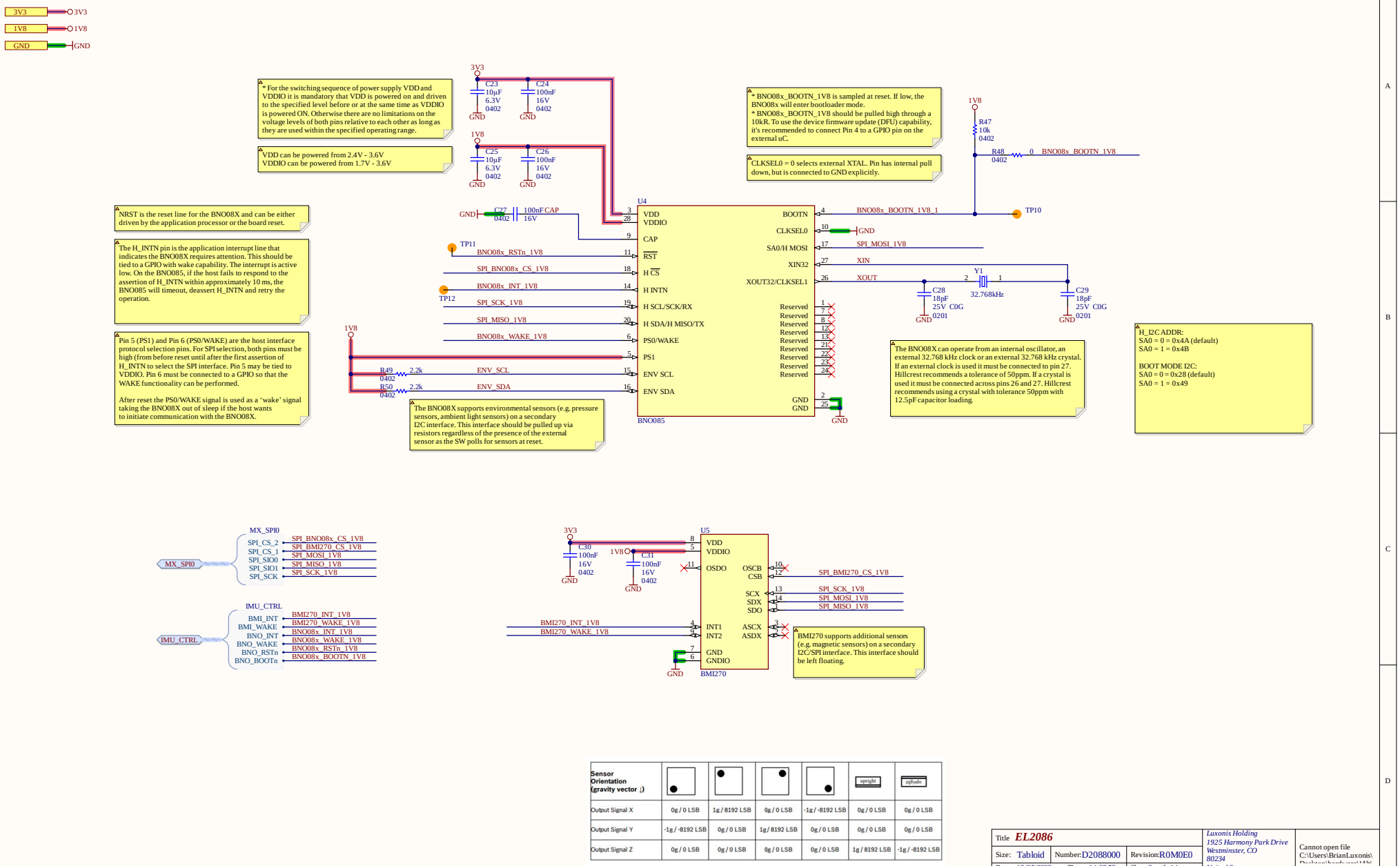
Title: EL2086			Luxonis Holding 1925 Harmony Park Drive Westminster, CO 80234 United States
Size: Tabloid	Number: D2088000	Revision: R0M0E0	
Date: 19/05/2023 Time: 14:08:53	Sheet 7 of 14		
Drawn by: Eason Lin			

Cannot open file C:\Users\BrianLuxonis\

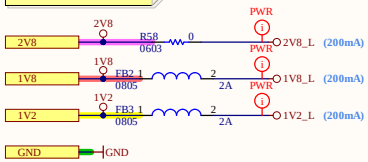


Title **EL2086**			*Luxonis Holding* *1925 Harmony Park Drive* *Westminster, CO* *80234* *United States*
Size: Tabloid	Number: D2088000	Revision: R0M0E0	
Date: 19/05/2023 Time: 14:08:53	Sheet 8 of 14		
Drawn by: ***Eason Lin***			

Cannot open file C:\Users\BrianLuxonis\


3V3
1V8
GND
* For the switching sequence of power supply VDD and VDDIO it is mandatory that VDD is powered on and driven to the specified level before or at the same time as VDDIO is powered ON. Otherwise there are no limitations on the voltage levels of both pins relative to each other as long as they are used within the specified operating range.
VDD can be powered from 2.4V - 3.6V
VDDIO can be powered from 1.7V - 3.6V
C23 10µF 6.3V 0402
C24 100nF 16V 0402
C25 10µF 6.3V 0402
C26 100nF 16V 0402
* BNO08x_BOOTN_1V8 is sampled at reset. If low, the BNO08x will enter bootloader mode.
* BNO08x_BOOTN_1V8 should be pulled high through a 10kR. To use the device firmware update (DFU) capability, it's recommended to connect Pin 4 to a GPIO pin on the external uC.
CLKSEL0 = 0 selects external XTAL. Pin has internal pull down, but is connected to GND explicitly.
R47 10k 0402
R48 0 0402
BNO08x_BOOTN_1V8
NRST is the reset line for the BNO08X and can be either driven by the application processor or the board reset.
The H_INTN pin is the application interrupt line that indicates the BNO08X requires attention. This should be tied to a GPIO with wake capability. The interrupt is active low. On the BNO085, if the host fails to respond to the assertion of H_INTN within approximately 10 ms, the BNO085 will timeout, deassert H_INTN and retry the operation.
Pin 5 (PS1) and Pin 6 (PS0/WAKE) are the host interface protocol selection pins. For SPI selection, both pins must be high (from before reset until after the first assertion of H_INTN to select the SPI interface. Pin 5 may be tied to VDDIO. Pin 6 must be connected to a GPIO so that the WAKE functionality can be performed.
After reset the PS0/WAKE signal is used as a 'wake' signal taking the BNO08X out of sleep if the host wants to initiate communication with the BNO08X.
C27 100nF CAP 16V 0402
U4
VDD
VDDIO
CAP
RST
H CS
H INTN
H SCL/SCK/RX
H SDA/H MISO/TX
PS0/WAKE
PS1
ENV SCL
ENV SDA
BOOTN
CLKSEL0
SA0/H MOSI
XIN32
XOUT32/CLKSEL1
Reserved
GND
BNO085
TP10
TP11
TP12
BNO08x_RSTn_1V8
SPI_BNO08x_CS_1V8
BNO08x_INT_1V8
SPI_SCK_1V8
SPI_MISO_1V8
BNO08x_WAKE_1V8
SPI_MOSI_1V8
XIN
XOUT
Y1 32.768kHz
C28 18pF 25V C0G 0201
C29 18pF 25V C0G 0201
R49 2.2k 0402
R50 2.2k 0402
ENV_SCL
ENV_SDA
The BNO08X supports environmental sensors (e.g. pressure sensors, ambient light sensors) on a secondary I2C interface. This interface should be pulled up via resistors regardless of the presence of the external sensor as the SW polls for sensors at reset.
The BNO08X can operate from an internal oscillator, an external 32.768 kHz clock or an external 32.768 kHz crystal. If an external clock is used it must be connected to pin 27. Hillcrest recommends a tolerance of 50ppm. If a crystal is used it must be connected across pins 26 and 27. Hillcrest recommends using a crystal with tolerance 50ppm with 12.5pF capacitor loading.
H_I2C ADDR:
SA0 = 0 = 0x4A (default)
SA0 = 1 = 0x4B
BOOT MODE I2C:
SA0 = 0 = 0x28 (default)
SA0 = 1 = 0x49
MX_SPI0
SPI_CS_2
SPI_CS_1
SPI_SIO0
SPI_SIO1
SPI_SCK
IMU_CTRL
BMI_INT
BMI_WAKE
BNO_INT
BNO_WAKE
BNO_RSTn
BNO_BOOTn
BMI270_INT_1V8
BMI270_WAKE_1V8
BNO08x_INT_1V8
BNO08x_WAKE_1V8
BNO08x_RSTn_1V8
BNO08x_BOOTN_1V8
U5
VDD
VDDIO
OSDO
OSCB
CSB
SCX
SDX
SDO
INT1
INT2
ASCX
ASDX
GND
GNDIO
BMI270
C30 100nF 16V 0402
C31 100nF 16V 0402
SPI_BMI270_CS_1V8
SPI_SCK_1V8
SPI_MOSI_1V8
SPI_MISO_1V8
BMI270 supports additional sensors (e.g. magnetic sensors) on a secondary I2C/SPI interface. This interface should be left floating.
Sensor Orientation (gravity vector ↓)
upright
upside down
Output Signal X
0g / 0 LSB
1g / 8192 LSB
-1g / -8192 LSB
Output Signal Y
Output Signal Z
Title EL2086
Size: Tabloid
Number: D2088000
Revision: R0M0E0
Date: 19/05/2023
Time: 14:08:53
Sheet 9 of 14
Drawn by: Eason Lin
Luxonis Holding
1925 Harmony Park Drive
Westminster, CO
80234
United States
Cannot open file
C:\Users\BrianLuxonis\

Place FBs and caps close to their associated camera connector.



Design to support 200mA for each power rail to have the max. compatibility of each image sensor. The max. rated current/ pin of the FPC connector is also 200mA.

OV9282 has the sequence requirement of power up and down. Not sure if this is controlled by the design inside the ArduCam module.

MODULE & SENSOR INFORMATION			
MODULE	TBD	I2C Clock Rate	400kHz (max)
SENSOR	OV9282 1 Mega pixel CMOS 1/4 inch	I2C Address (8 bits)	SLASEL (SID) = L: 0xC0 SLASEL (SID) = H: 0x20
MAX RESOLUTION	1280x800 @ 120 fps	Sensor Clock Input	6 - 27MHz

OV9282

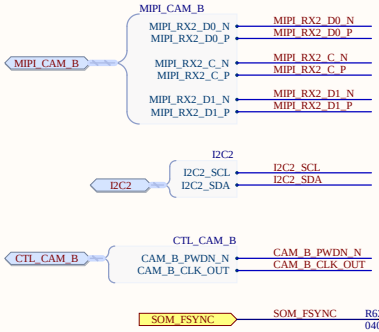
Supply Name		Voltage	Max Current
Module	Sensor		
DOVDD	VDD-IO	1.8V	4mA
DVDD	VDD-D	1.2V	98mA
AVDD	VDD-A	2.8V	30mA

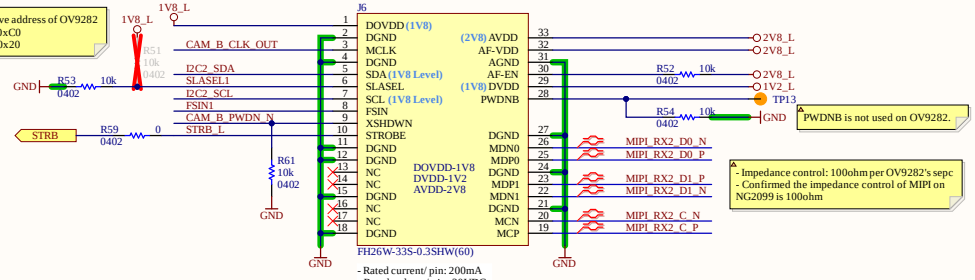
The above spec is from OV9282 because there is no spec of OV9782 on hand.

From OV9282 (1MP image sensor, 120 fps)
- XSHUTDOWN: reset and power down (internal pull down res)
- FSIN (FSIN/VSYNC): frame sync input/ vertical sync output
- STROBE (STROBE): frame exposure output indicator
- SLASEL (SID): SCCB ID select pin
- MCLK (XVCLK): system input clock
- SDA (SDA): SCCB (serial camera control bus) data
- SCL (SCL): SCCB input clock

Mark "LEFT" on PCB
Place so that is the module's left camera.

Slave address of OV9282
L: 0xC0
H: 0x20

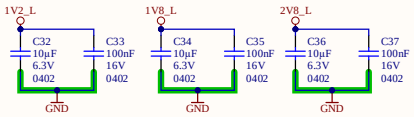




- Rated current/ pin: 200mA
- Rated voltage/ pin: 30VDC

PWDNB is not used on OV9282.

- Impedance control: 100ohm per OV9282's sepc
- Confirmed the impedance control of MIPI on NG2099 is 100ohm



Close to CCM FPC

Because the stereo pair of OV9282 modules hard wired to CAM_B (below) no additional reset cirucitry is required to account for different conditions. This means that "CAM1" (Left) is reset via CAM_PWDN, and "CAM2" (Right), is reset via CAM_PWM. This also means that the signal CAM_AUX_IO1 is no longer required here, as that was only possible if the stereo pair were connected to CAM_C or CAM_D

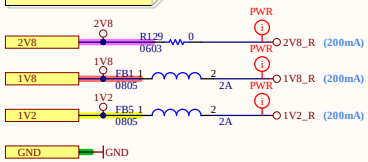
OV9282 sensor I2C address may be changed via I2C protocol. Therefore, in order to assign different I2C address to the sensors on the same I2C bus, one needs to hold the reset the all sensors except one and assign a unique I2C address to the active sensor. This routine should be applied for all sensors in the initialization routine.

CAMERA CONNECTOR RESET CONNECTION TABLE

CAM NO	CAMERA CONNECTOR			
	CAM_A	CAM_B	CAM_C	CAM_D
CAM_1	CAM_PWDN	CAM_PWDN	CAM_PWDN	CAM_PWDN
CAM_2	CAM_PWM	CAM_PWM	CAM_AUX_IO1	CAM_AUX_IO1

Title	EL2086		Luxonis Holding 1925 Harmony Park Drive Westminster, CO 80234 United States
Size: Tabloid	Number: D2088000	Revision: R0M0E0	
Date: 19/05/2023 Time: 14:08:53	Sheet 10 of 14		
Drawn by: Eason Lin			Cannot open file C:\Users\BrianLuxonis\

Place FBs and caps close to their associated camera connector.



Design to support 200mA for each power rail to have the max. compatibility of each image sensor. The max. rated current/ pin of the FPC connector is also 200mA.

OV9282 has the sequence requirement of power up and down. Not sure if this is controlled by the design inside the ArduCam module.

MODULE & SENSOR INFORMATION			
MODULE	TBD	I2C Clock Rate	400kHz (max)
SENSOR	OV9282 1 Mega pixel CMOS 1/4 inch	I2C Address (8 bits)	SLASEL (SID) = L: 0xC0 SLASEL (SID) = H: 0x20
MAX RESOLUTION	1280x800 @ 120 fps	Sensor Clock Input	6 - 27MHz

OV9282

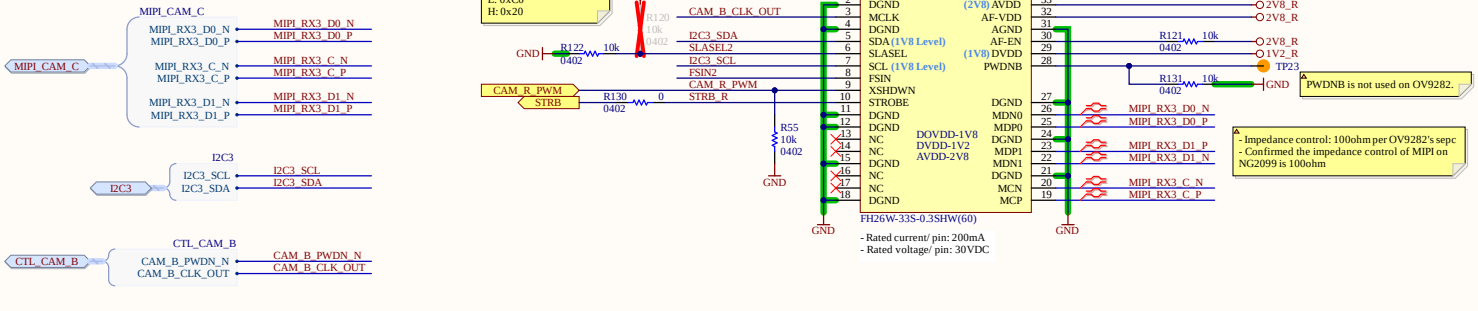
Supply Name		Voltage	Max Current
Module	Sensor		
DOVDD	VDD-IO	1.8V	4mA
DVDD	VDD-D	1.2V	98mA
AVDD	VDD-A	2.8V	30mA

The above spec is from OV9282. It's the same with OV9782 (same sensors, color one w/ bayer filter, grayscale w/out it)

From OV9282 (1MP image sensor, 120 fps)
- XSHUTDOWN: reset and power down (internal pull down res)
- FSIN (FSIN/VSYNC): frame sync input/ vertical sync output
- STROBE (STROBE): frame exposure output indicator
- SLASEL (SID): SCCB ID select pin
- MCLK (XVCLK): system input clock
- SDA (SDA): SCCB (serial camera control bus) data
- SCL (SCL): SCCB input clock

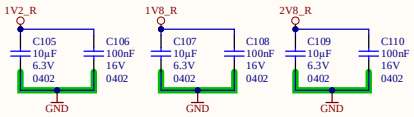
Mark "RIGHT" on PCB
Place so that is the module's right camera.

Slave address of OV9282
L: 0xC0
H: 0x20



- Rated current/ pin: 200mA
- Rated voltage/ pin: 30VDC

- Impedance control: 100ohm per OV9282's sepc
- Confirmed the impedance control of MIPI on NG2099 is 100ohm



Close to CCM FPC

Because the stereo pair of OV9282 modules hard wired to CAM_B (below) no additional reset cirucitry is required to account for different conditions. This means that "CAM1" (Left) is reset via CAM_PWDN, and "CAM2" (Right), is reset via CAM_PWM. This also means that the signal CAM_AUX_IO1 is no longer required here, as that was only possible if the stereo pair were connected to CAM_C or CAM_D

OV9282 sensor I2C address may be changed via I2C protocol. Therefore, in order to assign different I2C address to the sensors on the same I2C bus, one needs to hold the reset the all sensors except one and assign a unique I2C address to the active sensor. This routine should be applied for all sensors in the initialization routine.

CAMERA CONNECTOR RESET CONNECTION TABLE

CAM NO	CAMERA CONNECTOR			
	CAM_A	CAM_B	CAM_C	CAM_D
CAM_1	CAM_PWDN	CAM_PWDN	CAM_PWDN	CAM_PWDN
CAM_2	CAM_PWM	CAM_PWM	CAM_AUX_IO1	CAM_AUX_IO1

Title: EL2086			Luxonis Holding 1925 Harmony Park Drive Westminster, CO 80234 United States
Size: Tabloid	Number: D2088000	Revision: R0M0E0	Cannot open file C:\Users\BrianLuxonis\
Date: 19/05/2023 Time: 14:08:53	Sheet 11 of 14		
Drawn by: Eason Lin			

TO TOF MODULE

3V3 — 3V3
1V8 — 1V8
GND — GND
3V3_VCSEL — 3V3_VCSEL

FB4 2A 0805
3V3 — 1 — 2 — TP20 — 3V3_TOF
C56 10µF 6.3V 0402
C57 10µF 6.3V 0402
C58 100nF 10V 0402
C59 100nF 10V 0402
GND

It's worth measuring the current when bringing up the board.

There is a LOT of current on VCSEL_3V3. Suggest to put LARGE capacitors to provide enough current to the VCSEL for illumination.

3V3_VCSEL
C66 150µF 1411
C67 150µF 1411
C60 10µF 6.3V 0402
C61 10µF 6.3V 0402
C62 10µF 6.3V 0402
C63 100nF 10V 0402
C64 100nF 10V 0402
C65 100nF 10V 0402
GND

I2C1
I2C1 — I2C1_SCL, I2C1_SDA — I2C1_SCL, I2C1_SDA

MIPI_CAM_A
MIPI_CAM_A — MIPI_RX4_C_P, MIPI_RX4_C_N, MIPI_RX4_D0_P, MIPI_RX4_D0_N, MIPI_RX4_D1_P, MIPI_RX4_D1_N

CTL_CAM_A
CTL_CAM_A — CAM_A_CLK_OUT, CAM_A_PWDN_N

SOM_FSYNC — SOM_FSYNC — R96 0 0402 — FSIN3

Supply Information

Supply Name emb. Module	Sensor	Voltage	Max Current
DOVDD	VDD-IO	1.8V	2.5mA
DVDD	VDD-D	1.05V	52mA
AVDD	VDD-A	2.8V	50mA
Supply CBA ext.			
VDD_VCC		3.3V	1000mA
VDD_VCSEL		3.3V	3500mA
DOVDD		1.8V	

MIPI speed of S5K33DXX: 1.6Gbps/ lane

I2C level of S5K33DXX: 1V8

Input clock requirement of S5K33DXX: 6 to 64MHz

I2C address of S5K33DXX
- L: 20h/21h (Default)
- H: 5Ah/5Bh

R95 10k 0402 — GND

J9
MIPI_RX4_C_P 19
MIPI_RX4_C_N 20
MIPI_RX4_D0_N 26
MIPI_RX4_D0_P 25
MIPI_RX4_D1_N 22
MIPI_RX4_D1_P 23
I2C1_SDA 5
I2C1_SCL 7
STRB — R97 0 0402 — STRB_TOF — PWR 10
1V8 — 1
CAM_A_CLK_OUT 3
1V8 — R93 10k 0402 — CAM_A_PWDN_N 9
FSIN3 8
1V8 — R94 10k 0402 — SLASEL 6

MCP, MCN, D0N, D0P, D1N, D1P, SDA, SCL, STROBE, IOVDD_TOF, MCLK, RST, FSIN, SLASEL/XVS

DOVDD-1V8
DVDD-1V05
AVDD-2V8

VCC_3V3 17, 16 — PWR — 3V3_TOF
VCSEL_3V3 29, 30, 32, 33 — PWR — 3V3_VCSEL
NC 13, 14 — R98 0 0402 — 3V3_TOF
AGND 31
DGND 2, 4, 11, 12, 15, 18, 21, 24, 27, 28 — GND

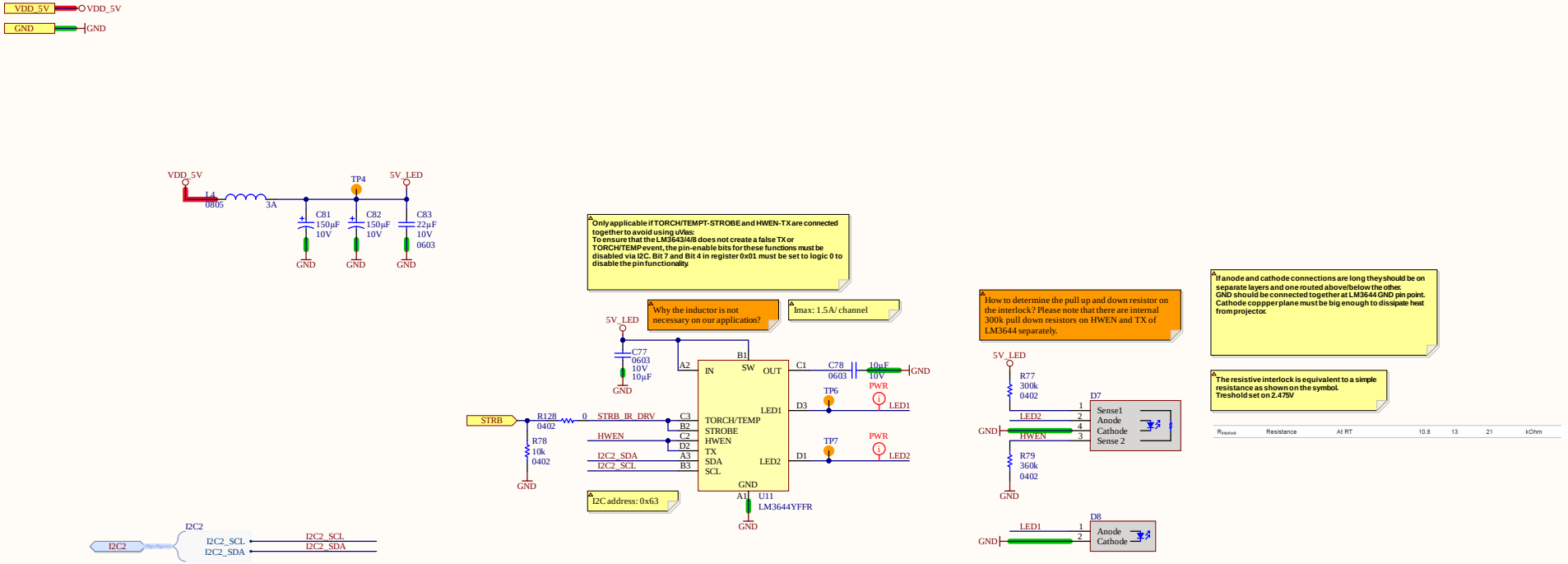
JH-B2027-00

- Voltage rating /pin: 30VDC
- Current rating /pin: 200mA

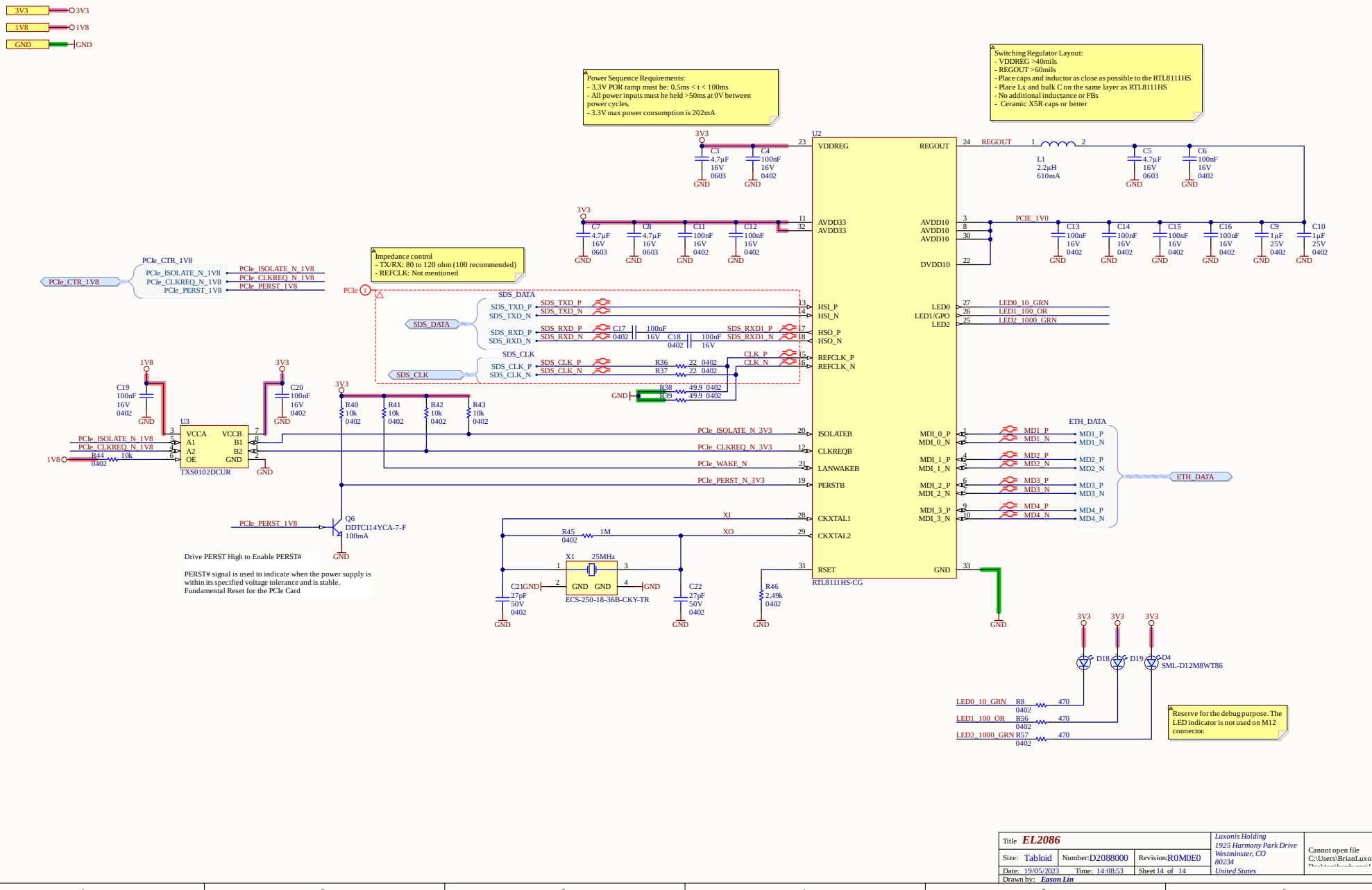
No power sequence requirement for ToF module

The max. current is designed for 200mA per pin to maximize the compability of different sensors.

Title: EL2086			Luxonis Holding 1925 Harmony Park Drive Westminster, CO 80234 United States
Size: Tabloid	Number: D2088000	Revision: R0M0E0	Cannot open file C:\Users\BrianLuxonis\
Date: 19/05/2023 Time: 14:08:53	Sheet 12 of 14		
Drawn by: Eason Lin			



Title	EL2086		Luxonis Holding 1925 Harmony Park Drive Westminster, CO 80234 United States
Size: Tabloid	Number: D2088000	Revision: R0M0E0	Cannot open file C:\Users\BrianLuxonis\
Date: 19/05/2023	Time: 14:08:53	Sheet 13 of 14	
Drawn by: Eason Lin			


3V3
1V8
GND
Power Sequence Requirements:
- 3.3V POR ramp must be: 0.5ms < t < 100ms
- All power inputs must be held >50ms at 0V between power cycles.
- 3.3V max power consumption is 202mA
Switching Regulator Layout:
- VDDREG >40mils
- REGOUT >60mils
- Place caps and inductor as close as possible to the RTL8111HS
- Place Lx and bulk C on the same layer as RTL8111HS
- No additional inductance or FBs
- Ceramic X5R caps or better
U2
VDDREG
REGOUT
L1
2.2µH
610mA
AVDD33
AVDD10
DVDD10
PCIE_1V0
Impedance control
- TX/RX: 80 to 120 ohm (100 recommended)
- REFCLK: Not mentioned
PCIe_CTR_1V8
PCIe_ISOLATE_N_1V8
PCIe_CLKREQ_N_1V8
PCIe_PERST_1V8
SDS_DATA
SDS_CLK
SDS_TXD_P
SDS_TXD_N
SDS_RXD_P
SDS_RXD_N
SDS_CLK_P
SDS_CLK_N
HSI_P
HSI_N
HSO_P
HSO_N
REFCLK_P
REFCLK_N
LED0
LED1/GPO
LED2
LED0_10_GRN
LED1_100_OR
LED2_1000_GRN
U3
TXS0102DCUR
VCCA
VCCB
A1
A2
OE
B1
B2
PCIe_ISOLATE_N_3V3
PCIe_CLKREQ_N_3V3
PCIe_WAKE_N
PCIe_PERST_N_3V3
ISOLATEB
CLKREQB
LANWAKEB
PERSTB
Q6
DDTC114YCA-7-F
100mA
Drive PERST High to Enable PERST#
PERST# signal is used to indicate when the power supply is within its specified voltage tolerance and is stable.
Fundamental Reset for the PCIe Card
XI
XO
X1
25MHz
ECS-250-18-36B-CKY-TR
CKXTAL1
CKXTAL2
RSET
RTL8111HS-CG
MDI_0_P
MDI_0_N
MDI_1_P
MDI_1_N
MDI_2_P
MDI_2_N
MDI_3_P
MDI_3_N
ETH_DATA
D18
D19
D4
SML-D12M8WT86
Reserve for the debug purpose. The LED indicator is not used on M12 connector.
Title EL2086
Size: Tabloid
Number:D2088000
Revision:R0M0E0
Date: 19/05/2023
Time: 14:08:53
Sheet 14 of 14
Drawn by: Eason Lin
Luxonis Holding
1925 Harmony Park Drive
Westminster, CO
80234
United States
Cannot open file
C:\Users\BrianLuxonis\