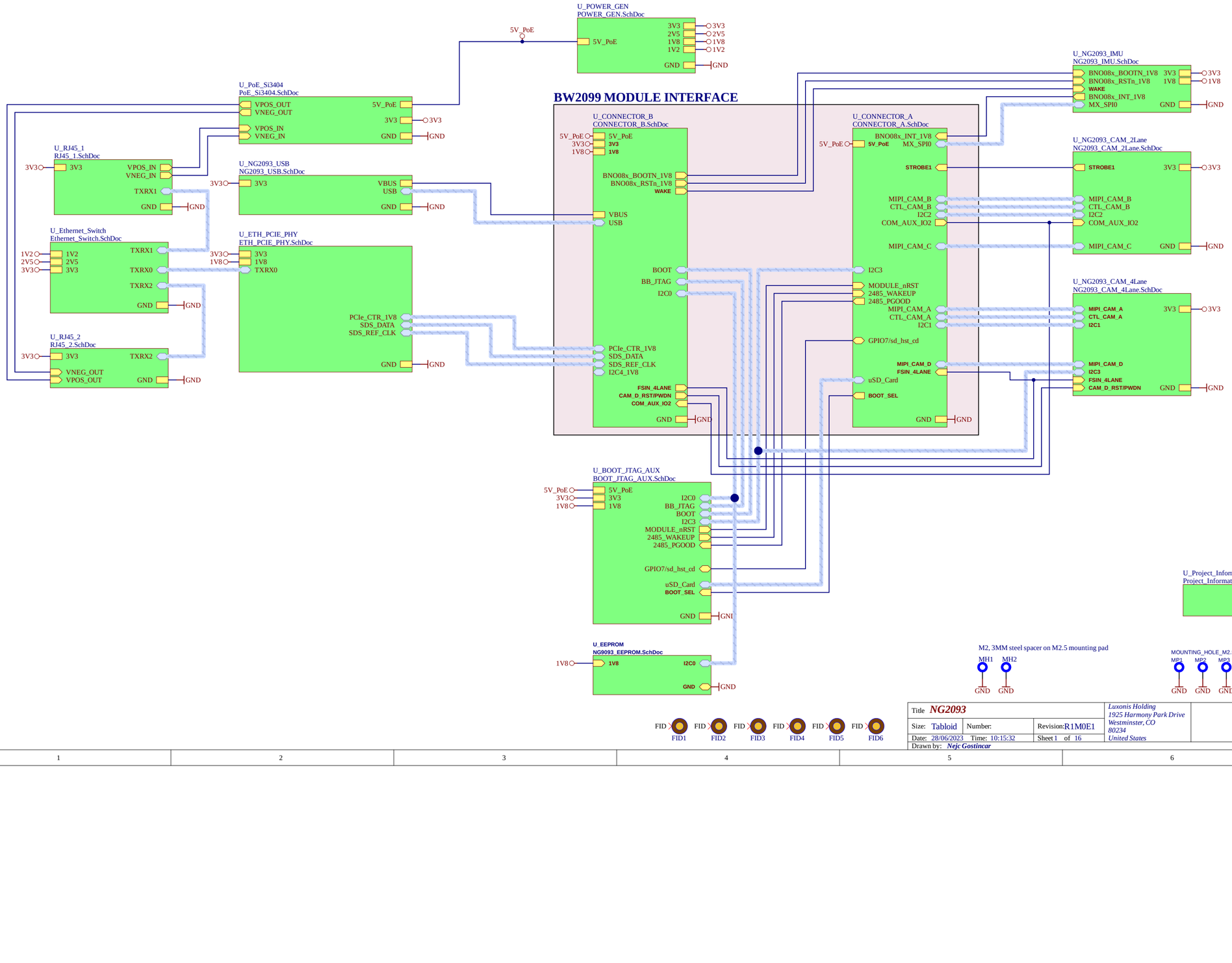


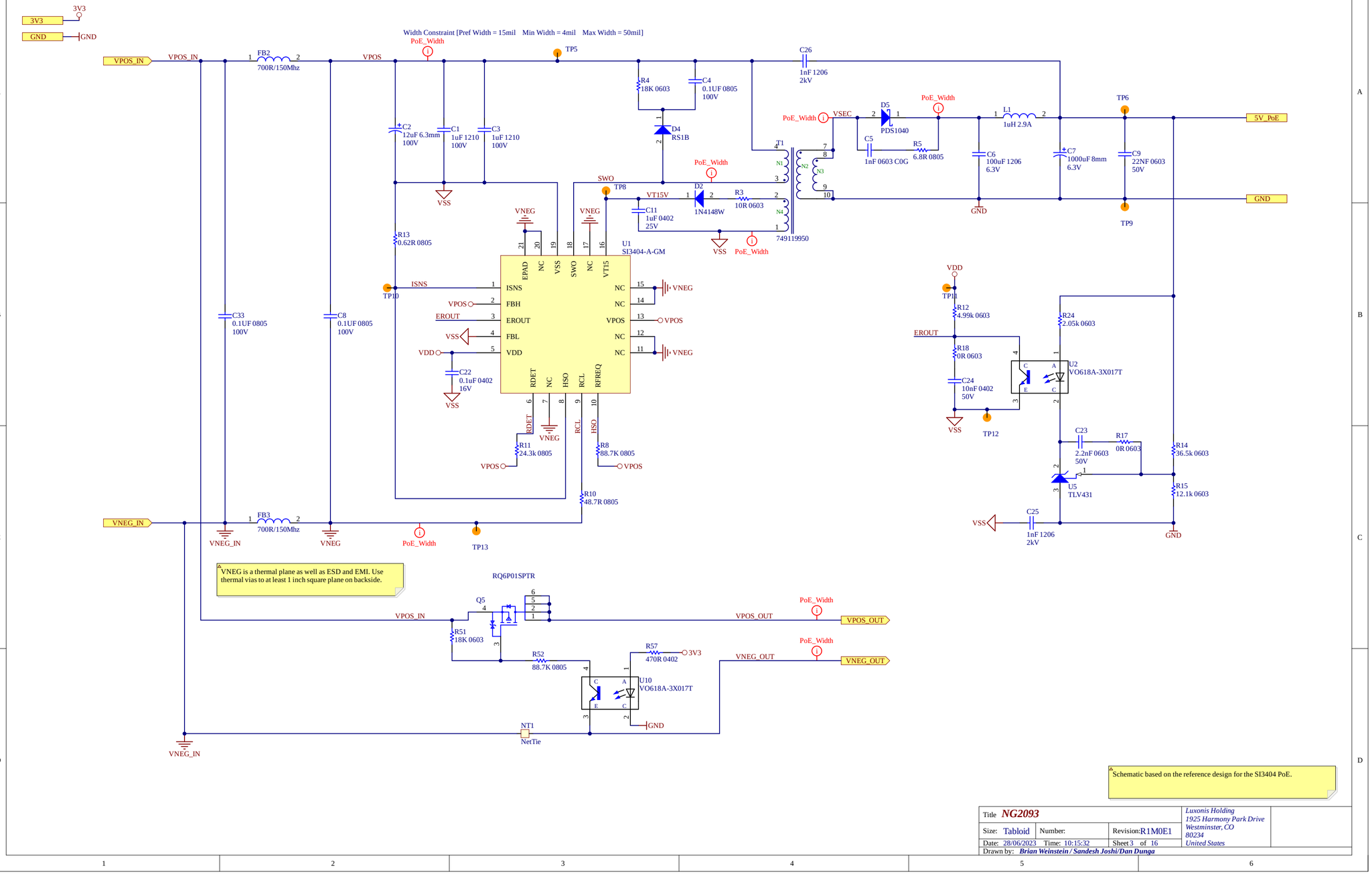

| | | | |
|---|---|---|---|
| Title | NG2093 | | Luxonis Holding<br>1925 Harmony Park Drive<br>Westminster, CO<br>80234<br>United States |
| Size: Tabloid | Number: | Revision: R1M0E1 | |
| Date: 28/06/2023 | Time: 10:15:32 | Sheet 1 of 16 | |
| Drawn by: Nejc Gostincar | | | |

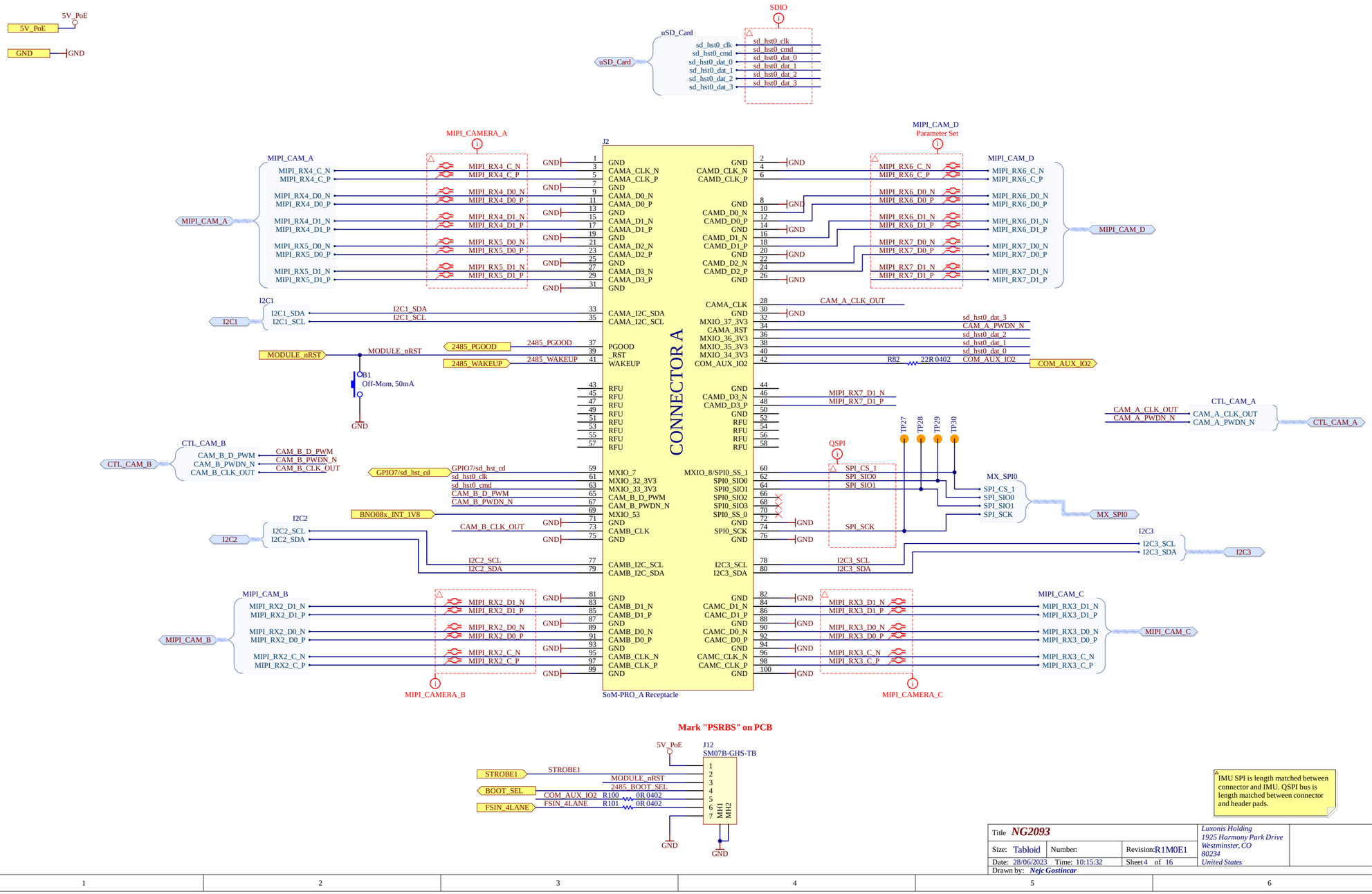
# *Project: NG2093*
# *Current Revision: R1M0E1*

## *NG2093* *Revision History:*

| Date | Revision | Reason for Change | Changes Implemented |
|---|---|---|---|
| 12-May-2021 | Initial Release -> R0M0E0 | | |
| 06-Jan-2022 | DD2088PoE_DChain_R0M0E0 -> NG2093_R0M0E0 | - Support for 4 cameras<br>- Remove PCIe clock generator circuit<br>- Add boot resistors to bridge the boot select switch<br>- Add a USB boot switch<br>- Change the series resitor (R82) for COM_AUX_IO2 from 10k to 22R<br>- Change USB MUX to CBTL02043ABQ,115<br>- Add EEPROM<br>- Change 3,3V power supply from TLV62569 to TPS51313DRCR<br>- Change 1,2V power supply from TLV62569 to TLV62080DSG<br>- Change 2,5V power supply from TLV75525PDRVR to NCP139AFCTC05ADJT2G<br>- Connected WAKE signal from IMU to MXIO10 | - Support for 4 cameras (2x 4-Lane MIPI and 2x 2-Lane MIPI)<br>- Remove PCIe clock generator circuit<br>- Added boot resistors to bridge the boot select switch<br>- Added a USB boot switch<br>- Change the series resitor (R82) for COM_AUX_IO2 from 10k to 22R<br>- Change USB MUX to CBTL02043ABQ,115 and added capacitors to VDD pins<br>- Added EEPROM<br>- Change 3,3V power supply from TLV62569 to TPS51313DRCR<br>- Change 1,2V power supply from TLV62569 to TLV62080DSG<br>- Change 2,5V power supply from TLV75525PDRVR to NCP139AFCTC05ADJT2G<br>- Connected WAKE signal from IMU to MXIO10 |
| 09-Jan-2022 | NG2093_R0M0E0 -> NG2093_R1M0E1 | - Current ethernet switch is not available on the market due to shortage<br>- Mosfet Q5 is not available on market. | - Replace it with AR8327N-AL1A<br>- Replaced Q5 with RQ6P01SPTR |

| | | | |
|---|---|---|---|
| Title *NG2093* | | | *Luxonis Holding*<br>*1925 Harmony Park Drive*<br>*Westminster, CO*<br>*80234*<br>*United States* |
| Size: Tabloid | Number: | Revision: R1M0E1 | |
| Date: 28/06/2023 Time: 10:15:32 | | Sheet 2 of 16 | |
| Drawn by: ***Nejc Gostincar*** | | | |


3V3
GND
Width Constraint [Pref Width = 15mil Min Width = 4mil Max Width = 50mil]
PoE_Width
TP5
VPOS_IN
VPOS
FB2
700R/150Mhz
C26
1nF 1206
2kV
R4
18K 0603
C4
0.1UF 0805
100V
D4
RS1B
C2
12uF 6.3mm
100V
C1
1uF 1210
100V
C3
1uF 1210
100V
VSS
SWO
TP8
VT15V
D2
1N4148W
R3
10R 0603
C11
1uF 0402
25V
T1
749119950
VSEC
D5
PDS1040
L1
1uH 2.9A
C5
1nF 0603 C0G
R5
6.8R 0805
C6
100uF 1206
6.3V
C7
1000uF 8mm
6.3V
C9
22NF 0603
50V
TP6
TP9
5V_PoE
GND
VNEG
R13
0.62R 0805
U1
SI3404-A-GM
EPAD
NC
VSS
SWO
NC
VT15
ISNS
FBH
EROUT
FBL
VDD
RDET
HSO
RCLR
RFREQ
TP10
C33
0.1UF 0805
100V
C8
0.1UF 0805
100V
C22
0.1uF 0402
16V
R11
24.3k 0805
R8
88.7K 0805
R10
48.7R 0805
VPOS
VNEG_IN
FB3
700R/150Mhz
TP13
TP11
R12
4.99k 0603
R18
0R 0603
C24
10nF 0402
50V
TP12
U2
VO618A-3X017T
R24
2.05k 0603
C23
2.2nF 0603
50V
R17
0R 0603
R14
36.5k 0603
U5
TLV431
R15
12.1k 0603
C25
1nF 1206
2kV
VNEG is a thermal plane as well as ESD and EMI. Use thermal vias to at least 1 inch square plane on backside.
RQ6P01SPTR
Q5
R51
18K 0603
R52
88.7K 0805
R57
470R 0402
3V3
U10
VO618A-3X017T
VPOS_OUT
VNEG_OUT
NT1
NetTie
Schematic based on the reference design for the SI3404 PoE.
Title NG2093
Size: Tabloid
Number:
Revision: R1M0E1
Date: 28/06/2023 Time: 10:15:32
Sheet 3 of 16
Drawn by: Brian Weinstein / Sandesh Joshi/Dan Dunga
Luxonis Holding
1925 Harmony Park Drive
Westminster, CO
80234
United States




**Mark "PSRBS" on PCB**




IMU SPI is length matched between connector and IMU. QSPI bus is length matched between connector and header pads.

| | | | |
|---|---|---|---|
| Title: NG2093 | | | Luxonis Holding<br>1925 Harmony Park Drive<br>Westminster, CO<br>80234<br>United States |
| Size: Tabloid | Number: | Revision: R1M0E1 | |
| Date: 28/06/2023 Time: 10:15:32 | | Sheet 4 of 16 | |
| Drawn by: Nejc Gostincar | | | |

5V_PoE
GND
3V3
1V8

PCIe_ISOLATE_N_1V8 can be pulled up or down via the BOOT DIP, assuming the R27 jumper resistor is stuffed. If pulled high, the signal is levelshifted to a final 3.3V level for the RTL8111HS.

The Myriad X (MX) has 1.8V GPIO outputs, but a number of PCIe-related functions require 3.3V signaling. This includes the I2C for the PCIe reference clock, and the control signaling for the PHY bridge (though RTL8111HS can handle 1.8V signalling as well).

J3

CONNECTOR B

| | | | | | |
|---|---|---|---|---|---|
| 5V_PoE | GND | 1 | GND | GND | 2 | GND | 5V_PoE |
| | GND | 3 | GND | GND | 4 | GND | |
| | | 5 | 5V | 5V | 6 | | |
| | | 7 | 5V | 5V | 8 | | |
| | | 9 | 5V | 5V | 10 | | |
| | | 11 | 5V | 5V | 12 | | |
| | GND | 13 | GND | GND | 14 | GND | |
| | GND | 15 | GND | GND | 16 | GND | |
| | | 17 | I2S2_SCK | BOOT4 | 18 | BOOT4 | |
| | | 19 | I2S2_WS | BOOT3 | 20 | BOOT3 | |
| | | 21 | I2S2_IN_SD0 | BOOT2 | 22 | BOOT2 | |
| | | 23 | I2S2_OUT_SD0 | BOOT1 | 24 | BOOT1 | |
| | | 25 | I2S2_IN_SD1 | BOOT0 | 26 | BOOT0 | |
| | | 27 | I2S2_IN_SD2 | BOOT_AUX/PCIe_ISO_N | 28 | GPIO58 | |
| | | 29 | GND | | | | |
| | | 31 | RFU | GND | 30 | GND | |
| | | 33 | RFU | GND | 32 | GND | |
| | | 35 | RFU | | | | |
| | | 37 | RFU | I2C0_SCL | 34 | I2C0_SCL | |
| | | 39 | RFU | I2C0_SDA | 36 | I2C0_SDA | |
| | | 41 | RFU | | | | |
| | | 43 | RFU | GND | 38 | GND | |
| | | 45 | RFU | GND | 40 | GND | |
| | | 47 | RFU | | | | |
| | | 49 | RFU | MXIO_46 | 42 | BNO08x_BOOTN_1V8 | |
| | | 51 | RFU | MXIO_45 | 44 | BNO08x_RSTn_1V8 | |
| | | 53 | RFU | | | | |
| | | 55 | RFU | | | | |
| I2C4_1V8 | I2C4_SDA_1V8 | 57 | I2C4_SDA | GND | 46 | GND | |
| | I2C4_SCL_1V8 | 59 | I2C4_SCL | MXIO_6 | 48 | | |
| | GND | 61 | GND | MXIO_9 | 50 | | |
| | | | | MXIO_10 | 52 | WAKE | |
| | PCIe_PERST_1V8 | 63 | PCIe_PERST | MXIO_11 | 54 | | |
| | PCIe_CLKREQ_N_1V8 | 65 | PCIe_CLKREQ_N | MXIO_12 | 56 | | |
| | | | | MXIO_14 | 58 | | |
| | GND | 67 | GND | MXIO_15 | 60 | | |
| SDS_DATA | SDS_TXD_P | 69 | SDS_TXD_P | MXIO_16 | 62 | | |
| | SDS_TXD_N | 71 | SDS_TXD_N | MXIO_17 | 64 | | |
| | GND | 73 | GND | MXIO_38 | 66 | | |
| | SDS_RXD_P | 75 | SDS_RXD_P | MXIO_39 | 68 | | |
| | SDS_RXD_N | 77 | SDS_RXD_N | MXIO_40 | 70 | R99 22R 0402 FSIN_4LANE | |
| | GND | 79 | GND | MXIO_42 | 72 | CAM_D_RST/PWDN | |
| SDS_REF_CLK | SDS_IO_CLKI_N | 81 | SDS_IO_CLKI_N | MXIO_43 | 74 | | |
| | SDS_REF_CLK_N | SDS_IO_CLKI_N | | RFU | 76 | | |
| | SDS_REF_CLK_P | SDS_IO_CLKI_P | 83 | SDS_IO_CLKI_P | | | |
| | GND | 85 | GND | | 78 | GND | |
| | | | | 5V/VBUS | 80 | VBUS | |
| | GND | 87 | GND | GND | 82 | GND | |
| BB_JTAG | SYS_RST | 89 | SYS_RST | USB_TX_N | 84 | USB_TX_N | |
| | TDO | 91 | TDO | USB_TX_P | 86 | USB_TX_P | |
| | TRST | 93 | TRST | GND | 88 | | |
| | TDI | 95 | TDI | USB_D_N | 90 | GND | |
| | TCK | 97 | TCK | USB_D_P | 92 | USB_D_N | |
| | TMS | 99 | TMS | GND | 94 | USB_D_P | |
| | | | | USB_RX_N | 96 | GND | |
| | | | | USB_RX_P | 98 | USB_RX_N | |
| | | | | GND | 100 | USB_RX_P | |

SoM-PRO_B Receptacle

R27 0R 0603 — PCIe_ISOLATE_N_1V8 — PCIe_CLKREQ_N_1V8 — PCIe_PERST_1V8 — PCIe_CTR_1V8

BOOT

I2C0

R78 10K 0402 — WAKE

U11 NC7SZ66M5X — COM_AUX_IO2 — FSIN_4LANE

C65 0.1uF 0402 10V — 1V8

R99 22R 0402 — FSIN_4LANE — CAM_D_RST/PWDN

SDS_REF_CLK — R6 22R 0402 — R25 22R 0402

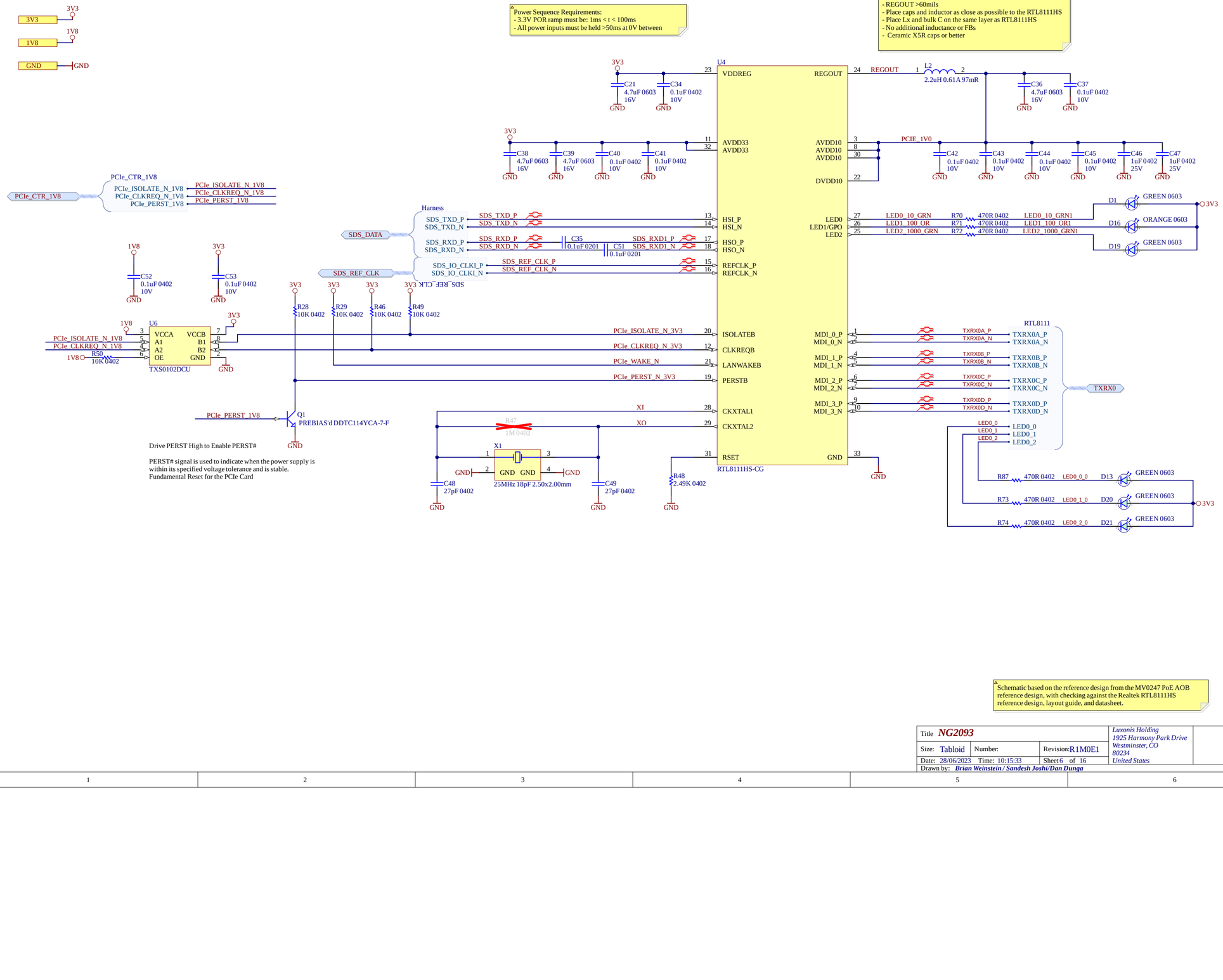
R26 49.9R 0402 — R30 49.9R 0402 — GND

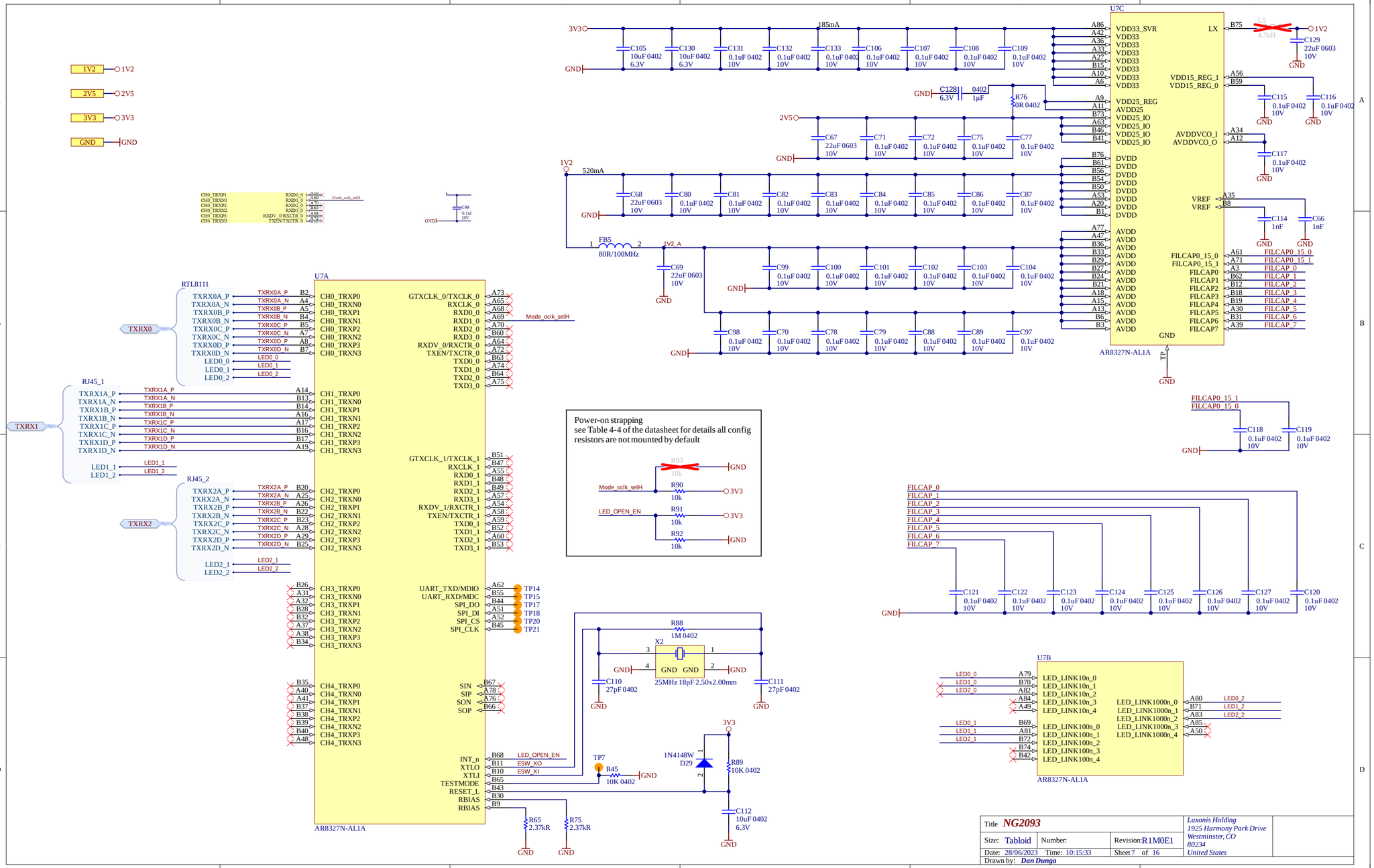
USB

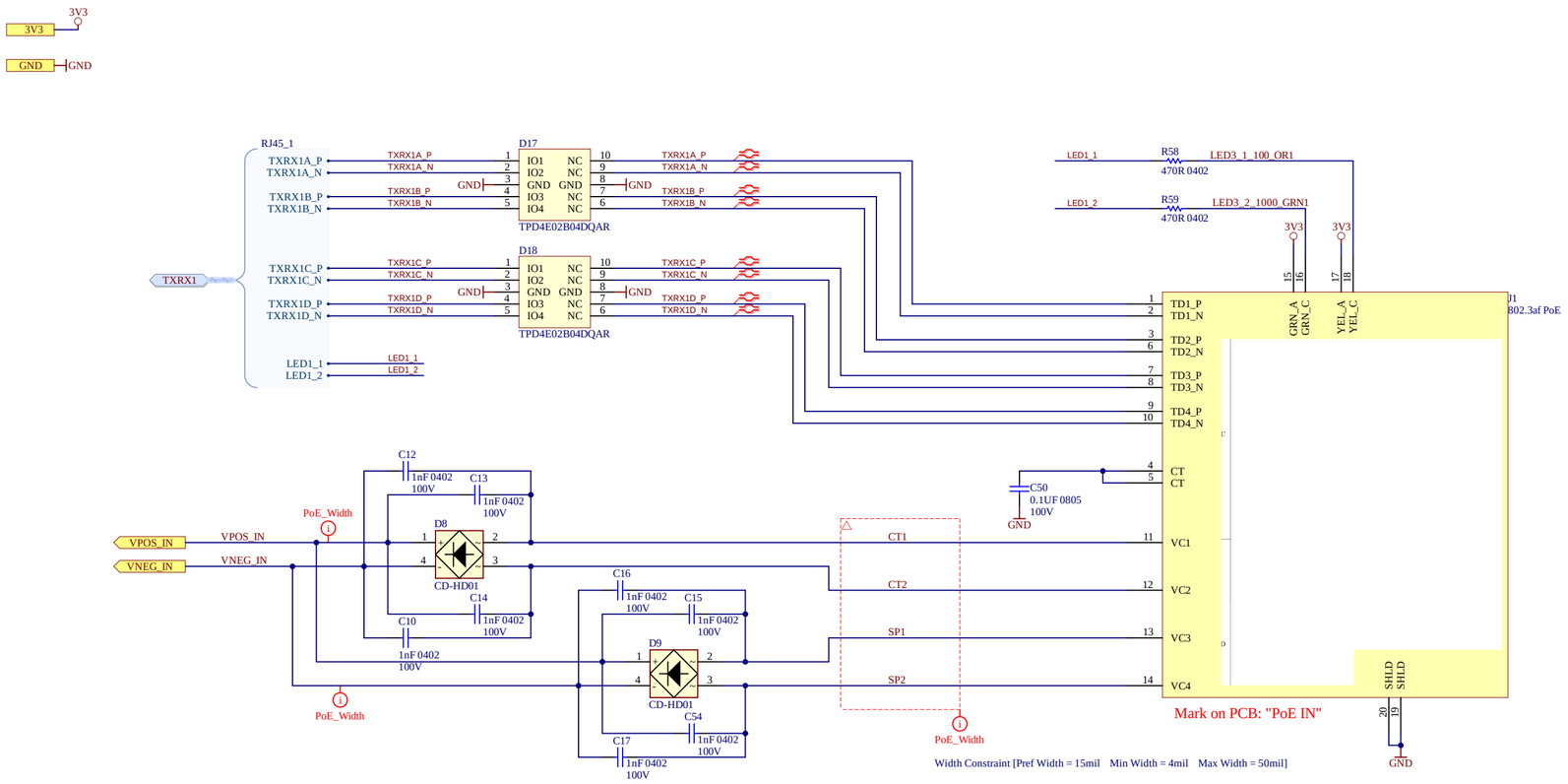
USB

| | |
|---|---|
| Title | NG2093 |
| Size: | Tabloid |
| Number: | |
| Revision: | R1M0E1 |
| Date: | 28/06/2023 |
| Time: | 10:15:32 |
| Sheet | 5 of 16 |
| Drawn by: | Nejc Gostincar |

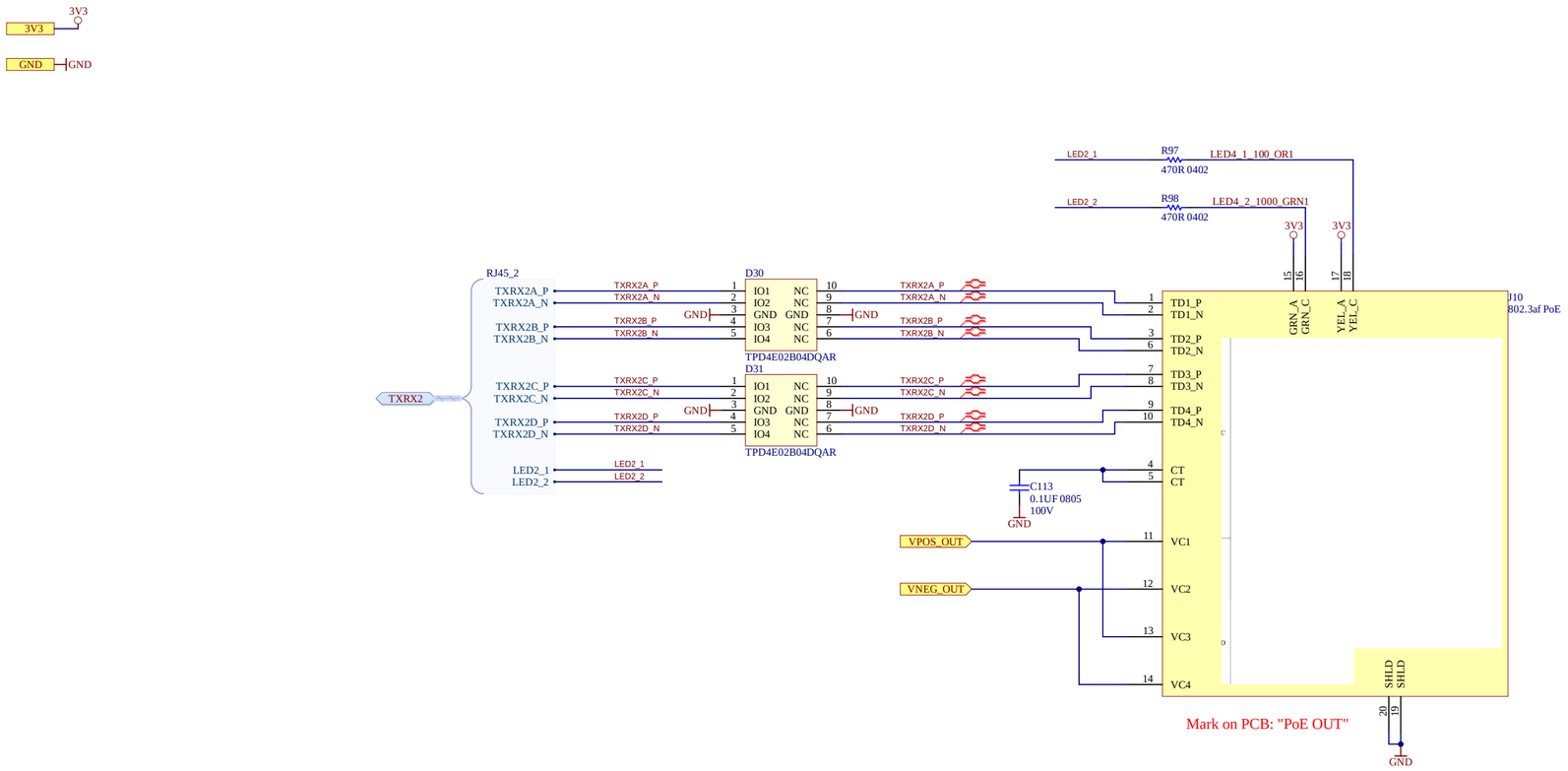
Luxonis Holding
1925 Harmony Park Drive
Westminster, CO
80234
United States


3V3
1V8
GND
Power Sequence Requirements:
- 3.3V POR ramp must be: 1ms < t < 100ms
- All power inputs must be held >50ms at 0V between
Switching Regulator Layout:
- VDDREG >40mils
- REGOUT >60mils
- Place caps and inductor as close as possible to the RTL8111HS
- Place Lx and bulk C on the same layer as RTL8111HS
- No additional inductance or FBs
- Ceramic X5R caps or better
U4
VDDREG
REGOUT
L2
2.2uH 0.61A 97mR
C21 4.7uF 0603 16V
C34 0.1uF 0402 10V
C36 4.7uF 0603 16V
C37 0.1uF 0402 10V
AVDD33
AVDD10
DVDD10
PCIE_1V0
C38 4.7uF 0603 16V
C39 4.7uF 0603 16V
C40 0.1uF 0402 10V
C41 0.1uF 0402 10V
C42 0.1uF 0402 10V
C43 0.1uF 0402 10V
C44 0.1uF 0402 10V
C45 0.1uF 0402 10V
C46 1uF 0402 25V
C47 1uF 0402 25V
PCIe_CTR_1V8
PCIe_ISOLATE_N_1V8
PCIe_CLKREQ_N_1V8
PCIe_PERST_1V8
Harness
SDS_TXD_P
SDS_TXD_N
SDS_RXD_P
SDS_RXD_N
SDS_DATA
C35 0.1uF 0201
C51 0.1uF 0201
SDS_RXD1_P
SDS_RXD1_N
HSI_P
HSI_N
HSO_P
HSO_N
SDS_IO_CLKI_P
SDS_IO_CLKI_N
SDS_REF_CLK_P
SDS_REF_CLK_N
SDS_REF_CLK
REFCLK_P
REFCLK_N
LED0
LED1/GPO
LED2
LED0_10_GRN
LED1_100_OR
LED2_1000_GRN
R70 470R 0402
R71 470R 0402
R72 470R 0402
LED0_10_GRN1
LED1_100_OR1
LED2_1000_GRN1
D1 GREEN 0603
D16 ORANGE 0603
D19 GREEN 0603
C52 0.1uF 0402 10V
C53 0.1uF 0402 10V
R28 10K 0402
R29 10K 0402
R46 10K 0402
R49 10K 0402
U6
VCCA
VCCB
A1
B1
A2
B2
OE
GND
TXS0102DCU
R50 10K 0402
PCIe_ISOLATE_N_3V3
PCIe_CLKREQ_N_3V3
PCIe_WAKE_N
PCIe_PERST_N_3V3
ISOLATEB
CLKREQB
LANWAKEB
PERSTB
RTL8111
MDI_0_P
MDI_0_N
MDI_1_P
MDI_1_N
MDI_2_P
MDI_2_N
MDI_3_P
MDI_3_N
TXRX0A_P
TXRX0A_N
TXRX0B_P
TXRX0B_N
TXRX0C_P
TXRX0C_N
TXRX0D_P
TXRX0D_N
TXRX0
Q1
PREBIAS'd DDTC114YCA-7-F
PCIe_PERST_1V8
Drive PERST High to Enable PERST#
PERST# signal is used to indicate when the power supply is within its specified voltage tolerance and is stable.
Fundamental Reset for the PCIe Card
X1
XO
CKXTAL1
CKXTAL2
R47 1M 0402
X1 25MHz 18pF 2.50x2.00mm
C48 27pF 0402
C49 27pF 0402
RSET
R48 2.49K 0402
RTL8111HS-CG
LED0_0
LED0_1
LED0_2
R87 470R 0402
R73 470R 0402
R74 470R 0402
D13 GREEN 0603
D20 GREEN 0603
D21 GREEN 0603
Schematic based on the reference design from the MV0247 PoE AOB reference design, with checking against the Realtek RTL8111HS reference design, layout guide, and datasheet.
Title NG2093
Size: Tabloid
Number:
Revision: R1M0E1
Date: 28/06/2023
Time: 10:15:33
Sheet 6 of 16
Drawn by: Brian Weinstein / Sandesh Joshi/Dan Dunga
Luxonis Holding
1925 Harmony Park Drive
Westminster, CO
80234
United States

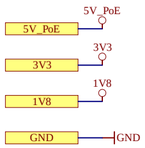

1V2
2V5
3V3
GND
U7C
AR8327N-AL1A
U7A
AR8327N-AL1A
RTL8111
RJ45_1
RJ45_2
TXRX0
TXRX1
TXRX2
185mA
520mA
FB5
80R/100MHz
Power-on strapping
see Table 4-4 of the datasheet for details all config resistors are not mounted by default
Mode_oclk_selH
LED_OPEN_EN
U7B
AR8327N-AL1A
Title NG2093
Size: Tabloid
Number:
Revision:R1M0E1
Date: 28/06/2023
Time: 10:15:33
Sheet 7 of 16
Drawn by: Dan Dunga
Luxonis Holding
1925 Harmony Park Drive
Westminster, CO
80234
United States



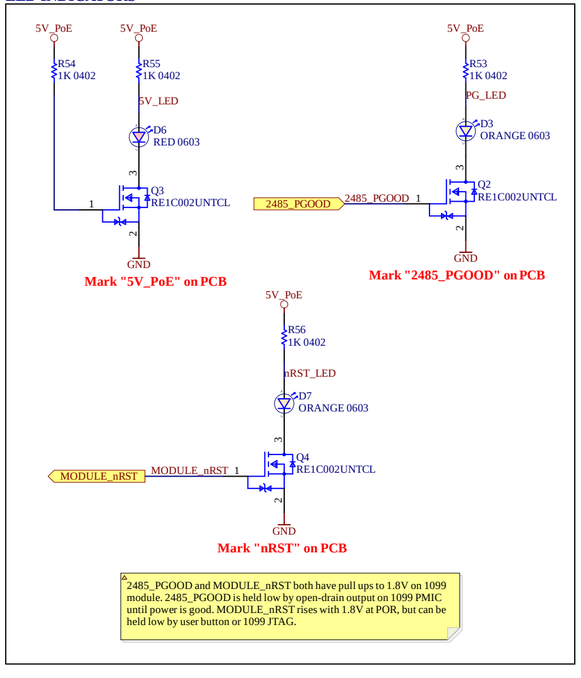

| | | | |
|---|---|---|---|
| Title | NG2093 | | Luxonis Holding<br>1925 Harmony Park Drive<br>Westminster, CO<br>80234<br>United States |
| Size: Tabloid | Number: | Revision: R1M0E1 | |
| Date: 28/06/2023 | Time: 10:15:33 | Sheet 8 of 16 | |
| Drawn by: Nejc Gostincar | | | |



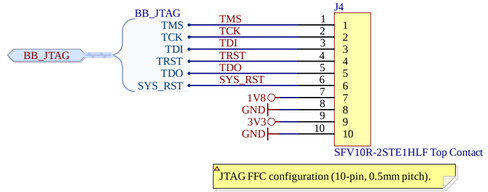

| | | |
|---|---|---|
| Title **NG2093** | | *Luxonis Holding*<br>*1925 Harmony Park Drive*<br>*Westminster, CO*<br>*80234*<br>*United States* |
| Size: Tabloid | Number: | Revision: R1M0E1 |
| Date: 28/06/2023 Time: 10:15:33 | Sheet 9 of 16 | |
| Drawn by: ***Dan Dunga*** | | |



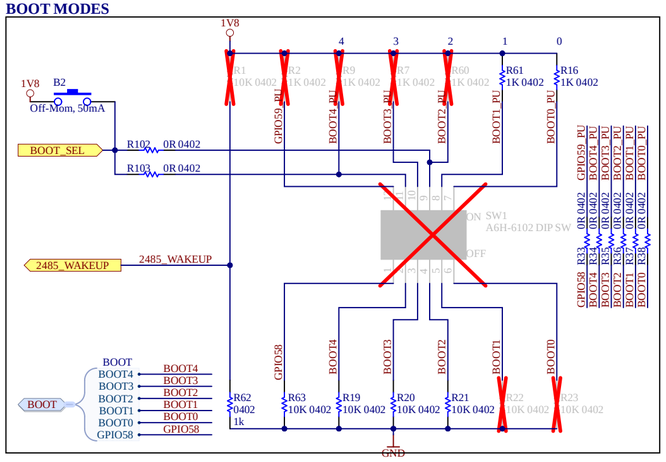
## LED INDICATORS



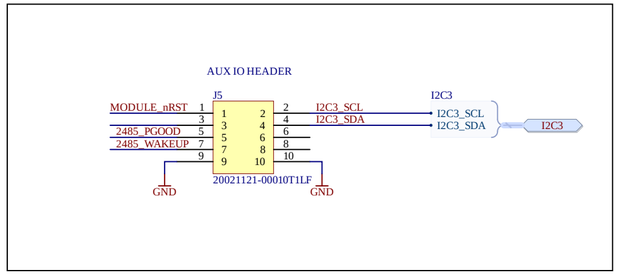

## JTAG



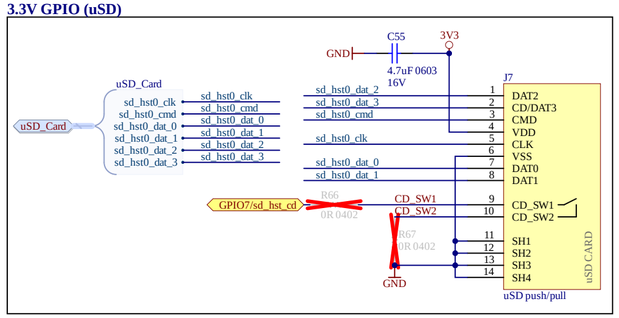

## BOOT MODES



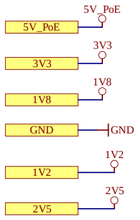

## AUX IO HEADER



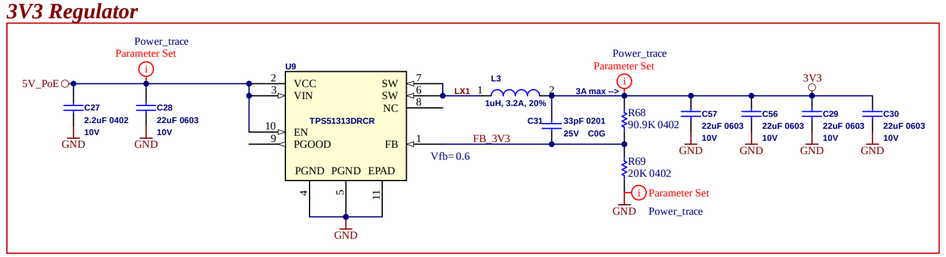

## 3.3V GPIO (uSD)



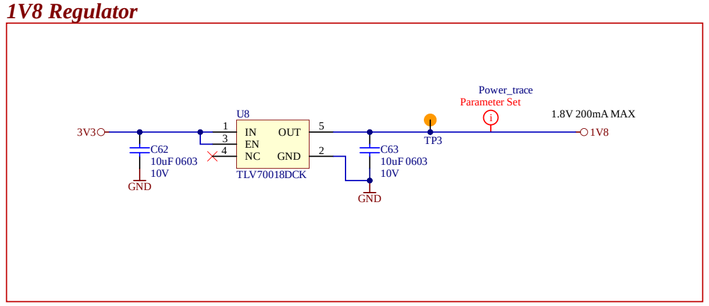

| | | | |
|---|---|---|---|
| Title | NG2093 | | Luxonis Holding<br>1925 Harmony Park Drive<br>Westminster, CO<br>80234<br>United States |
| Size: Tabloid | Number: | Revision: R1M0E1 | |
| Date: 28/06/2023 | Time: 10:15:33 | Sheet 10 of 16 | |
| Drawn by: Nejc Gostincar | | | |



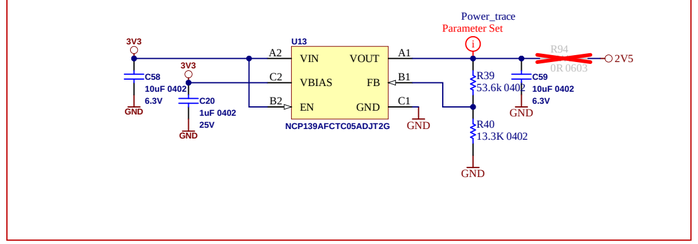

## 3V3 Regulator



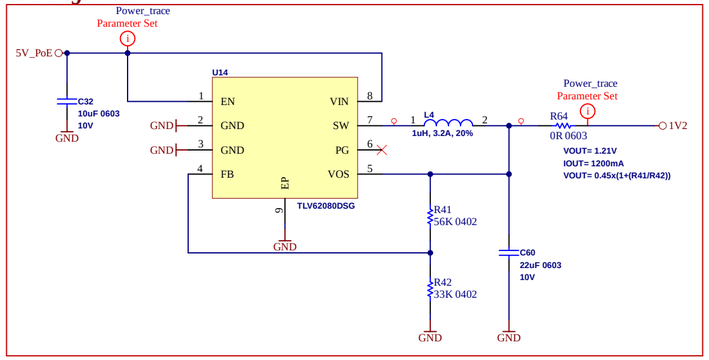

## 1V8 Regulator




## 2V5 Regulator

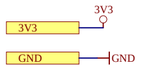


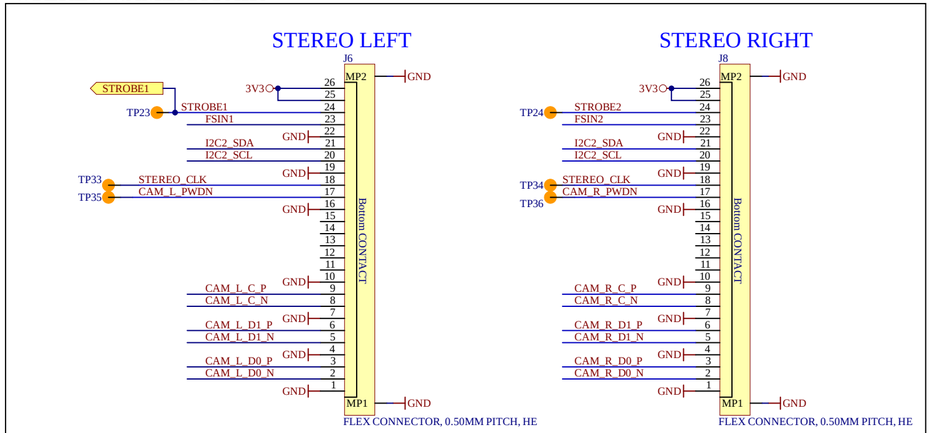

## 1V2 Regulator

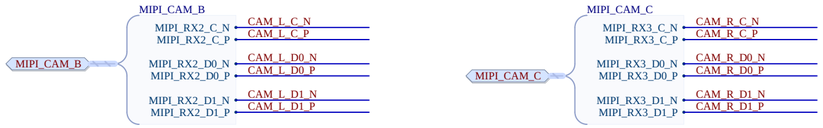



| | | | |
|---|---|---|---|
| Title | NG2093 | | Luxonis Holding<br>1925 Harmony Park Drive<br>Westminster, CO<br>80234<br>United States |
| Size: Tabloid | Number: | Revision: R1M0E1 | |
| Date: 28/06/2023 | Time: 10:15:33 | Sheet 11 of 16 | |
| Drawn by: Brian Weinstein / Sandesh Joshi/Dan Dunga | | | |

# STEREO CAMERA PAIR

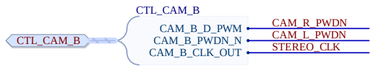


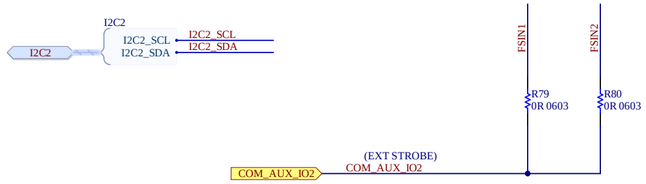





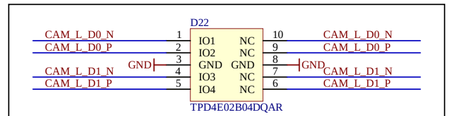


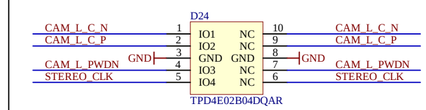


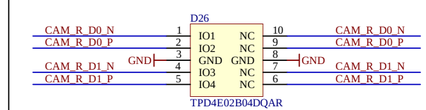



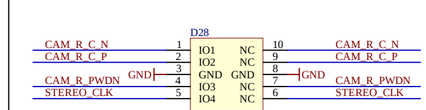

"CAM1" (Left) is reset via CAM_PWDN, and "CAM2" (Right), is reset via CAM_PWM.

## ESD PROTECTION



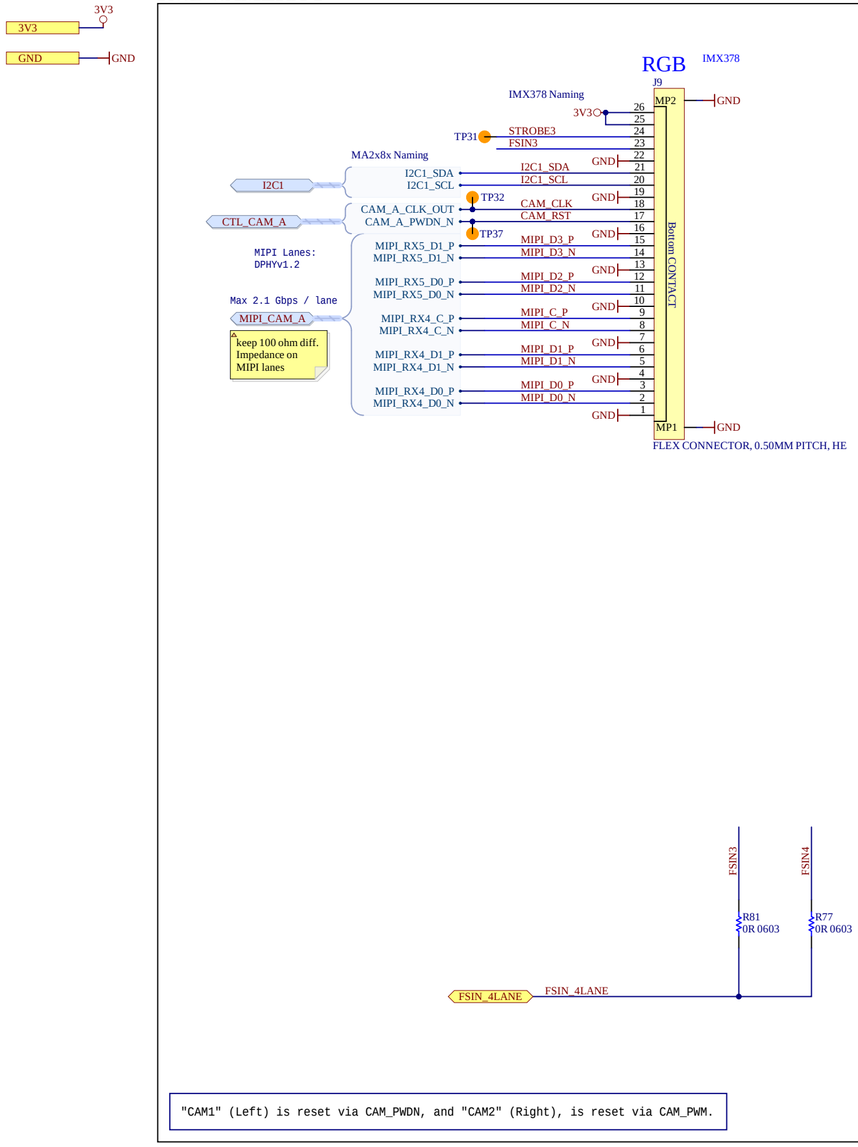



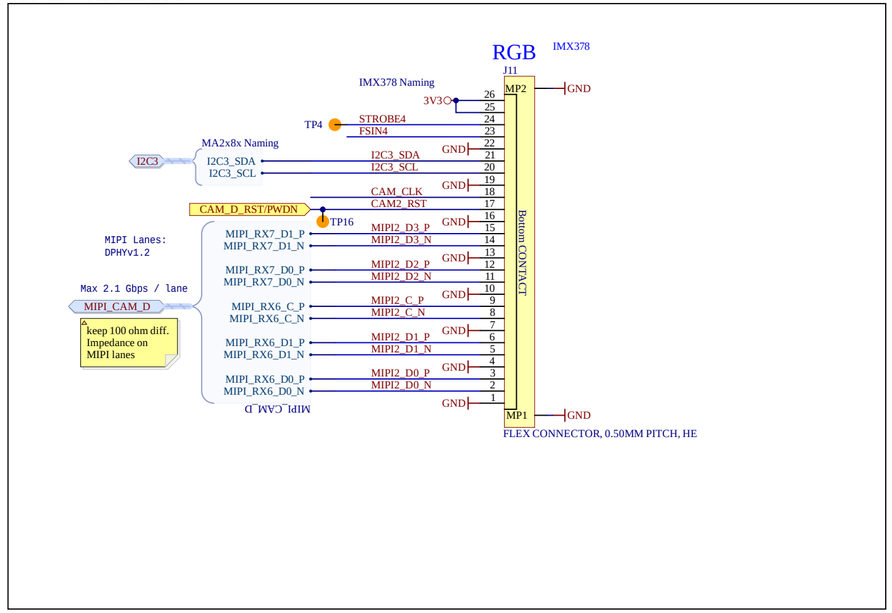




| | | | |
|---|---|---|---|
| Title **NG2093** | | | *Luxonis Holding*<br>*1925 Harmony Park Drive*<br>*Westminster, CO*<br>*80234*<br>*United States* |
| Size: Tabloid | Number: | Revision: R1M0E1 | |
| Date: 28/06/2023 Time: 10:15:33 | | Sheet 12 of 16 | |
| Drawn by: ***Nejc Gostincar*** | | | |

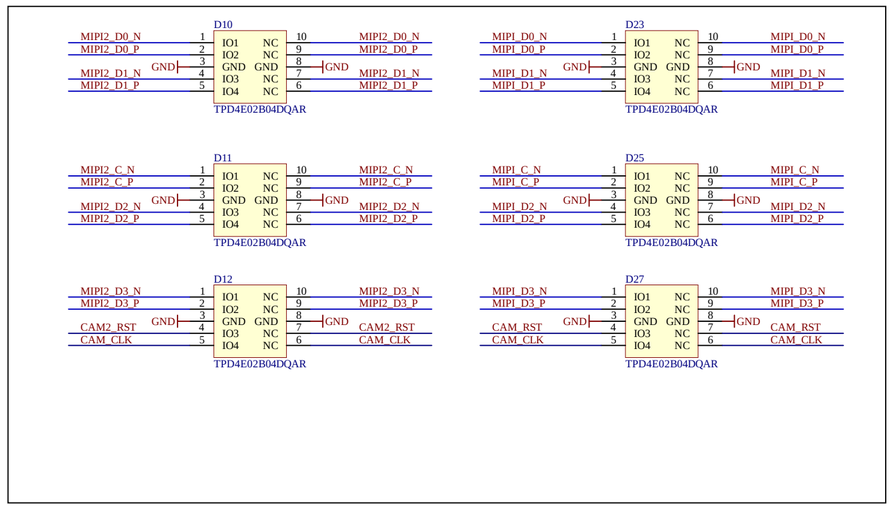
## RGB CAMERA 1



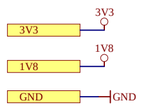

## RGB CAMERA 2




## ESD PROTECTION

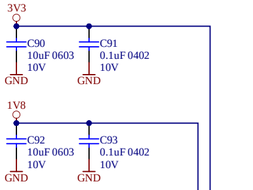



| | | | |
|---|---|---|---|
| Title **NG2093** | | | *Luxonis Holding*<br>*1925 Harmony Park Drive*<br>*Westminster, CO*<br>*80234*<br>*United States* |
| Size: Tabloid | Number: | Revision: R1M0E1 | |
| Date: 28/06/2023 | Time: 10:15:33 | Sheet 13 of 16 | |
| Drawn by: ***Nejc Gostincar*** | | | |




* For the switching sequence of power supply VDD and VDDIO it is mandatory that VDD is powered on and driven to the specified level before or at the same time as VDDIO is powered ON. Otherwise there are no limitations on the voltage levels of both pins relative to each other as long as they are used within the specified operating range.

VDD can be powered from 2.4V - 3.6V
VDDIO can be powered from 1.7V - 3.6V

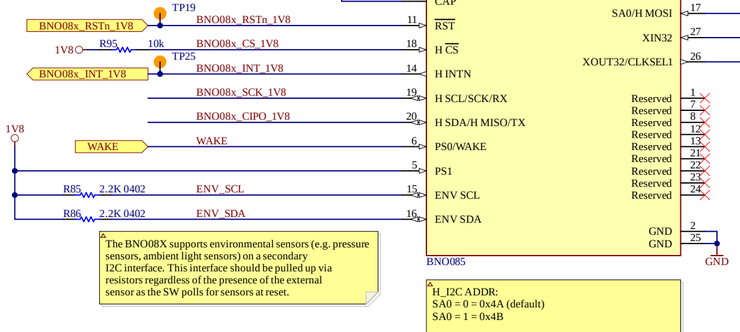


NRST is the reset line for the BNO08X and can be either driven by the application processor or the board reset.

The H_INTN pin is the application interrupt line that indicates the BNO08X requires attention. This should be tied to a GPIO with wake capability. The interrupt is active low. On the BNO085, if the host fails to respond to the assertion of H_INTN within approximately 10 ms, the BNO085 will timeout, deassert H_INTN and retry the operation.

Pin 5 (PS1) and Pin 6 (PS0/WAKE) are the host interface protocol selection pins. For SPI selection, both pins must be high (from before reset until after the first assertion of H_INTN to select the SPI interface. Pin 5 may be tied to VDDIO. Pin 6 must be connected to a GPIO so that the WAKE functionality can be performed.

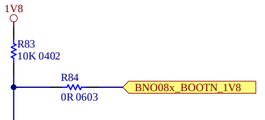
After reset the PS0/WAKE signal is used as a 'wake' signal taking the BNO08X out of sleep if the host wants to initiate communication with the BNO08X.




The BNO08X supports environmental sensors (e.g. pressure sensors, ambient light sensors) on a secondary I2C interface. This interface should be pulled up via resistors regardless of the presence of the external sensor as the SW polls for sensors at reset.

* BNO08x_BOOTN_1V8 is sampled at reset. If low, the BNO08x will enter bootloader mode.
* BNO08x_BOOTN_1V8 should be pulled high through a 10kR. To use the device firmware update (DFU) capability, it's recommended to connect Pin 4 to a GPIO pin on the external uC.

CLKSEL0 = 0 selects external XTAL. Pin has internal pull down, but is connected to GND explicitly.

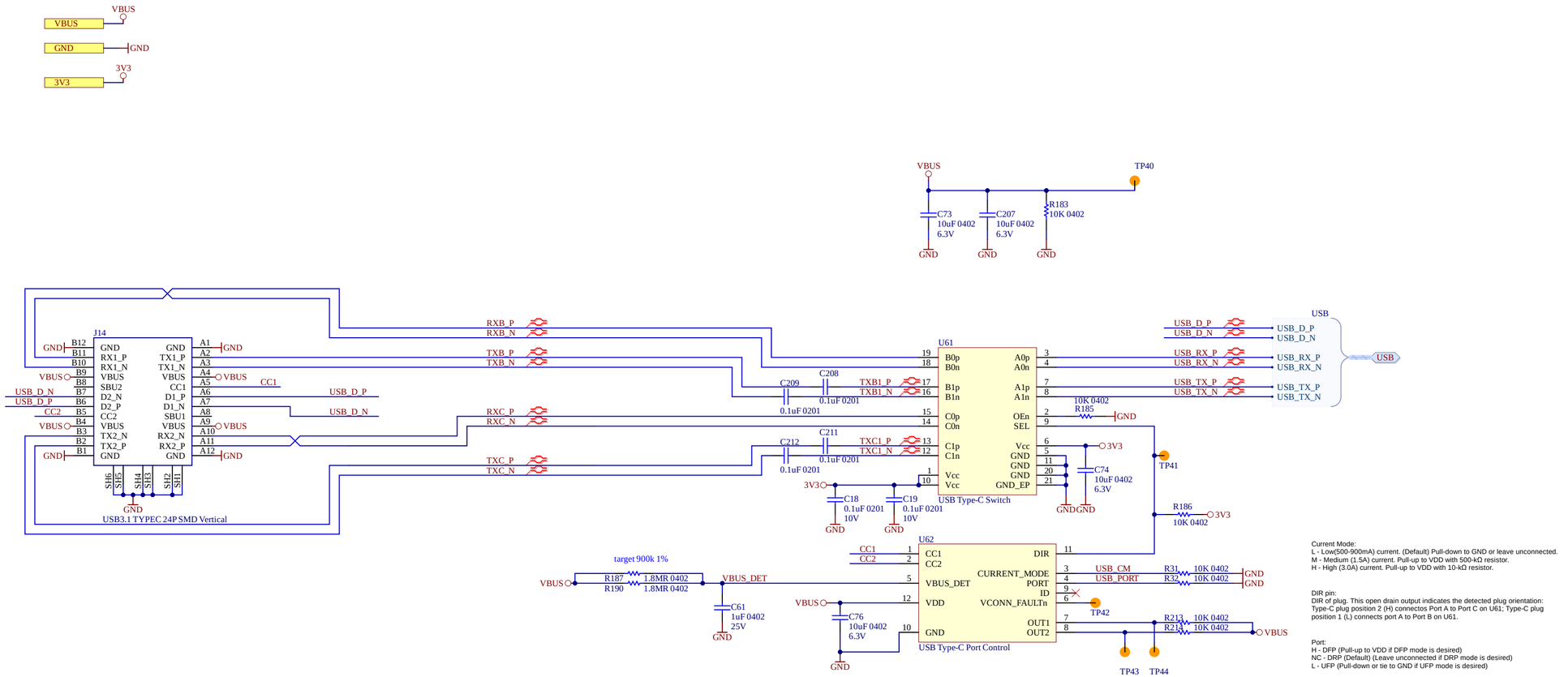



The BNO08X can operate from an internal oscillator, an external 32.768 kHz clock or an external 32.768 kHz crystal. If an external clock is used it must be connected to pin 27. Hillcrest recommends a tolerance of 50ppm. If a crystal is used it must be connected across pins 26 and 27. Hillcrest recommends using a crystal with tolerance 50ppm with 12.5pF capacitor loading.

H_I2C ADDR:
SA0 = 0 = 0x4A (default)
SA0 = 1 = 0x4B

BOOT MODE I2C:
SA0 = 0 = 0x28 (default)
SA0 = 1 = 0x49

| | | | |
|---|---|---|---|
| Title NG2093 | | | Luxonis Holding<br>1925 Harmony Park Drive<br>Westminster, CO<br>80234<br>United States |
| Size: Tabloid | Number: | Revision: R1M0E1 | |
| Date: 28/06/2023 Time: 10:15:33 | | Sheet 14 of 16 | |
| Drawn by: Nejc Gostincar | | | |

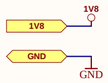


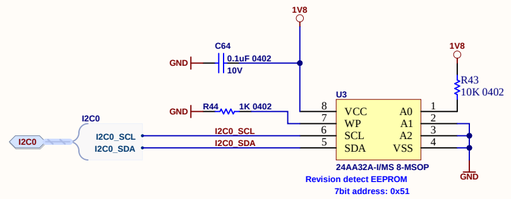

Current Mode:
L - Low(500-900mA) current. (Default) Pull-down to GND or leave unconnected.
M - Medium (1.5A) current. Pull-up to VDD with 500-kΩ resistor.
H - High (3.0A) current. Pull-up to VDD with 10-kΩ resistor.

DIR pin:
DIR of plug. This open drain output indicates the detected plug orientation: Type-C plug position 2 (H) connectos Port A to Port C on U61; Type-C plug position 1 (L) connects port A to Port B on U61.

Port:
H - DFP (Pull-up to VDD if DFP mode is desired)
NC - DRP (Default) (Leave unconnected if DRP mode is desired)
L - UFP (Pull-down or tie to GND if UFP mode is desired)

| | | | |
|---|---|---|---|
| Title **NG2093** | | | *Luxonis Holding*<br>*1925 Harmony Park Drive*<br>*Westminster, CO*<br>*80234*<br>*United States* |
| Size: Tabloid | Number: | Revision: R1M0E1 | |
| Date: 28/06/2023 Time: 10:15:33 | | Sheet 15 of 16 | |
| Drawn by: ***Nejc Gostincar*** | | | |




| | | | |
|---|---|---|---|
| Title **NG2093** | | | *Luxonis Holding*<br>*1925 Harmony Park Drive*<br>*Westminster, CO*<br>*80234*<br>*United States* |
| Size: Tabloid | Number: 16 | Revision: | |
| Date: 28/06/2023 | Time: 10:15:34 | Sheet 16 of 16 | |
| Drawn by: ***Nejc Gostincar*** | | | |

Cannot open file C:\Users\BrianLuxonis\