**OAK-SoM-MAX – RVC3 with eMMC Flash**

# Features

* RVC3 VPU
* Quad-core Arm\* A53 CPU with Linux\*

on chip

* 16/32GB eMMC 5.1
* 32Kb I2C EEPROM
* USB3.1, gen2 10gbps
* PCIe x2 (ext. ref clk)
* 1x 4-Lane MIPI DSI-2 D-PHY
* 2x 2-Lane MIPI DSI-2 D-PHY
* Multiple MIPI CSI-2 D-PHY variants:
  1. 6x 2-Lane MIPI
  2. 1x 4-Lane + 4x 2-Lane MIPI
  3. 2x 4-Lane + 2x 2-Lane MIPI
* QSPI, SDIO, UART, I2C, I2S, RGMII
* Boot Modes Supported: eMMC, USB
* On-board power generation

# Applications

* Industrial automation
* Robotics and autonomy
* Security systems
* Remote intelligence
* Autonomous checkout
* Native RobotHUB support

# Variants

OAK-SoM-MAX options are listed below based on VPU used on the SoM:

* RVC3 with external DRAM:
* 16Gbit
* 32Gbit (default)

# Description

The Luxonis OAK-SoM-MAX is a system-on-module (SoM) designed for integration into a top-level system with a need for a low-power, 4 TOPS AI vision system. The OAK-SoM-MAX interfaces with the system through two 10-gbps-rated 100-pin DF40C-100DP-0.4V(51) board-to-board mezzanine connectors which carry all signal I/O as well as 5V input. The on-board SMPS system regulates the 5V input and provides all necessary digital and analog power. An auxiliary power port is offered to interface without connection to a baseboard.

Core digital electronics on the OAK-SoM-MAX include the RVC3 VPU along with 2x 16Gbit DDR, a 32GB eMMC 5.1 flash device and a 32kb EEPROM. USB 3.1 Gen2, QSPI, UART, I2C, 2-lane PCIe, RGMII and SDIO are all broken out from the SoM and routed through the mezzanine connectors to the system.

Additionally, the OAK-SoM-MAX exposes six 2-lane MIPI CSI-2 D-PHY channels, several variants are available upon request, default being six 2-lane MIPI, allowing for multiple camera inputs.

On top, one 4-lane MIPI DSI-2 D-PHY and 2x 2-lane MIPI DSI-2 D-PHY channels are exposed, allowing multiple DSI peripherals.

I2S interface with APB data 32 bit bus width is exposed; one output and 3 stereo inputs give the ability to connect multiple microphones and one external audio device.

GPIO Boot selection, JTAG, and additional RVC3 GPIOs are exposed as well. A 10-pin JTAG connector is also provided on-board to allow for debug without the need for a baseboard, note that connector will be omitted in later production runs.

The SoM can be booted via USB and eMMC.

SoM power consumption is use-case dependent, but typical consumption is under 7.5W with thermal mitigation.

**Device Information**

|  |  |
| --- | --- |
| **PART NUMBER** | **SIZE (W x L x H)1** |
| OAK-SoM-MAX | 40mm x 40mm x 28.3mm |

1. Including components and heatsink

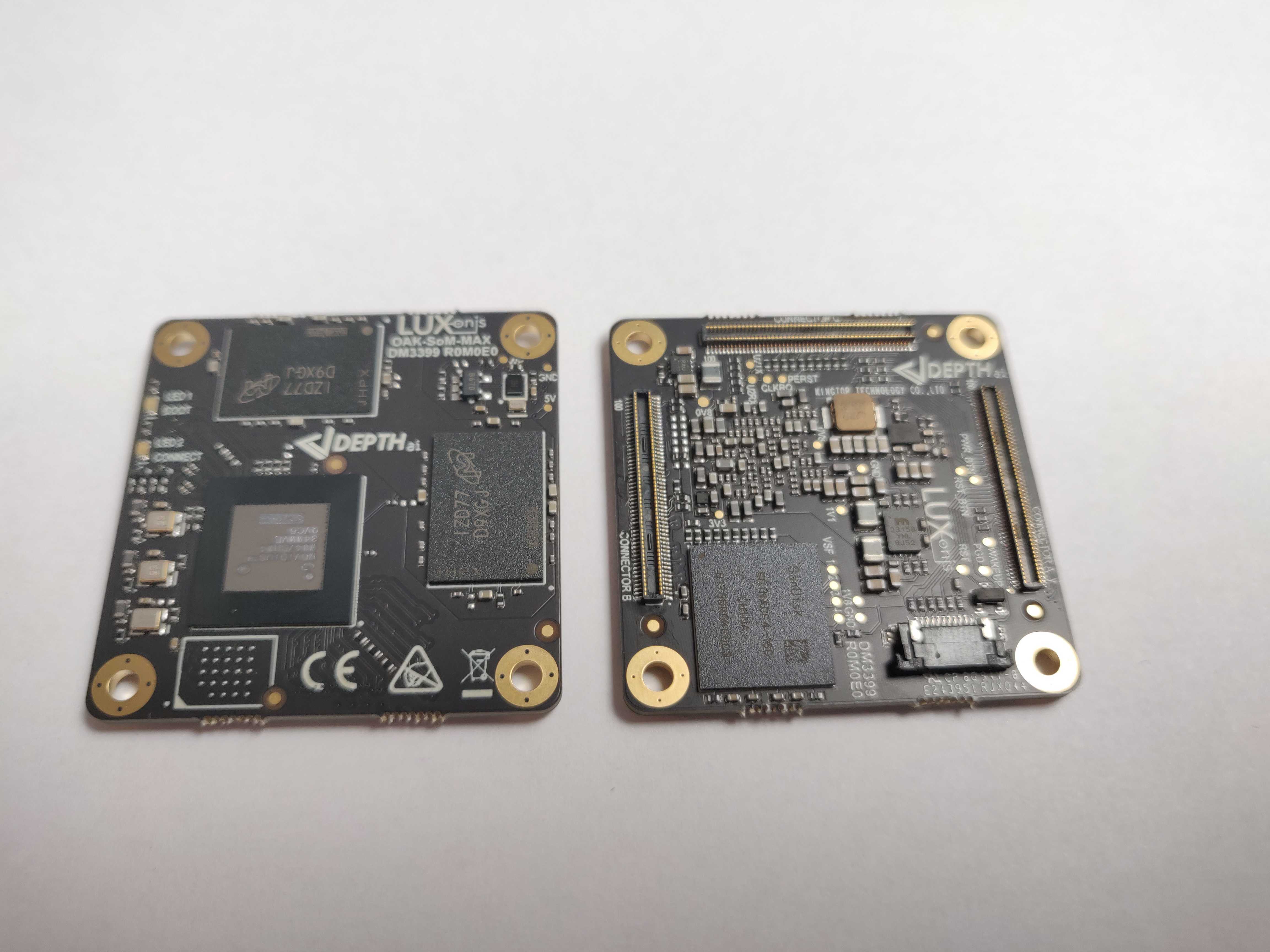


Figure - Top and Bottom of OAK-SoM-MAX PCBA

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# Block Diagram

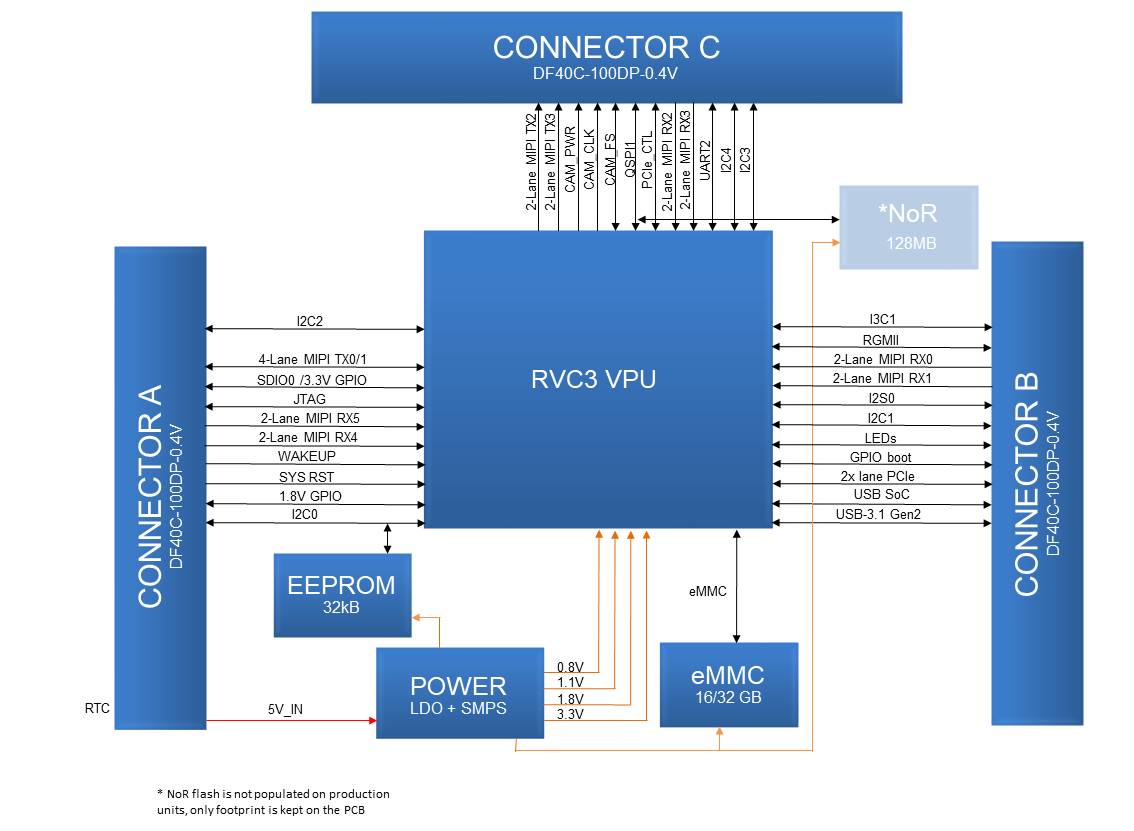


Figure 2 - Schematic Block Diagram

# 5 Electrical Characteristics

## 5.1 Absolute Maximum Ratings1

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| **SYMBOL** | **RATINGS** | **MIN** | **MAX** | **UNIT** |
| **V**IN | External input supply voltage range.2 | 3.6 | 5.5 | V |
| **V**I/O\_1V8 | Input voltage SoM I/O for 1.8V logic | -0.3 | 2.0 | V |
| **V**I/O\_3V3 | Input voltage SoM I/O for 3.3V logic | -0.3 | 3.6 | V |
| **I**I/O | IO output current drive strength | 2 | 12 | mA |
| **T**J | Junction temperature. |  | 105 | C |
| **T**STG | Storage temperature. | -30 | 150 | C |

## 5.2 Recommended Operating Conditions

|  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- |
| **SYMBOL** | **RATINGS** | **MIN** | **TYP** | **MAX** | **UNIT** |
| **V**IN | External input supply voltage range.2 | 4.5 | 5.0 | 5.25 | V |
| **V**I/O\_1V8 | Input voltage SoM I/O for 1.8V logic | 0 |  | 1.8 | V |
| **V**I/O\_3V3 | Input voltage SoM I/O for 3.3V logic | 0 |  | 3.3 | V |
| **P**Q | Quiescent power draw3 |  | TBD |  | W |
| **P**IDLE | Idle power draw4 |  | TBD |  | W |
| **P**INFR | Inference power draw5 |  | 5.5 |  | W |
| **T**A | Ambient operating temperature6 |  | 25 | 50 | °C |
| **T**J | Junction temperature.6 |  |  | 105 | °C |

1. Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended* *Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
2. Applies to 5V input pins only
3. With SoM in reset
4. RVC3 booted to base mode via USB
5. MobilenetSSDV2 detector, 30fps
6. With default Luxonis passive heatsink, running Mobilenet-SSDV2 30fps. Custom or active thermal solutions are recommended in ambient environments >50C, and/or for highly demanding inference operations >2.5W.

# 6 SoM Connector

## 6.1 Pinout

The following contains the pinout of 100-pin DF40C-100DP-0.4V(51) connector, part A.

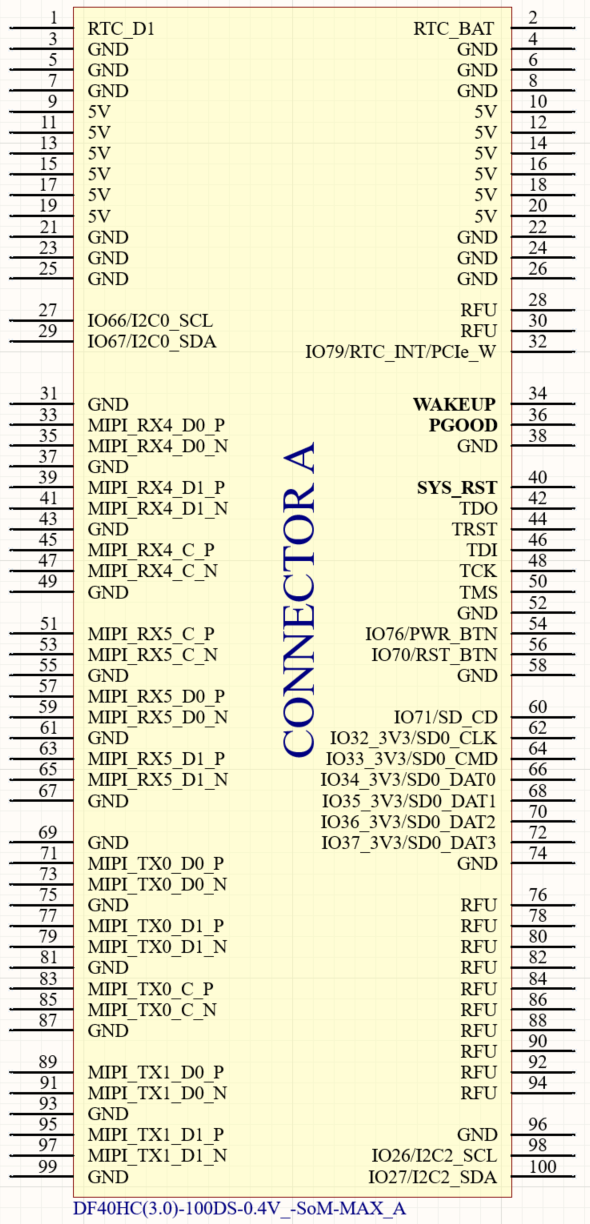


Figure 3 - Schematic Pinout, Connector A

The following contains the pinout of 100-pin DF40C-100DP-0.4V(51) connector, part B.

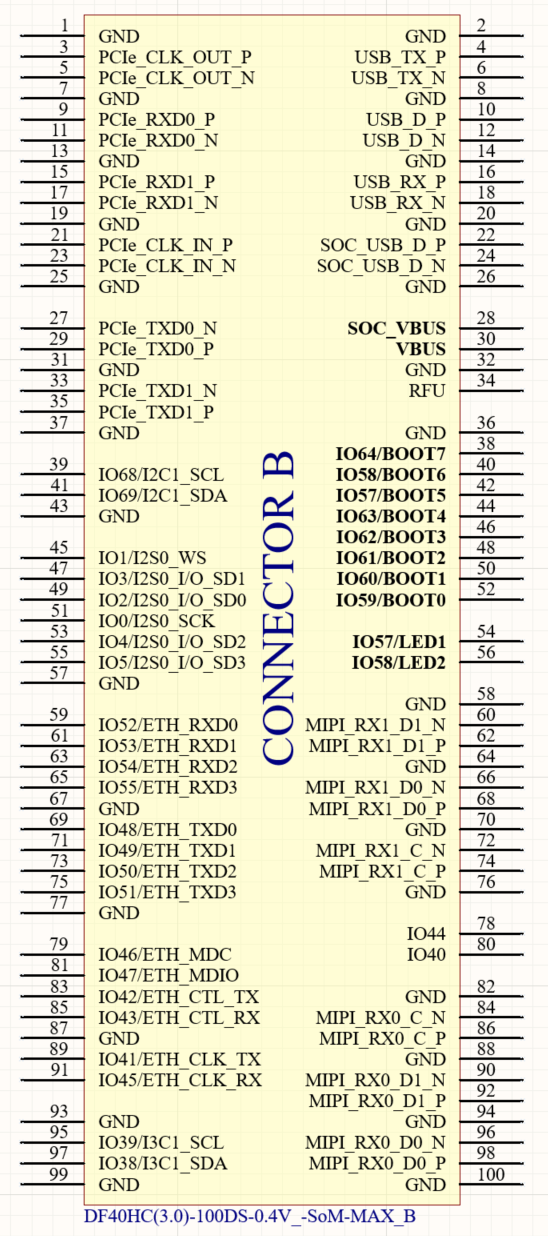


Figure 3 - Schematic Pinout, Connector B

The following contains the pinout of 100-pin DF40C-100DP-0.4V(51) connector, part C.

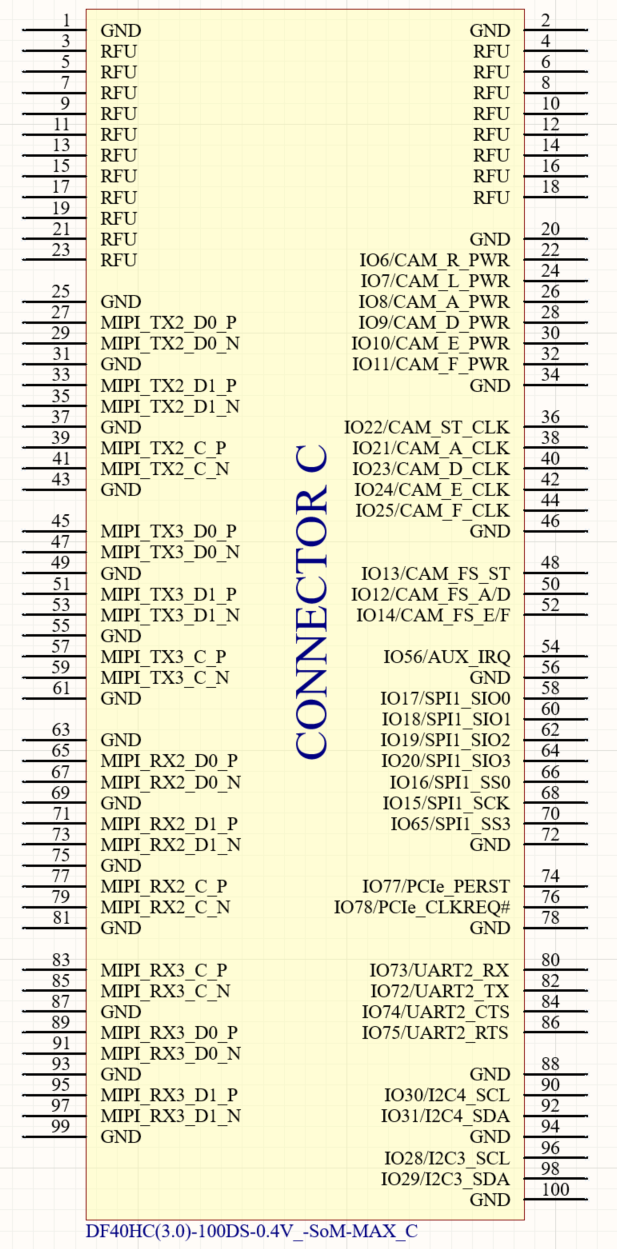


Figure 4 - Schematic Pinout, Connector C

## 6.2 I2C

The OAK-SoM-MAX SoM offers five dedicated I2C interfaces, I2C0, I2C1, I2C2, I2C3 and I2C4, additional one I3C1 (backwards compatible with I2C) is exposed by default. All does come with 2.2Kohm pull-up resistors (SDA & SCL) to the on-SoM 1.8V rail. For custom baseboard designs, all five I2C and one I3C interfaces are available and routed through the mezzanine connectors. I2C0 is already used for EEPROM which located on SoM. On baseboards, preferably the I2C1 interface is used for communication with the RGB color camera, the I2C2 interface is used to communicate with the pair of stereo cameras, the I2C3 is used for additional cameras or other peripherals such as programmability of PCIe. The I3C1 is typically unused but accessible through test points or connector pads.

### 6.2.1 EEPROM I2C0 Address Usage

The 32K I2C Serial EEPROM on most Luxonis baseboards is used for revision detect and a storage location for RTL8111HS driver if applicable. With functional address lines 7-bit address for EEPROM is set to 0x50. Use of the I2C0 interface on other components is possible, but with consideration of the existing usage of the EEPROM.

### 6.2.2 RGB Camera I2C1 Address Usage

The IMX378 RGB camera on most Luxonis baseboards uses some specific addresses as seen in Figure . Use of the I2C1 interface on other components is possible, but with consideration of the existing usage of the RGB camera.

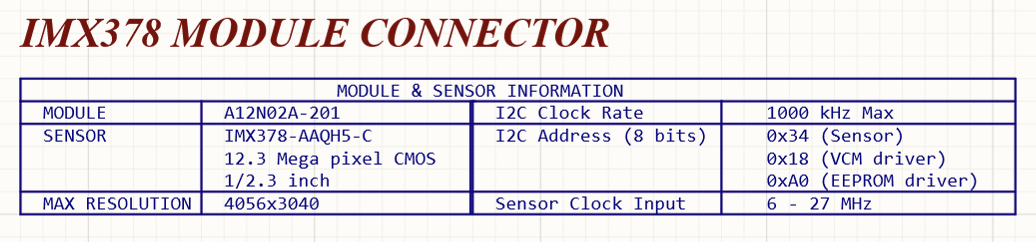


Figure 5 - Baseboard I2C1 RGB Camera Module Usage

### 6.2.3 Stereo Camera I2C2 Address Usage

The pair of OV9282 sensors comprising the stereo pair some Luxonis baseboards uses specific addresses as seen in Figure . Use of the I2C2 interface on other components is possible, but with consideration of the existing usage of the stereo camera.

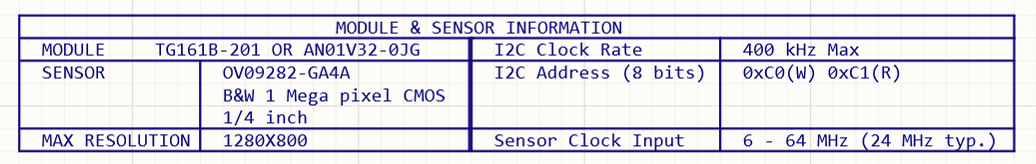


Figure 6 - Baseboard I2C2 Stereo Camera Module Usage

## 6.3 MIPI

Six MIPI CSI-2 DPHY interfaces are available as input to the SoM. Several variants are available upon request, default being six 2-lane MIPI, all allowing a maximum of 2.5Gbps (per lane).

Controller grouping can be done for following configurations:

* 6x 2-Lane MIPI
* 1x 4-Lane + 4x 2-Lane MIPI
* 2x 4-Lane + 2x 2-Lane MIPI

For each of the four camera interfaces, the inter-pair delay of that interface is matched to the clock pair within +/-1ps, and all pairs are routed with 100ohm differential impedance.

Three MIPI DSI-2 D-PHY channels one 4-lane and two 2-lane MIPI DSI-2 D-PHY are exposed, with maximum effective bit rate of 2.5 Gbps (per lane).

## 6.4 I2S

Four stereo inputs or outputs for microphones/speakers supporting I2S are available routed thorough mezzanine connector. With use of word select up to eight microphones can be connected to the interface and eight channel stereo audio device can be attached to the SoM. Supported only on hardware level at the moment.

|  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- |
| **Pin/**  **Conn. #** | **Pin name / Primary Function** | **SoM GPIO** | **Alt. 1** | **PU/PD on SoM** | **Pin Type** | **Description** |
| 49/B | I2S2\_I/O\_SD0 | IO\_2 |  |  | 1.8V GPIO | Typically used for I2S interface but can be reconfigured to any other GPIO. |
| 47/B | I2S2\_ I/O \_SD1 | IO\_3 |  |  | 1.8V GPIO | Typically used for I2S interface but can be reconfigured to any other GPIO. |
| 53/B | I2S2\_I/O \_SD2 | IO\_4 |  |  | 1.8V GPIO | Typically used for I2S interface but can be reconfigured to any other GPIO. |
| 55/B | I2S2\_ I/O\_SD3 | IO\_5 |  |  | 1.8V GPIO | Typically used for I2S interface but can be reconfigured to any other GPIO. |
| 45/B | I2S2\_WS | IO\_1 |  |  | 1.8V GPIO | Typically used for I2S interface but can be reconfigured to any other GPIO. |
| 51/B | I2S2\_SCK | IO\_0 |  |  | 1.8V GPIO | Typically used for I2S interface but can be reconfigured to any other GPIO. |

Table – I2S Pin Configuration

## 6.5 RGMII

The 1G Ethernet (GbE) block allows TX and RX of 10/100/1000Mbit Ethernet data using an external PHY via an RGMII interface. Feature set includes Full duplex and half duplex mode, IEEE 1588 Timestamp enabled, Remote wake up packet detection with 4 wake-up packet filters, MAC Management counters… The GbE enables a host to transmit and receive data over Ethernet in compliance with the IEEE 802.3- 2008.

## 6.6 PCIe

PCIe Gen 4 2-lane expansion bus is routed through mezzanine connector B. It supports all standard requirements of PCIe Rev 4.0, version 1.0. External reference clocking should be used for EP/RC applications. The reference clock signal used must be 100MHz.

|  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- |
| **Pin/**  **Conn. #** | **Pin name / Primary Function** | **SoM GPIO** | **Alt. 1** | **PU/PD on SoM** | **Pin Type** | **Description** |
| 35/B | SDS\_TXD1\_P | PCIe\_TXD1\_P |  | AC coupling | SDS | PCIe x2 lane transmitter data differential pair positive. Board implements AC coupling caps on board. |
| 33/B | SDS\_TXD1\_N | PCIe\_TXD1\_N |  | AC Coupling | SDS | PCIe x2 lane transmitter data differential pair negative. Board implements AC coupling caps on board. |
| 15/B | SDS\_RXD1\_P | PCIe\_RXD1\_P |  |  | SDS | PCIe x2 lane receiver data differential pair positive. |
| 17/B | SDS\_RXD1\_N | PCIe\_RXD1\_N |  |  | SDS | PCIe x2 lane receiver data differential pair negative. |
| 23/B | SDS\_IO\_CLKI\_N | PCIe\_CLKI\_N |  |  | SDS | PCIe differential reference clock input from clock generator negative. |
| 21/B | SDS\_IO\_CLKI\_P | PCIe\_CLKI\_P |  |  | SDS | PCIe differential reference clock input from clock generator positive. |
| 5/B | SDS\_IO\_CLKO\_N | PCIe\_CLKO\_N |  |  | SDS | PCIe differential reference clock output from clock generator negative. |
| 3/B | SDS\_IO\_CLKO\_P | PCIe\_CLKO\_P |  |  | SDS | PCIe differential reference clock output from clock generator positive. |
| 29/B | SDS\_TXD0\_P | PCIe\_TXD0\_P |  | AC coupling | SDS | PCIe x2 lane transmitter data differential pair positive. Board implements AC coupling caps on board. |
| 27/B | SDS\_TXD0\_N | PCIe\_TXD0\_N |  | AC Coupling | SDS | PCIe x2 lane transmitter data differential pair negative. Board implements AC coupling caps on board. |
| 9/B | SDS\_RXD0\_P | PCIe\_RXD0\_P |  |  | SDS | PCIe x2 lane receiver data differential pair positive. |
| 11/B | SDS\_RXD0\_N | PCIe\_RXD0\_N |  |  | SDS | PCIe x2 lane receiver data differential pair negative. |
| 76/B | PCIe\_CLKREQ\_N | IO\_78 |  |  | PCIe | Ref Clk request Signal |
| 74/B | PCIe\_PERST | IO\_77 |  |  | PCIe | Actve Low Reset Input to the add in Card. |

Table 2 – PCIe Pin Configuration

## 6.7 USB3.1 Gen2

USB3.1 is exposed it can operate as a device. Maximum of 10Gbps serial data rate can be achieved.

|  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- |
| **Pin/**  **Conn. #** | **Pin name / Primary Function** | **SoM GPIO** | **Alt. 1** | **PU/PD on SoM** | **Pin Type** | **Description** |
| 6/B | USB\_TX\_N | USB\_TX\_N |  |  | USB3 | USB 3.0 SSTX (-) / No AC caps on SoM / 0.5ps intra-pair tuning / 90ohm +/-10% |
| 4/B | USB\_TX\_P | USB\_TX\_P |  |  | USB3 | USB 3.0 SSTX (+) / No AC caps on SoM / 0.5ps intra-pair tuning / 90ohm +/-10% |
| 16/B | USB\_RX\_P | USB\_RX\_P |  |  | USB3 | USB 3.0 SSRX (+) / 0.5ps intra-pair tuning / 90ohm +/-10% |
| 18/B | USB\_RX\_N | USB\_RX\_N |  |  | USB3 | USB 3.0 SSRX (-) / 0.5ps intra-pair tuning / 90ohm +/-10% |
| 12/B | USB\_D\_N | USB\_D\_N |  |  | USB2 | USB 2.0 (-) / 2ps intra-pair tuning / 90ohm +/-10% |
| 10/B | USB\_D\_P | USB\_D\_P |  |  | USB2 | USB 2.0 (+) / 2ps intra-pair tuning / 90ohm +/-10% |
| 24/B | SOC\_USB\_D\_N | SOC\_USB\_D\_N |  |  | SOC\_USB2 | USB 2.0 (-) / 2ps intra-pair tuning / 90ohm +/-10%, SoC USB factory debug port |
| 22/B | SOC\_USB\_D\_P | SOC\_USB\_D\_P |  |  | SOC\_USB2 | USB 2.0 (+) / 2ps intra-pair tuning / 90ohm +/-10%, SoC USB factory debug port |
| 30/B | 5V/VBUS | 5V/VBUS |  |  | PWR | USB UFP VBUS sense input for VBUS detect. Can be tied to 5V. |
| 25/B | 5V/SoC\_VBUS | 5VSoC\_/VBUS |  |  | PWR | USB SoC VBUS sense input for VBUS detect. Can be connected to test point and left floating. |

Table 3 - USB Pin Configuration

## 6.8 eMMC

32GB eMMC with 5.1 host controller flash storage device on SoM can be used as a permanent storage medium and as storage location for firmware boot images. Fastest recommended eMMC boot mode can be selected with boot mode number 0x8F. Using 8 parallel data lines you can achieve 3Gbits per second data rate and 1.5Gbits data rate for HS400 and HS200 mode respectively.

## 6.9 PGOOD

PGOOD is a 1.8V open-drain output from the SoM PMIC and is pulled high when the PMIC evaluates power is good. PGOOD has a 10Kohm pull-up resistor to the on-SoM 1.8V rail.

This pin should be left floating if unused or tied to a high-impedance input to sense PGOOD. Do not pull or tie PGOOD to GND.

## 6.10 WAKEUP

WAKEUP is a 1.8V input to the SoM which is pulled to GND through a 1Kohm resistor on SoM. If driven high and sensed during the rising edge of \_RST power-on-reset, the on-chip e-fuse is used for boot selection. At present, this functionality is not used on any Luxonis SoM.

The WAKEUP pin was originally intended for waking the SoM from deep sleep mode, but this functionality is not supported on Luxonis SoMs. However, any IO can be used to trigger an interrupt and wake the SoM.

## 6.11 \_RST

\_RST is the active-low VPU reset input. \_RST has a 1.8V 10Kohm pull-up resistor on the SoM, and can be driven low from the baseboard to reset the RVC3.

## 6.12 Camera Reference Clocks

Six pins are used to provide a 24MHz reference clock to the image sensor ICs on the baseboard. IO21:IO24 are dedicated clock configurable outputs while IO25 does have the same controller as IO21 so it is better to use this one as GPIO. Each signal has a 121Kohm, pull down on the SoM. CAMA\_CLK is meant to be used for RGB cameras and CAMST\_CLK for grayscale stereo pair cameras and others can be used as needed. All configurable clock channels (four) are routed to these pins, If more clocks are needed, multiple cameras reference clock inputs can be shorted together using series resistor although clock buffers are recommended.

## 6.13 Camera Reset Signals

Six pins are used for individually resetting or powering down the RGB and stereo pair cameras. These signals are CAM\_R\_PWR, CAM\_L\_PWR, CAM\_A\_PWR , CAM\_D\_PWR , CAM\_E\_PWR and , CAM\_F\_PWR. Each of these signals is 1.8V and are active-low. No pull-up or pull-down resistors are on these signals on the SoM.

## 6.14 1.8V Shared SPI1 (QSPI)

The signals with prefix “SPI1” are part of a QSPI bus which is shared with the optional on-SoM NOR flash. All signals related to SPI1 are delay-matched on the SoM to +/-100ps to the connector interface.

|  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- |
| **Pin/**  **Conn. #** | **Pin name / Primary Function** | **SoM GPIO** | **Alt. 1** | **PU/PD on SoM** | **Pin Type** | **Description** |
| 60/A | SPI0\_SS\_3 | IO\_65 |  |  | 1.8V GPIO | GPIO, or can be configured as second CS for SPI0, MX in Controller or Peripheral mode. / +/-100ps inter-SPI0 |
| 70/A | SPI0\_SS\_0 | IO\_16 |  | PU: 1kR/1.8V | 1.8V GPIO | Hardwired to SoM on-board NOR S# / +/-100ps inter-SPI0 |
| 74/A | SPI0\_SCK | IO\_15 |  |  | 1.8V GPIO | Hardwired to SoM on-board NOR C / +/-100ps inter-SPI0 |
| 62/A | SPI0\_SIO0 | IO\_17 |  |  | 1.8V GPIO | Hardwired to SoM on-board NOR DQ0 / +/-100ps inter-SPI0 |
| 64/A | SPI0\_SIO1 | IO\_18 |  |  | 1.8V GPIO | Hardwired to SoM on-board NOR DQ1 / +/-100ps inter-SPI0 |
| 66/A | SPI0\_SIO2 | IO\_19 |  | PU: 1kR/1.8V | 1.8V GPIO | Hardwired to SoM on-board NOR W#/DQ2 / +/-100ps inter-SPI0 |
| 68/A | SPI0\_SIO3 | IO\_20 |  | PU: 1kR/1.8V | 1.8V GPIO | Hardwired to SoM on-board NOR DQ3/HOLD# / +/-100ps inter-SPI0 |

Table 4 - SPI0 Pin Configuration

With the NOR flash unpopulated the SPI1 bus can be used by the RVC3 in either controller or peripheral mode. With the RVC3 in controller mode, SPI1\_SS\_3 and SPI1\_SS\_0 can be used as chip selects for any baseboard peripherals, and additional baseboard chip selects can be configured by using IOs, if required. With the RVC3 in peripheral mode, either the SPI1\_SS\_3 or SPI1\_SS\_0 can be used by the baseboard controller to select the RVC3 as a peripheral. Unlike for controller mode, in peripheral mode, IOs cannot be configured as chip selects for the RVC3, only SPI1\_SS\_3 and SPI1\_SS\_0 can be used for this purpose.

With the NOR flash populated, the SPI1 bus can still be used by the RVC3 in either controller or peripheral mode, but the NOR flash now occupies the SPI1\_SS\_0 location so some care must be taken to avoid contention. With the NOR flash populated, and the RVC3 is in controller mode, the SPI0\_SS\_0 selects the NOR flash. SPI1\_SS\_3 (or other reconfigured IO) can be used as a second chip select for baseboard peripherals. When in peripheral mode SPI1\_SS\_3 should be used as the chip select for the peripheral RVC3 to avoid contention when communicating with NOR flash using SPI1\_SS\_0.

Note that when an external controller is accessing the NOR flash on the SoM, the RVC3 must not be allowed to access at the same time. Asserting \_RST for the RVC3 is an option to prevent this contention.

## 6.15 3.3V GPIO Bank

The SoM offers six GPIO which are 3.3V signaling for easy interface to common peripherals and devices with 3.3V signaling. These GPIO offer several configurations including SDIO, UART, PWM, and I2C, along with general purpose IO and are listed in Table .

|  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- |
| **Pin/**  **Conn. #** | **Pin name / Primary Function** | **SoM GPIO** | **Alt. 1** | **PU/PD on SoM** | **Pin Type** | **Description** |
| 66/A | IO\_34\_3V3 | IO\_34 | sd\_hst0\_dat\_0 | PU: 40.2kR/1.8V | 3.3V GPIO | 3.3V GPIO. Note PU/PD resistors that are configured for SDIO, but also compatible with SPI. / +/-100ps inter-SD\_HST |
| 62/A | IO\_32\_3V3 | IO\_32 | sd\_hst0\_clk | PU: 40.2kR/1.8V | 3.3V GPIO | 3.3V GPIO. Note PU/PD resistors that are configured for SDIO, but also compatible with SPI. / +/-100ps inter-SD\_HST |
| 61/A | IO\_33\_3V3 | IO\_33 | sd\_hst0\_cmd | PU: 40.2kR/1.8V | 3.3V GPIO | 3.3V GPIO. Note PU/PD resistors that are configured for SDIO, but also compatible with SPI. / +/-100ps inter-SD\_HST |
| 72/A | IO\_37\_3V3 | IO\_37 | sd\_hst0\_dat\_3 | PD: 300kR/GND | 3.3V GPIO | 3.3V GPIO. Note PU/PD resistors that are configured for SDIO, but also compatible with SPI. / +/-100ps inter-SD\_HST |
| 70/A | IO\_36\_3V3 | IO\_36 | sd\_hst0\_dat\_2 | PU: 40.2kR/1.8V | 3.3V GPIO | 3.3V GPIO. Note PU/PD resistors that are configured for SDIO, but also compatible with SPI. / +/-100ps inter-SD\_HST |
| 68/A | IO\_35\_3V3 | IO\_35 | sd\_hst0\_dat\_1 | PU: 40.2kR/1.8V | 3.3V GPIO | 3.3V GPIO. Note PU/PD resistors that are configured for SDIO, but also compatible with SPI. / +/-100ps inter-SD\_HST |

Table 5 - 3.3V GPIO Pin Configuration

### 6.16.1 3.3V GPIO Bank - SDIO

The 3.3V GPIO bank is nominally configured for use with SDIO, as appropriate pull-up and pull-down resistors exist on the SoM. CLK, CMD, and DAT[0:3] are available for use. Optional signals such as card detect can be implemented using the 1.8V GPIO.

### 6.16.2 1.8V GPIO

The default IO voltage for all GPIO is 1.8V, with the exceptions of the 3.3V GPIO listed in Table . Each IO can be muxed to alternate functionality, alternate functionalities will be at first muxed upon request case per case, when OAK-SoM-MAX matures as a product a default muxing table will be provided. In addition to muxed functionality, each IO is fully user-programmable with support or four output drive strengths (2mA, 4mA, 8mA, 12mA), selectable output slew-rate (slow/fast), open-drain output mode, LVCMOS/LVTTL compatible input modes with selectable hysteresis, programmable pull-up/pull-down input options, power-on-start capability, and no requirements for power sequencing. Additionally, 100MHz frequency can be achieved with less than 15pF external load, or up to 125MHz with less than 10pF external load.

|  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- |
| **Pin/**  **Conn. #** | **Pin name / Primary Function** | **SoM GPIO** | **PU/PD on SoM** | **Pin Type** | **Description** |
| 27/A | I2C0\_SCL | IO\_66 | PU: 2.2kR/1.8V | 1.8V GPIO | I2C clock |
| 29/A | I2C0\_SDA | IO\_67 | PU: 2.2kR/1.8V | 1.8V GPIO | I2C data |
| 54/A | PWR\_BTN | IO\_24 |  | 1.8V GPIO | User configurable IO meant as a software controller shutdown button |
| 56/A | RST\_BTN | IO\_13 |  | 1.8V GPIO | User configurable IO meant as a software reset button |
| 60/A | IO\_71 | IO\_71 |  | 1.8V GPIO | General purpose IO |
| 27/A | I2C2\_SCL | IO\_66 | PU: 2.2kR/1.8V | 1.8V GPIO | I2C clock |
| 29/A | I2C2\_SDA | IO\_67 | PU: 2.2kR/1.8V | 1.8V GPIO | I2C data |

Table 6 - 1.8V GPIO Pin Configuration (connector A)

|  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- |
| 38/B | **BOOT7** | IO\_64 | PD:  10kR/1.8V | 1.8V GPIO | GPIO BOOT pin, please use this as GPIO with extra care |
| 39/B | I2C1\_SCL | IO\_68 | PU: 2.2kR/1.8V | 1.8V GPIO | I2C clock, can be used as GPIO |
| 40/B | **BOOT6** | IO\_58 | PD:  10kR/1.8V | 1.8V GPIO | GPIO BOOT pin, please use this as GPIO with extra care |
| 41/B | I2C0\_SDA | IO\_69 | PU: 2.2kR/1.8V | 1.8V GPIO | I2C data, can be used as GPIO |
| 42/B | **BOOT5** | IO\_57 | PD:  10kR/1.8V | 1.8V GPIO | GPIO BOOT pin, please use this as GPIO with extra care |
| 44/B | **BOOT4** | IO\_63 | PD:  10kR/1.8V | 1.8V GPIO | GPIO BOOT pin, please use this as GPIO with extra care |
| 46/B | **BOOT3** | IO\_62 | PD:  10kR/1.8V | 1.8V GPIO | GPIO BOOT pin, please use this as GPIO with extra care |
| 48/B | **BOOT2** | IO\_61 | PD:  10kR/1.8V | 1.8V GPIO | GPIO BOOT pin, please use this as GPIO with extra care |
| 50/B | **BOOT1** | IO\_60 | PD:  10kR/1.8V | 1.8V GPIO | GPIO BOOT pin, please use this as GPIO with extra care |
| 52/B | **BOOT0** | IO\_59 | PD:  10kR/1.8V | 1.8V GPIO | GPIO BOOT pin, please use this as GPIO with extra care |
| 54/B | **BOOT5** | IO\_57 | PD:  10kR/1.8V | 1.8V GPIO | GPIO BOOT pin, please use this as GPIO with extra care |
| 56/B | **BOOT6** | IO\_58 | PD:  10kR/1.8V | 1.8V GPIO | GPIO BOOT pin, please use this as GPIO with extra care |
| 59/B | ETH\_PHY\_RXD0 | IO\_52 |  | 1.8V GPIO | RGMII data bus |
| 61/B | ETH\_PHY\_RXD1 | IO\_53 |  | 1.8V GPIO | RGMII data bus |
| 63/B | ETH\_PHY\_RXD2 | IO\_54 |  | 1.8V GPIO | RGMII data bus |
| 65/B | ETH\_PHY\_RXD3 | IO\_55 |  | 1.8V GPIO | RGMII data bus |
| 69/B | ETH\_PHY\_TXD0 | IO\_48 |  | 1.8V GPIO | RGMII data bus |
| 71/B | ETH\_PHY\_TXD1 | IO\_53 |  | 1.8V GPIO | RGMII data bus |
| 73/B | ETH\_PHY\_TXD2 | IO\_50 |  | 1.8V GPIO | RGMII data bus |
| 75/B | ETH\_PHY\_TXD3 | IO\_51 |  | 1.8V GPIO | RGMII data bus |
| 78/B | IO\_44 | IO\_44 |  | 1.8V GPIO | General purpose 1.8V IO |
| 79/B | IO\_40 | IO\_40 |  | 1.8V GPIO | General purpose 1.8V IO |
| 80/B | ETH\_GMII\_MDC | IO\_46 |  | 1.8V GPIO | RGMII control bus |
| 81/B | ETH\_GMII\_MDIO | IO\_47 |  | 1.8V GPIO | RGMII control bus |
| 83/B | ETH\_PYH\_CTL\_TX | IO\_42 |  | 1.8V GPIO | RGMII control bus |
| 85/B | ETH\_PYH\_CTL\_RX | IO\_43 |  | 1.8V GPIO | RGMII control bus |
| 89/B | ETH\_PYH\_CLK\_TX | IO\_41 |  | 1.8V GPIO | RGMII control bus |
| 91/B | ETH\_PYH\_CLK\_RX | IO\_45 |  | 1.8V GPIO | RGMII control bus |
| 41/B | I2C3\_SCL | IO\_39 | PU: 2.2kR/1.8V | 1.8V GPIO | I2C clock, can be used as GPIO |
| 41/B | I2C3\_SDA | IO\_38 | PU: 2.2kR/1.8V | 1.8V GPIO | I2C data, can be used as GPIO |

Table 7 - 1.8V GPIO Pin Configuration (connector B)

|  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- |
| 22/C | CAM\_R\_PWR | IO\_6 |  | 1.8V GPIO | Camera power control line |
| 24/C | CAM\_L\_PWR | IO\_7 |  | 1.8V GPIO | Camera power control line |
| 26/C | CAM\_A\_PWR | IO\_8 |  | 1.8V GPIO | Camera power control line |
| 28/C | CAM\_D\_PWR | IO\_9 |  | 1.8V GPIO | Camera power control line |
| 30/C | CAM\_E\_PWR | IO\_10 |  | 1.8V GPIO | Camera power control line |
| 32/C | CAM\_F\_PWR | IO\_11 |  | 1.8V GPIO | Camera power control line |
| 36/C | CAM\_ST\_CLK | IO\_22 | PD: 121kR/GND | 1.8V GPIO | Camera reference clock line |
| 38/C | CAM\_A\_CLK | IO\_21 | PD: 121kR/GND | 1.8V GPIO | Camera reference clock line |
| 40/C | CAM\_D\_CLK | IO\_23 | PD: 121kR/GND | 1.8V GPIO | Camera reference clock line |
| 42/C | CAM\_E\_CLK | IO\_24 | PD: 121kR/GND | 1.8V GPIO | Camera reference clock line |
| 44/C | (CAM\_F\_CLK) | IO\_25 | PD: 121kR/GND | 1.8V GPIO | Camera reference clock line (same clock output as IO21) |
| 48/C | CAM\_FS\_ST | IO\_13 |  | 1.8V GPIO | Camera frame sync I/O (can be used as FSYNC source or for detection of external FSYNC source) |
| 50/C | CAM\_FS\_A/D | IO\_12 |  | 1.8V GPIO | Camera frame sync I/O (can be used as FSYNC source or for detection of external FSYNC source) |
| 52/C | CAM\_FS\_E/F | IO\_14 |  | 1.8V GPIO | Camera frame sync I/O (can be used as FSYNC source or for detection of external FSYNC source) |
| 54/C | AUX\_IO\_IRQ | IO\_56 |  | 1.8V GPIO | Auxiliary interrupt input, can be used as GPIO |
| 58/C | SPI1\_SIO0 | IO\_17 |  | 1.8V GPIO | Hardwired to SoM on-board NOR DQ0 / +/-100ps inter-SPI1 |
| 60/C | SPI1\_SIO1 | IO\_18 |  | 1.8V GPIO | Hardwired to SoM on-board NOR DQ1 / +/-100ps inter-SPI1 |
| 62/C | SPI1\_SIO2 | IO\_19 | PU: 1kR/1.8V | 1.8V GPIO | Hardwired to SoM on-board NOR W#/DQ2 / +/-100ps inter-SPI1 |
| 64/C | SPI1\_SIO3 | IO\_20 | PU: 1kR/1.8V | 1.8V GPIO | Hardwired to SoM on-board NOR DQ3/HOLD# / +/-100ps inter-SPI1 |
| 66/C | SPI1\_SS\_0 | IO\_16 | PU: 1kR/1.8V | 1.8V GPIO | Hardwired to SoM on-board NOR S# / +/-100ps inter-SPI1 |
| 68/C | SPI1\_SCK | IO\_15 |  | 1.8V GPIO | Hardwired to SoM on-board NOR C / +/-100ps inter-SPI1 |
| 70/C | SPI1\_SS\_3 | IO\_65 |  | 1.8V GPIO | GPIO, or can be configured as second CS for SPI1, MX in Controller or Peripheral mode. / +/-100ps inter-SPI1 |
| 80/C | UART2\_RX | IO\_73 |  | 1.8V GPIO | Typically labeled as UART\_RX on Luxonis baseboards. |
| 82/C | UART2\_TX | IO\_72 |  | 1.8V GPIO | Typically labeled as UART\_TX on Luxonis baseboards |
| 84/C | UART2\_CTS | IO\_74 |  | 1.8V GPIO | UART\_CTS |
| 86/C | UART2\_RTS | IO\_75 |  | 1.8V GPIO | UART\_RTS |
| 90/C | I2C4\_SCL | IO\_30 | PU: 2.2kR/1.8V | 1.8V GPIO | I2C clock, can be used as GPIO |
| 92/C | I2C4\_SDA | IO\_31 | PU: 2.2kR/1.8V | 1.8V GPIO | I2C data, can be used as GPIO |
| 96/C | I2C3\_SCL | IO\_28 | PU: 2.2kR/1.8V | 1.8V GPIO | I2C clock, can be used as GPIO |
| 98/C | I2C3\_SDA | IO\_29 | PU: 2.2kR/1.8V | 1.8V GPIO | I2C data, can be used as GPIO |

Table 7 - 1.8V GPIO Pin Configuration (connector C)

## 6.17 RTC

Onboard RTC offers low-current, real-time clock (RTC) nano amperes time-keeping extending battery life and allowing smaller battery to be used on base board.

RTC can be accessed through an I2C serial interface featuring one digital Schmitt trigger input and one programmable threshold analog input. Interrupt output on falling/rising edge of the digital input (D1), is routed to connector A. Other features include two time-of-day alarm, the clock/calendar provides seconds, minutes, hours, day, date, month, and year information.

|  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- |
| **Pin/**  **Conn. #** | **Pin name / Primary Function** | **SoM GPIO** | **Alt. 1** | **Alt. 2** | **PU/PD on SoM** | **Pin Type** | **Description** |
| 1/A | RTC\_D1 |  |  |  |  | 1.8V GPIO | Onboard RTC digital input |
| 2/A | RTC\_BAT |  |  |  |  | 1.8V GPIO | Battery coin connection point (battery not populated on SoM) |
| 32/A | RTC\_INT | IO\_97 |  |  |  | 1.8V GPIO | RTC clock input/interrupt output pre-connected to SoM GPIO, in case of INT not needed pin can be used as any other GPIO |

Table 8 – RTC Pin Configuration (connector A)

## 6.17 JTAG

JTAG used to access the RVC3 for debugging is connected only to the onboard FPC connector, routed through the 100pin mezzanine connector to be accessed on the base board.

# 7 BOOT Modes

The boot signals are broken out from the SoM and routed through the mezzanine connector which offers the end user the option to easily configure the boot mode by setting the BOOT[7:0] bits high (1.8V) or low. Bits are sampled on the rising edge of \_RST during power-on-reset, and allow for boot from USB and eMMC currently supported.

To configure the eMMC flash boot mode, set the bits to 0xF [0b00001111].

To configure eMMC recovery USB boot, set the bits to 0x8F [0b10001111]. In this configuration, the RVC3 will boot using the USB 2 interface.

|  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- |
| **Pin/**  **Conn. #** | **Pin name / Primary Function** | **SoM GPIO** | **Alt. 1** | **Alt. 2** | **PU/PD on SoM** | **Pin Type** | **Description** |
| 28/B | BOOT7 | IO\_64 |  |  |  | 1.8V set BOOT pin | Boot register set pin bit 7 |
| 58/B | BOOT6 | IO\_58 |  |  |  | 1.8V set BOOT pin | Boot register set pin bit 6 |
| 56/B | BOOT5 | IO\_57 |  |  |  | 1.8V set BOOT pin | Boot register set pin bit 5 |
| 18/B | BOOT4 | IO\_63 |  |  |  | 1.8V set BOOT pin | Boot register set pin bit 4 (MSB) |
| 20/B | BOOT3 | IO\_62 |  |  |  | 1.8V set BOOT pin | Boot register set pin bit 3 |
| 22/B | BOOT2 | IO\_61 |  |  |  | 1.8V set BOOT pin | Boot register set pin bit 2 |
| 24/B | BOOT1 | IO\_60 |  |  |  | 1.8V set BOOT pin | Boot register set pin bit 1 |
| 26/B | BOOT0 | IO\_59 |  |  |  | 1.8V set BOOT pin | Boot register set pin bit 0 (LSB) |

Table 8 - BOOT Pin Configuration

# 8 SoM LEDs

There are two Light Emitting Diodes located on the edge of the OAK-SoM-MAX. Both are driven with IO and the functionality is user configurable. LED1 is signaling boot status by default while LED2 is signaling product connection status to RobotHUB.

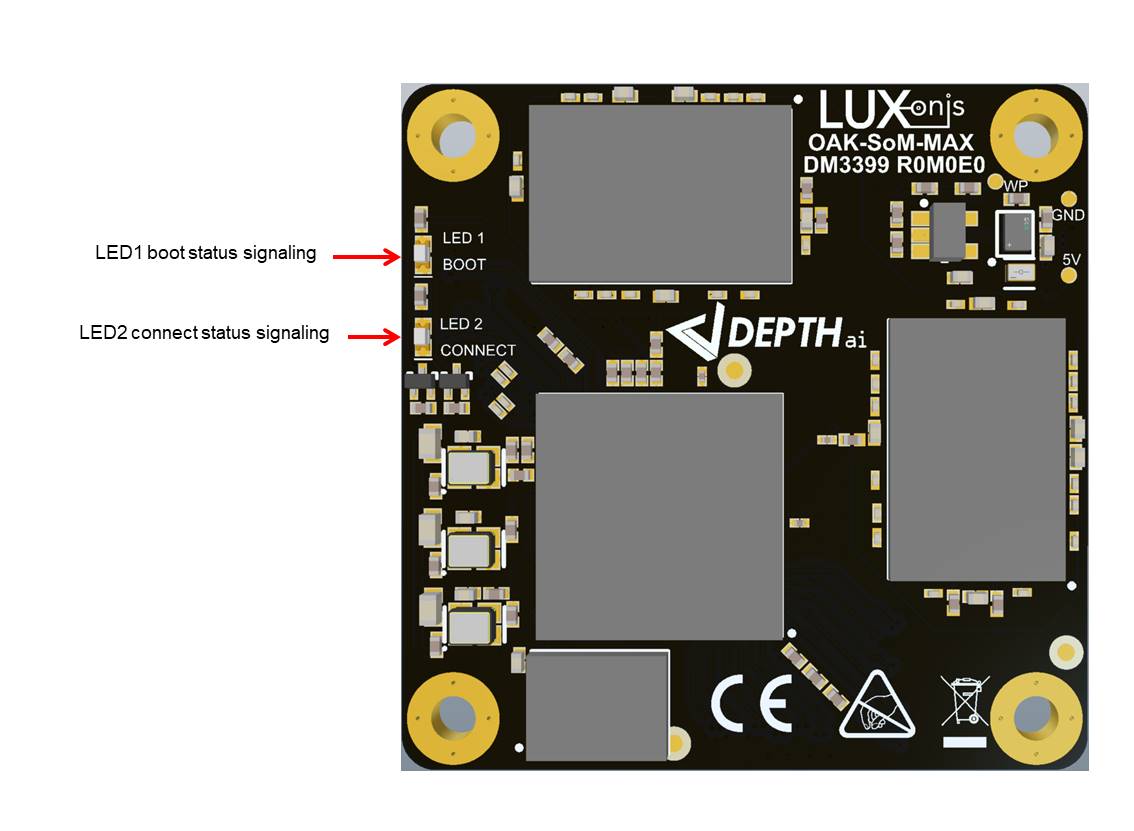


Figure 5 - Baseboard I2C2 Stereo Camera Module Usage

# 8 Mechanical Information

The following information is [the most](http://www.ti.com/corp/docs/legal/termsofuse.shtml) [current](http://www.ti.com/corp/docs/legal/termsofuse.shtml) data available for the designated device. This data is subject to change without notice and without revision of this document.

## 8.1 OAK-SoM-MAX Dimensions

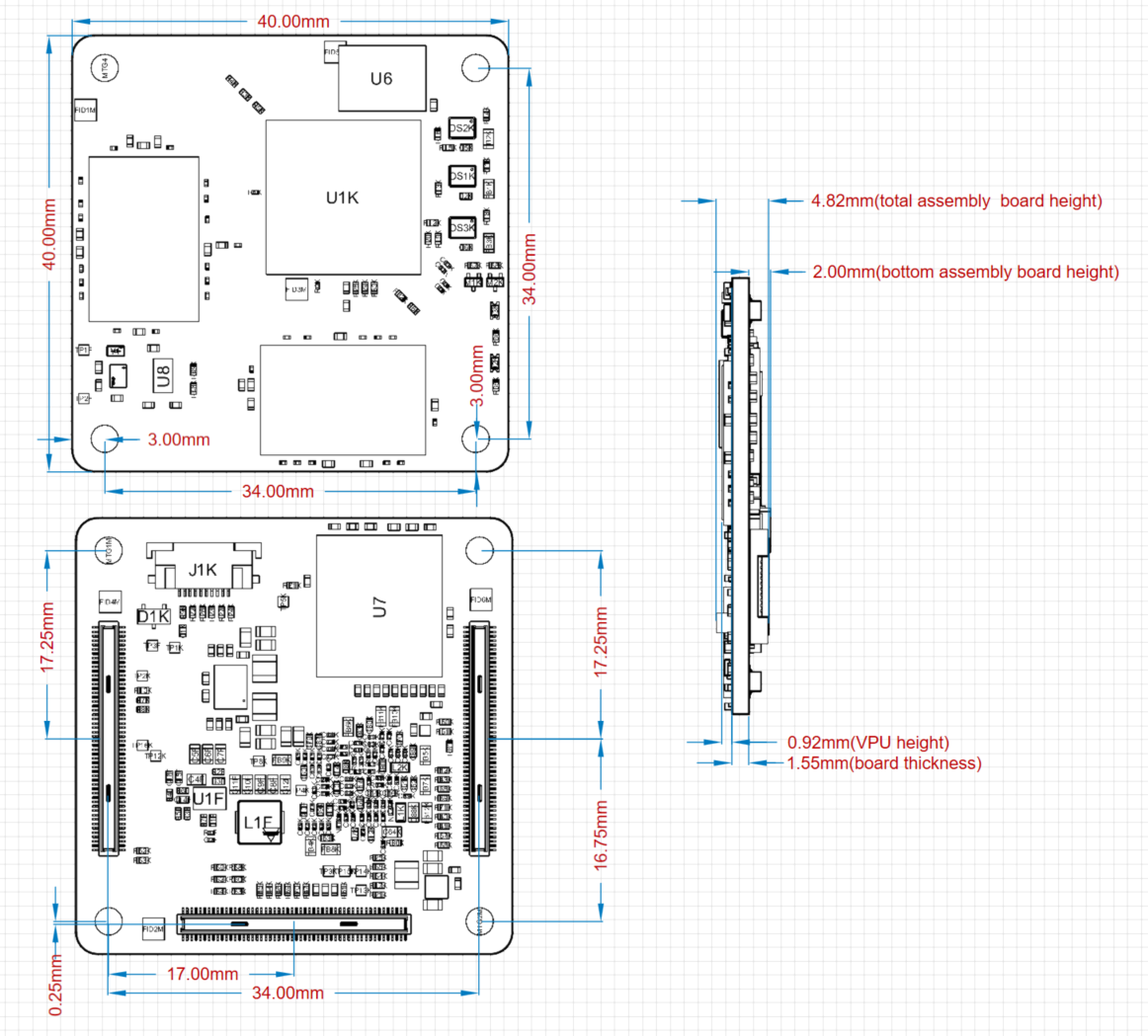


Figure 9 – Top, Bottom, and Side dimensions

## 8.2 Recommended Mounting Configuration

The OAK-SoM-MAX SoM is designed to be used with a 4x 3mm mated-height connector and accompanying 3mm standoffs. The B2B connector plugs are on the OAK-SoM-MAX (Hirose DF40C-100DP-0.4V), while the receptacle, which determines mated height, is on the baseboard (Hirose DF40HC(3.0)-100DS-0.4V). Wuerth Elektronik 9774030243R SMT standoffs are recommended.

## 8.3 OAK-SoM-MAX Mounting Holes

The OAK-SoM-MAX has 4 M2.5 mounting holes for securing the SoM. These mounting holes use a 2.6mm ID, and a 5.5mm OD pad, which is tied to SoM GND. M2-0.40 screws can be used with these pads to secure the SoM to the recommended Wuerth Elektronik 9774030243R SMT standoffs, or a custom solution using M2-0.40 or M2.5-0.45 screws can be used. Note that when using M2.5-0.45 screws, there is reduced tolerance between the B2B connector clocking and the screws’ hole alignment. This must be accounted for to ensure proper connector mating.

## 8.4 SoM Clearance

3mm is the board-to-board standoff height when using the recommended mounting configuration; however, components on the underside of the OAK-SoM-MAX reduce this clearance. For highest design reliability, it is recommended not to place components on the baseboard underneath the SoM, in case that is needed in the design, care must be taken in regard to clearance and noise coupling between SoM and baseboard components considering the noise immunity.

In previous designs many components have been successfully placed on the baseboard beneath the SoM making careful use of the 3D STEP file of the SoM, which is available online here [OAK-SoM-MAX](https://github.com/luxonis/depthai-hardware/tree/master/SoMs/OAK-SoM-Max).

# 9 Thermal Information

Power consumption can vary considerably depending on the application. A stereo vision application running Mobilenet-SSD V2 at 30fps typically consumes about 5.5W, but more aggressive applications can consume closer to 8W. Most of this power is consumed by the VPU. While the VFBGA provides an excellent thermal path from the VPU to the SoM, the thermal sink is small, and the part temperature can quickly rise toward the 105C max die temperature.

Heatsinking of the VPU is required for most applications, Luxonis does provide a custom made heatsink and TIM that can be attached to the SoM by using the same 4 screws as for mounting to baseboard, note that longer screws must be used in this case.

Table 2 details thermal parameters for the VPU simulated in a still air environment, an ambient temperature of 25C, 2W power dissipation, and under the test conditions described in JESD51-2A.

|  |  |  |
| --- | --- | --- |
| **Parameter** | **Value (C/W)** | **Description** |
| θJB | 5.95 | Junction-to-board thermal resistance (EIA/JESD51-8) |
| θJC | 0.029 | Junction-to-case thermal resistance |
| θJA | 19.30 | Junction-to-ambient thermal resistance (EIA/JESD51-2) |

Table - MA2485 Thermal Parameters

# 10 Revision History

* Initial Release – Jan 2023
  + Fixed SPI1 annotations in Table 7 – March 2023