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| --- | --- | --- | --- | --- |
|  | **Course:** | **COAL** | **Course Code:** | **EE-2003** |
|  | **Program:** | **BS (Computer Science)** | **Semester:** | **SPRING 2024** |
|  | **Deadline:** | **4th May'2024 (During Evaluation)** | **Total Marks:** | **10** |
|  | **Section:** | **BCS-4B**  **ASSIGNMENT-9** | **Roll number:** |  |

**Question:1 (10)**

It takes 15µs to complete one instruction in a non-pipelined processor. We were able to convert the circuit to a 6 stage pipeline processor. Stage 1 to 6 take 2μs, 1.5μs, 3μs, 4μs, 1.5μs, 3μs resp. Time to move from one pipe stage to another is 2μs.

**Calculate the following values for pipeline and non-pipelined processor** (Write the answer in the given table)

|  |  |  |
| --- | --- | --- |
| **Value** | **Non-Pipeline** | **Pipeline** |
| Clock Cycle |  |  |
| Clock Speed |  |  |
| Latency |  |  |
| Throughput for 46 instructions |  |  |
| Throughput for 1 instruction |  |  |
| Speedup of pipeline processor for  1 instruction |  |  |
| Speedup of pipeline processor for  75 instructions |  |  |