Lab 3 – multi-cycle controller

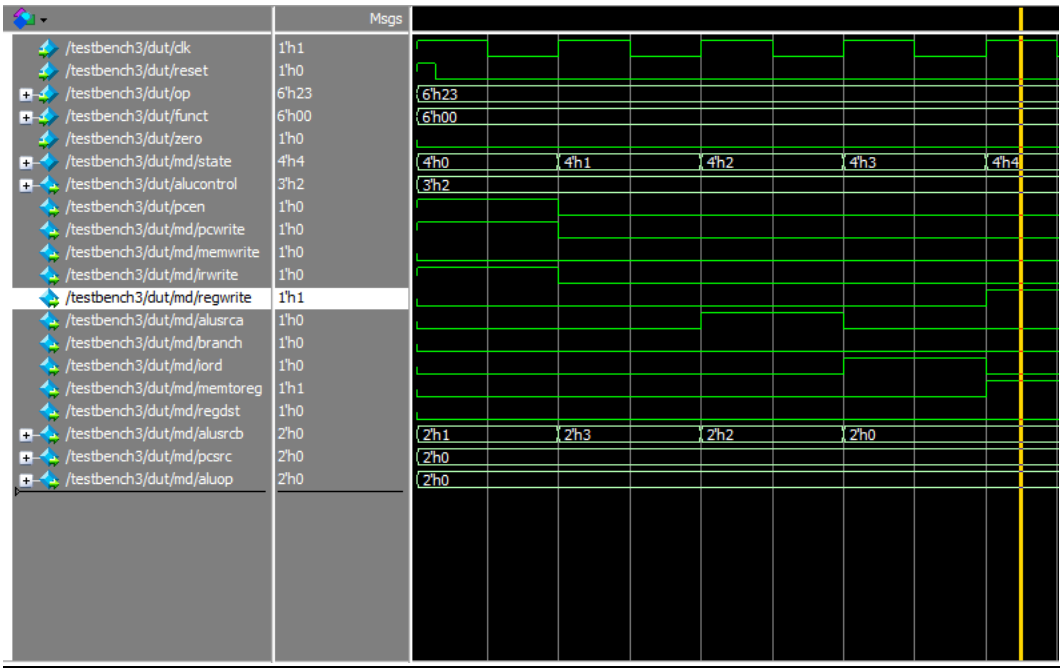
Hassan El-Seoudy	3780
Merna Adel	4168
Mahmoud Mohamed	2718
Bavly George Micheal	3756

Main decoder output table:

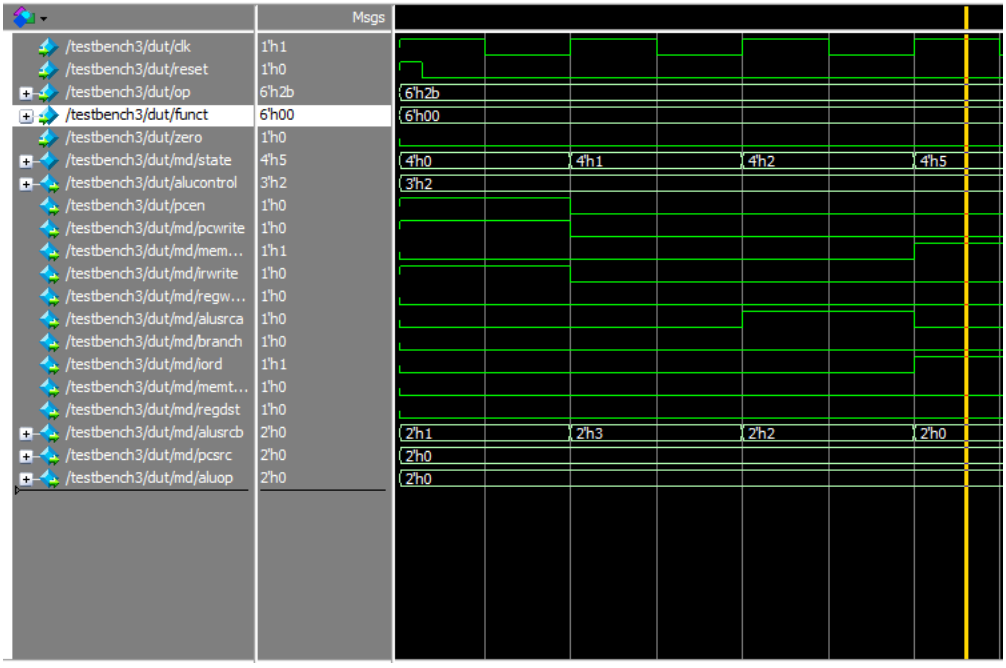
state	PCWrite	MemWrite	IRWrite	RegWrite	ALUSrcA	Branch	IorD	MemToReg	RegDst	ALUSrcB[1:0]	PCRSrc[1:0]	ALUOp	hexa
Fetch	1	0	1	0	0	0	0	0	0	01	00	00	5010
Decode	0	0	0	0	0	0	0	0	0	11	00	00	0030
memAdr	0	0	0	0	1	0	0	0	0	10	00	00	0420
memRD	0	0	0	1	0	0	0	1	0	00	00	00	0880
memWB	0	1	0	0	0	0	1	0	0	00	00	00	2100
memWR	0	0	0	0	1	0	0	0	0	00	00	00	0400
RtypeEX	0	0	0	0	0	0	0	1	1	00	00	10	00C2
RtypeWB	0	0	0	0	0	1	0	0	0	00	00	00	0840
BeqEx	0	0	0	0	1	0	0	0	0	00	01	01	0605
AddiEx	0	0	0	0	1	0	0	0	0	10	00	00	0420
AddiWB	0	0	0	1	0	0	0	0	0	00	00	00	0800
JEx	1	0	0	0	0	0	0	0	0	00	10	00	4008

Note:
The system Verilog code for controller, maindec and aludec modules as well as the test bench file can be found in this link:
https://github.com/Hassan-Elseoudy/MIPS-MultiCycle

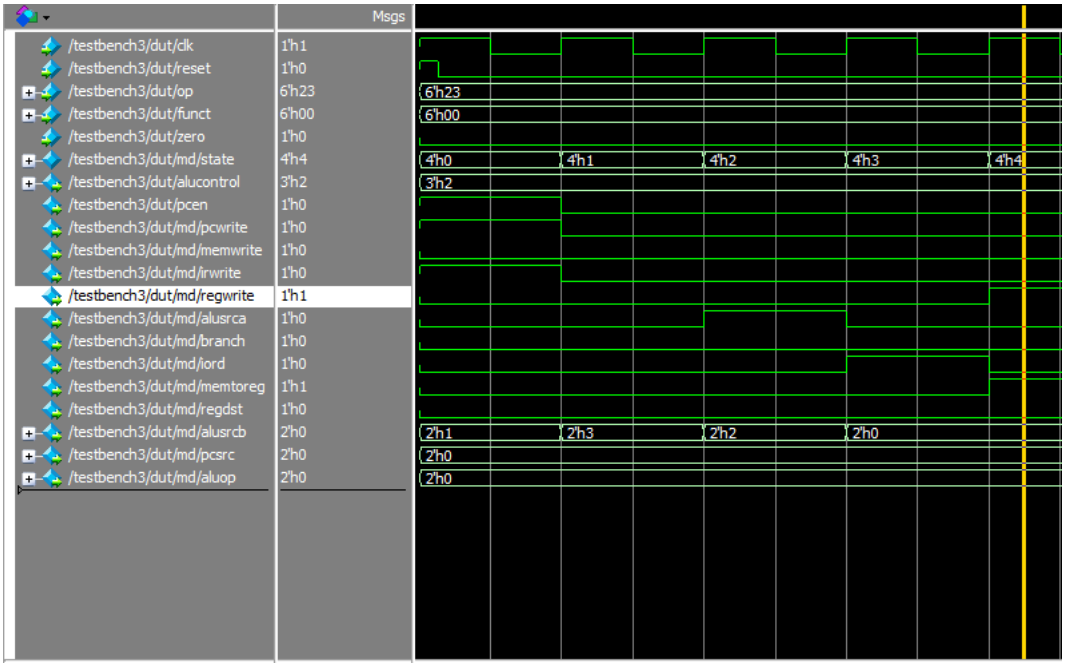
Simulation waveforms:



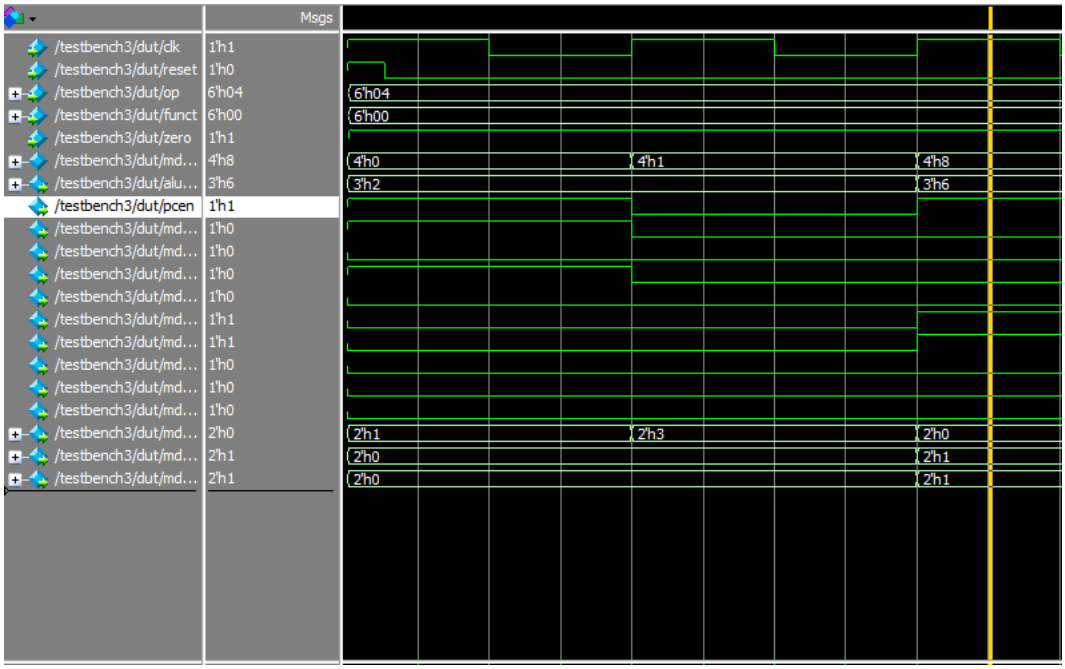
Waveform for lw instruction



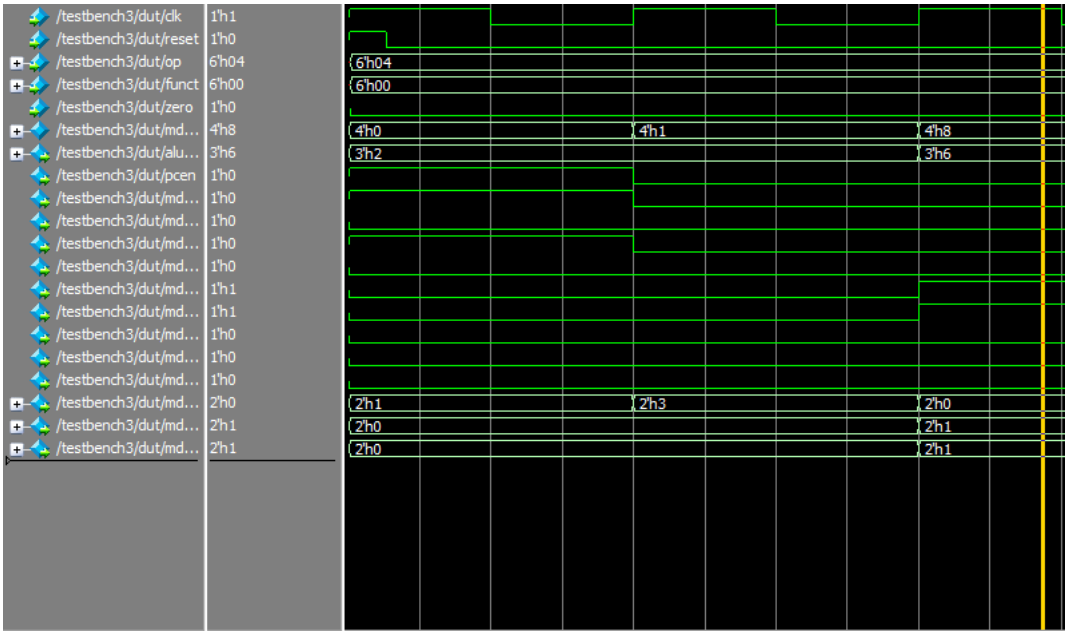
Waveform for sw instruction



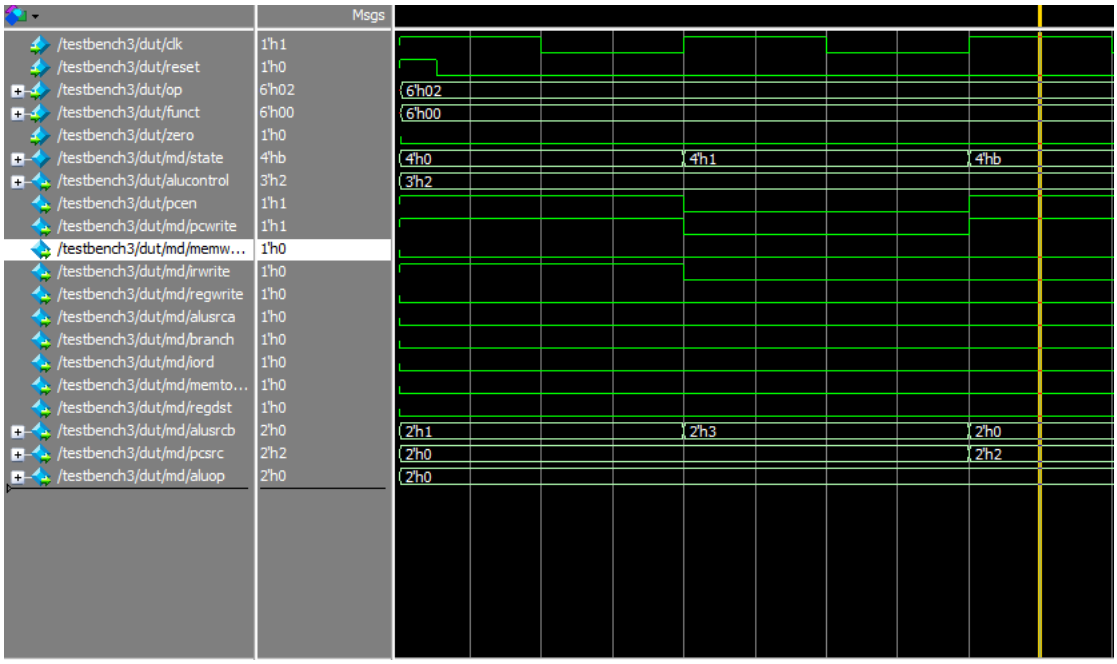
Waveform for R-type instruction



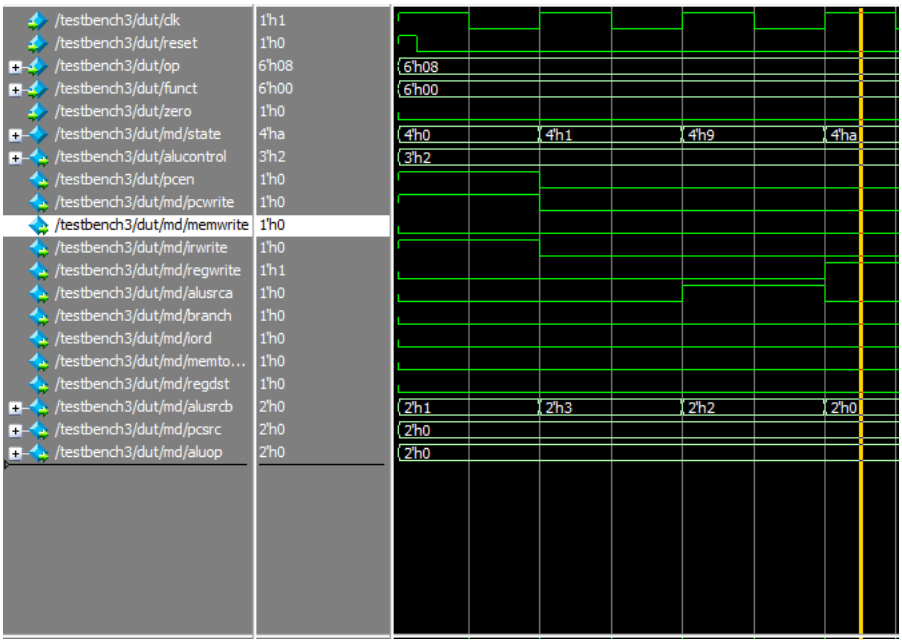
Waveform for beq instruction (branch taken)



Waveform for beq instruction (branch not taken)



Waveform for j instruction



Waveform for addi instruction