**Truth Table:**

|  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| a | b | c | a1 | a2 | a3 | a4 | a5 | x | y |
| 0 | 0 | 0 | 1 | 0 | 1 | 0 | 1 | 1 | 0 |
| 0 | 0 | 1 | 0 | 0 | 1 | 0 | 1 | 0 | 0 |
| 0 | 1 | 0 | 1 | 1 | 0 | 1 | 0 | 0 | 0 |
| 0 | 1 | 1 | 0 | 1 | 0 | 1 | 0 | 1 | 0 |
| 1 | 0 | 0 | 1 | 1 | 0 | 1 | 0 | 0 | 0 |
| 1 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 1 | 0 |
| 1 | 1 | 0 | 1 | 1 | 0 | 1 | 1 | 0 | 1 |
| 1 | 1 | 1 | 0 | 1 | 0 | 1 | 1 | 1 | 1 |

**Errors (listing 4):**

1. There is a “,” after “carry”.
2. At line 8, we should use “always\_comb ” and “begin”.
3. And use “end” in line 11.
4. There should be sign “&” after c in line 10.

**Error (listing 5):**

1. In line 6, there should be “logic carry1”.
2. There should be “DUT” in line 7.
3. There should be a1,b1,c1 in line 18.
4. There should be c1 intead of c in line 20.
5. We have to change the time period of input.
6. There should be b1 instead of b in line 24.
7. There should be a1 instead of a in line 30.
8. There will be “end” before “endmodule”.