**EXPERIMENT NO.4**

**COMBINATIONAL CIRCUIT DESIGN USING K-MAPS**

SUBMITTED TO:

Dr. Ubaid Ullah Fayyaz

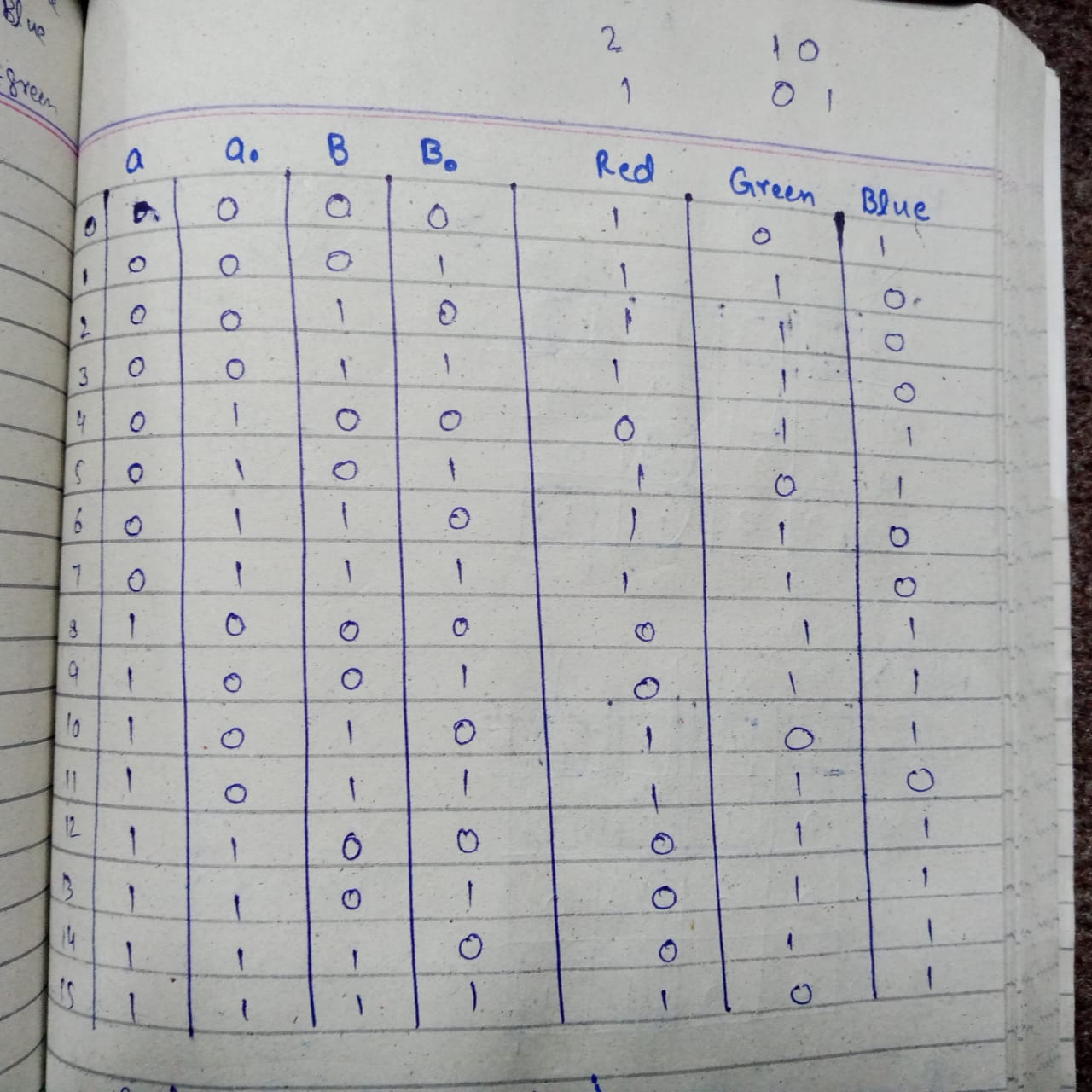
SUBMITTED BY:

Hassan Muavia

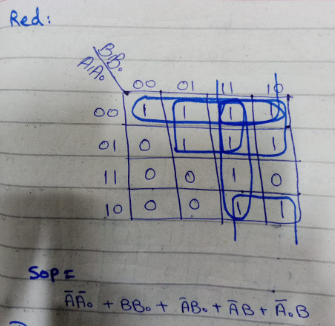
2022-EE-162

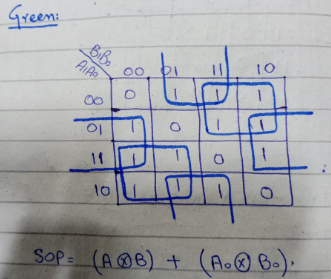
**UNIVERSITY OF ENGINEERING & TECHNOLOGY, LAHORE**

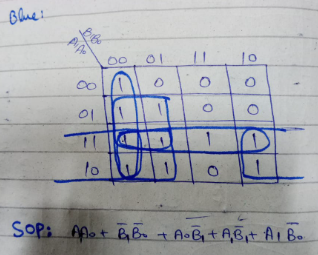
**Truth Table:**

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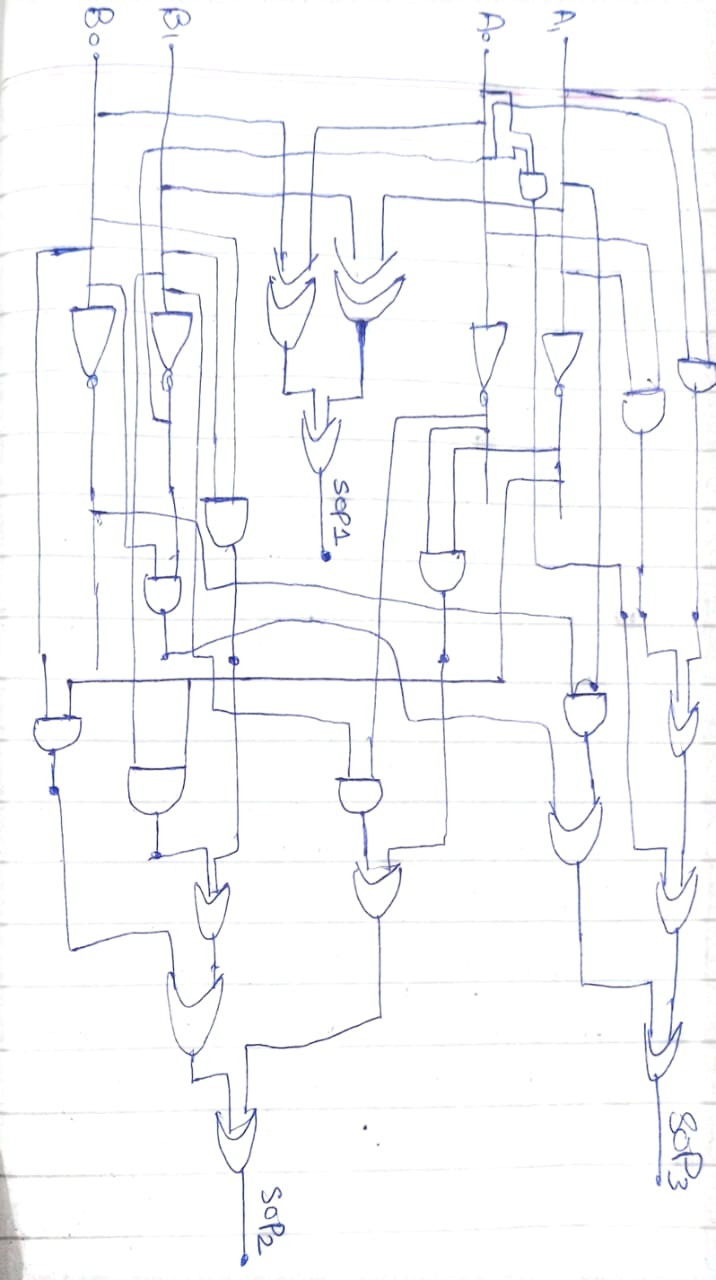
**K-maps:**



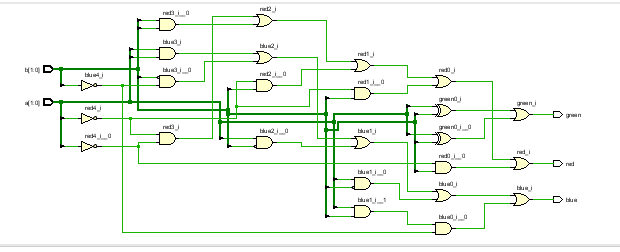




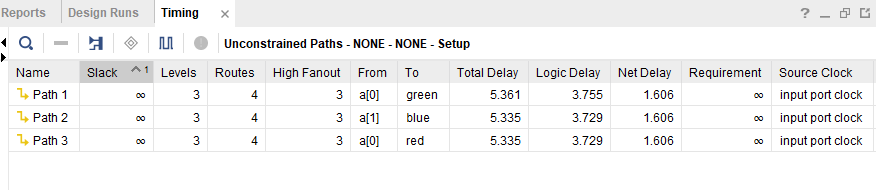
**Circuit Diagram:**



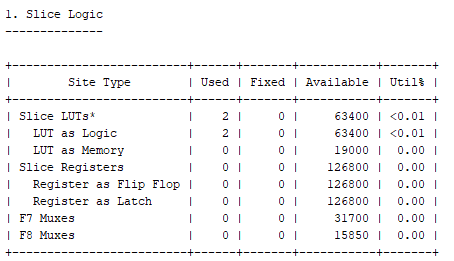
**Circuit diagram using vivado:**

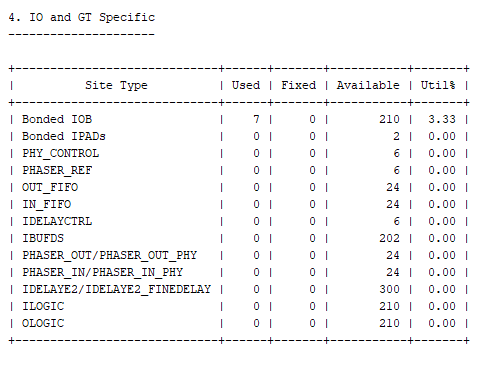


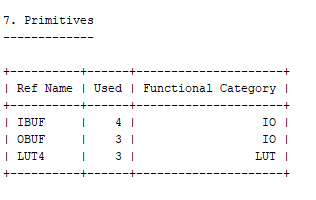
Delay in synthesis:



**Resource Utilization:**







**System Verilog Code:**

