EXPERIMENT NO. 3

COMBINATIONAL CIRCUITS:

STRUCTURAL MODELING USING VIVADO

SUBMITTED TO:

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SUBMITTED BY:

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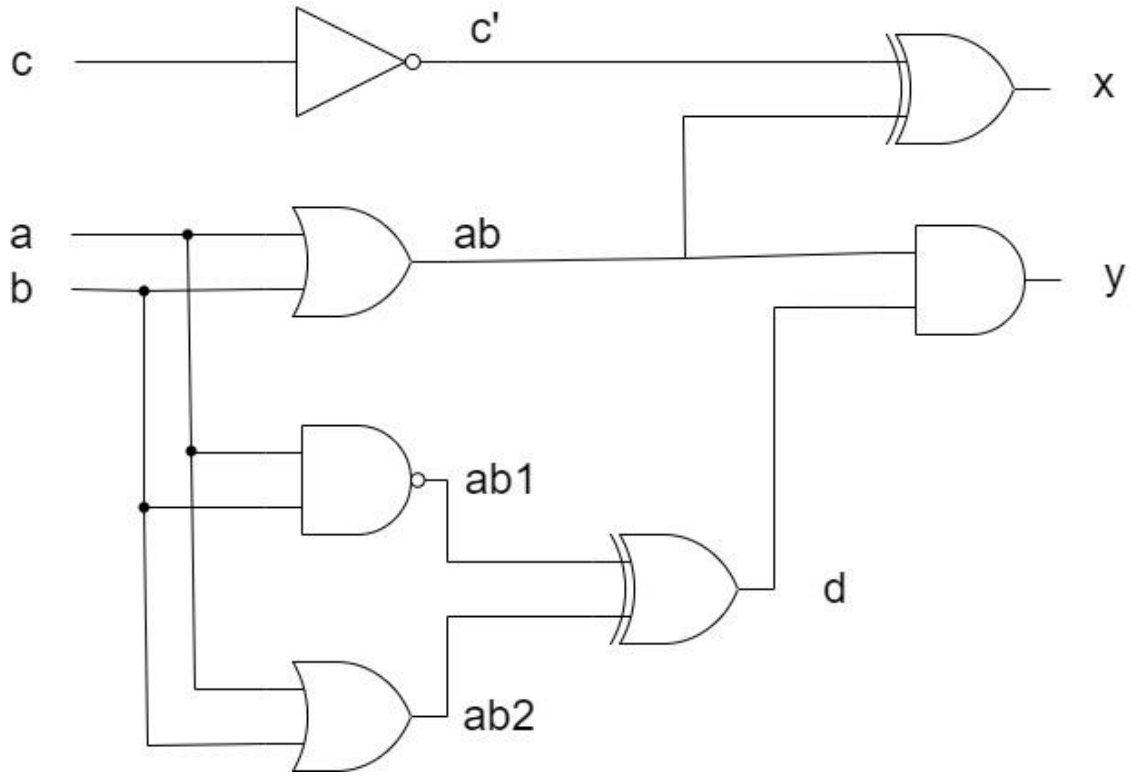
UNIVERSITY OF ENGINEERING AND TECHNOLOGY,

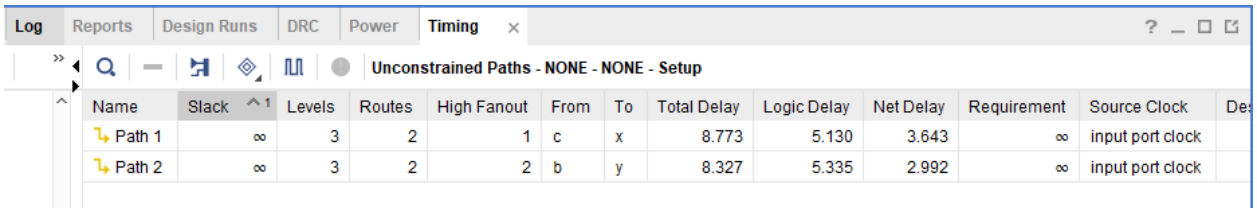
LAHORE

TRUTH TABLE:

a	b	c	a1	a2	a3	a4	a5	x	y
0	0	0	1	0	1	0	1	1	0
0	0	1	0	0	1	0	1	0	0
0	1	0	1	1	0	1	0	0	0
0	1	1	0	1	0	1	0	1	0
1	0	0	1	1	0	1	0	0	0
1	0	1	0	1	0	1	0	1	0
1	1	0	1	1	0	1	1	0	1
1	1	1	0	1	0	1	1	1	1



TIME DELAY:



Log | Reports | Design Runs | DRC | Power | Timing

Unconstrained Paths - NONE - NONE - Setup

Name	Slack	Levels	Routes	High Fanout	From	To	Total Delay	Logic Delay	Net Delay	Requirement	Source Clock	De
Path 1	∞	3	2	1	c	x	8.773	5.130	3.643	∞	input port clock	
Path 2	∞	3	2	2	b	y	8.327	5.335	2.992	∞	input port clock	

RESOURCES UTILIZATION:

1. Slice Logic

Site Type	Used	Fixed	Available	Util%
Slice LUTs*	1	0	63400	<0.01
LUT as Logic	1	0	63400	<0.01
LUT as Memory	0	0	19000	0.00
Slice Registers	0	0	126800	0.00
Register as Flip Flop	0	0	126800	0.00
Register as Latch	0	0	126800	0.00
F7 Muxes	0	0	31700	0.00
F8 Muxes	0	0	15850	0.00

* Warning! The Final LUT count, after physical optimizations and full

4. IO and GT Specific

Site Type	Used	Fixed	Available	Util%
Bonded IOB	5	0	210	2.38
Bonded IPADs	0	0	2	0.00
PHY_CONTROL	0	0	6	0.00
PHASER_REF	0	0	6	0.00
OUT_FIFO	0	0	24	0.00
IN_FIFO	0	0	24	0.00
IDELAYCTRL	0	0	6	0.00
IBUFDS	0	0	202	0.00
PHASER_OUT/PHASER_OUT_PHY	0	0	24	0.00
PHASER_IN/PHASER_IN_PHY	0	0	24	0.00
IDELAYE2/IDELAYE2_FINEDELAY	0	0	300	0.00
ILOGIC	0	0	210	0.00
OLOGIC	0	0	210	0.00

7. Primitives

Ref Name	Used	Functional Category
IBUF	3	IO
OBUF	2	IO
LUT3	1	LUT
LUT2	1	LUT