Tasks and System Parameters

Task1: Button1_Monitor

E	16 us
Р	50 ms
D	50 ms

Task2: Button2_Monitor

E	16 us
Р	50 ms
D	50 ms

Task3: Periodic_Transmitter

E	14 us
Р	100ms
D	100 ms

Task4: Uart_Reciever

E	22 us
Р	20 ms
D	20 ms

Task5: LOAD1

E	5 ms
Р	10 ms
D	10 ms

Task6: LOAD2

E	12 ms
Р	100 ms
D	100 ms

• Hyperperiod (H) = 100 ms

• CPU Load (U)=
$$\frac{(E1*2)+(E2*2)+(E3*1)+(E4*5)+(E5*10)+(E6*1))}{H} = 62.188 \%$$

System Schedulability

1) Rate-Monotonic Utilization Bound: -

URM =
$$n(2^{1/n}-1) = 6*(2^{1/6}-1) = 0.73477$$

U ≤ URM, so the system is schedulable

2) Time Demand Analysis: -

$$w_i = e_i + \sum_{k=1}^{i-1} \left(\frac{t}{p_k}\right) e_k$$

w: worst response time

e: execution time

t: time instance

P: periodicity i: task number

critical instant = 100ms

Task	Calculations	Schedulable?
LOAD 1	w1 (10) = 5m + 0 = 5, w1 (10) = 5 < 10	YES
Receiver	$w2 (20) = 22\mu + (20/10) * 5m = 10.022,$	YES
	w2 (20) = 10.022 < 20	
Button 1	$w3 (50) = 16\mu + (50/10) * 5m + (50/20) * 22\mu = 25.071$	YES
	w3 (20) = 25.071 < 50	
Button 2	$w4 (50) = 16\mu + (50/10) * 5m + (50/20) * 22\mu + (50/50)$	YES
	$* 16\mu = 25.087$	
	w4 (50) = 25.087 < 50	
Transmitter	$w5 (100) = 14\mu + (100/10) * 5m + (100/20) * 22\mu$	YES
	$+ (100/50) * 16\mu + (100/50) * 16\mu$	
	= 50.188, w5 (100) = 50.188 < 100	
Load 2	$w5 (100) = 12m + (100/10) * 5m + (100/20) * 14\mu$	YES
	$+ (100/50) * 16\mu + (100/50) * 16\mu$	
	$+ (100/100) * 22\mu = 62.156$	
	w5 (100) = 62.156 < 100	

The System is schedulable, and the results are as expected. As the analytical method results match the simulation, then the results indicate a successful implementation.

System offline simulation

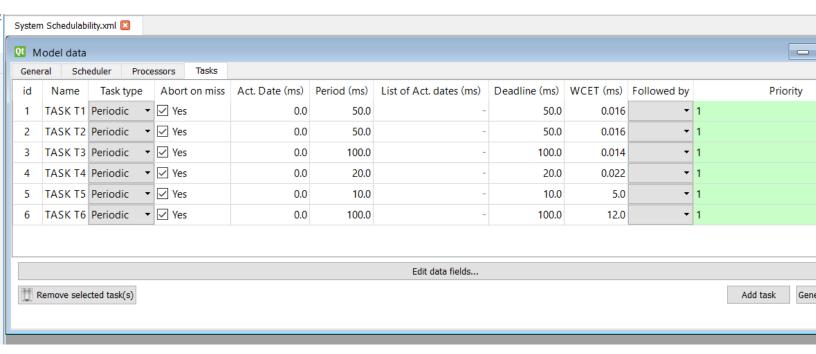


Figure 1: Task set configurations

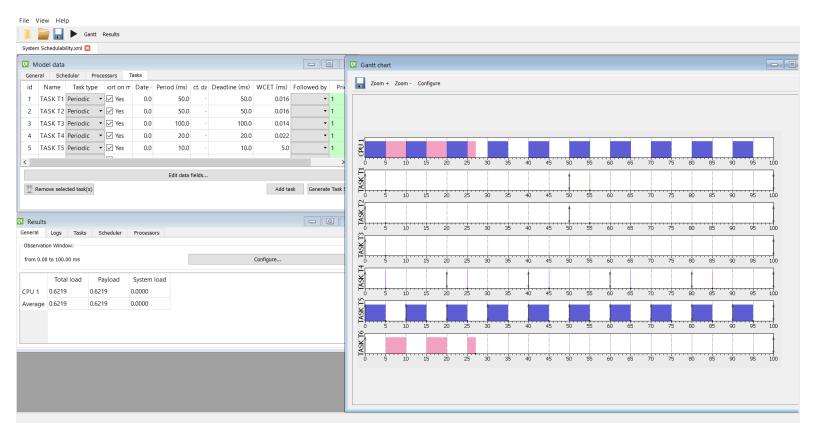


Figure 2: CPU load and system simulation using Gantt chart

Tasks Execution Plot

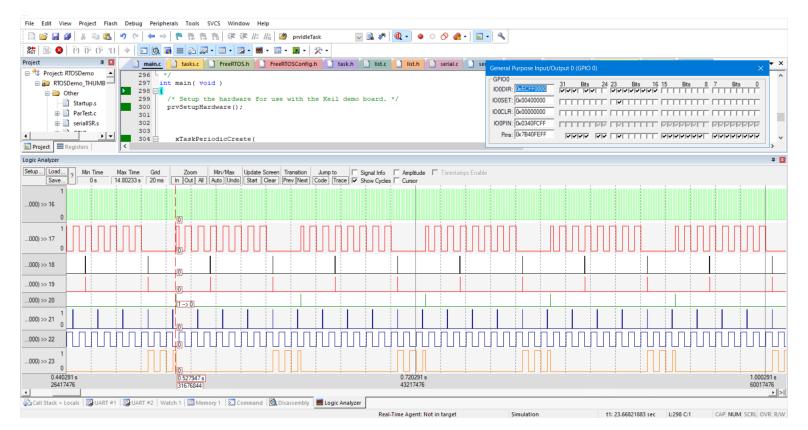


Figure 3: System real execution plot using Logic Analyzer

Task	GPIO PIN
Tick	PORTO.PIN16
Idle Task	PORTO.PIN17
Button1_Monitor	PORTO.PIN18
Button2_Monitor	PORTO.PIN19
Periodic_Transmitter	PORTO.PIN20
Uart_Receiver	PORTO.PIN21
LOAD1	PORTO.PIN22
LOAD2	PORTO.PIN23

Table 1: GPIO Pins assigned to Tasks to plot on Logic Analyzer

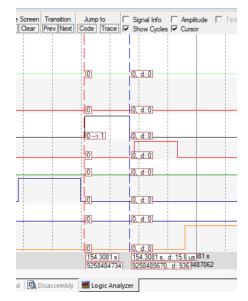


Figure 4: Task1 execution time

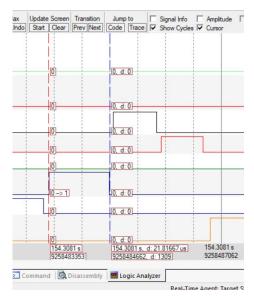


Figure 6: Task3 execution time

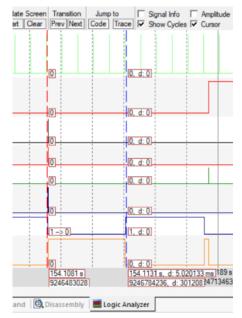


Figure 8: Task5 execution time

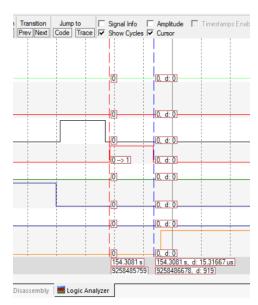


Figure 5: Task2 execution time

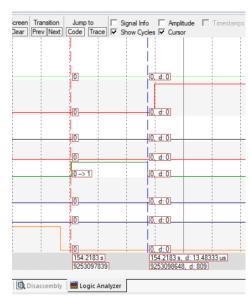


Figure 7: Task4 execution time

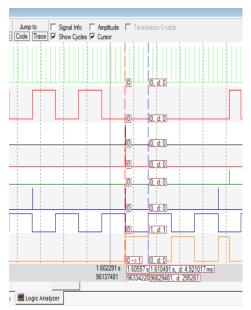


Figure 9: Task6 execution time