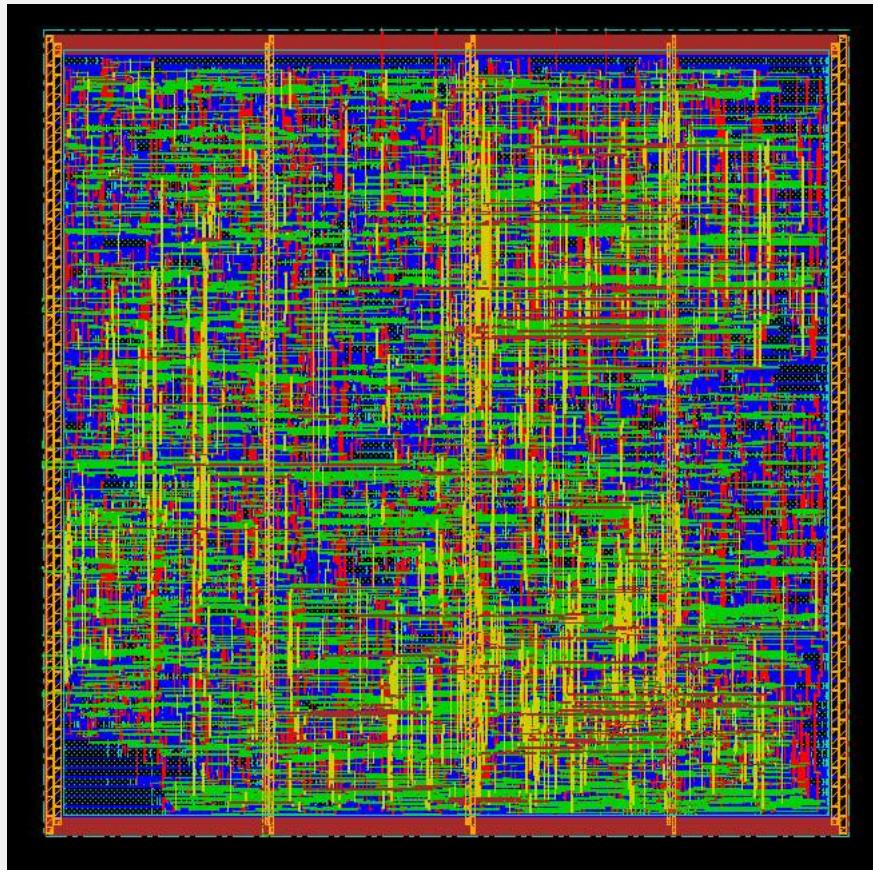


**LOW-POWER MULTI-CLOCK CONFIGURABLE PROCESSING SYSTEM  
(RTL TO GDS)**  
**&**  
**UNIVERSAL VERIFICATION METHODOLOGY  
(UVM)**

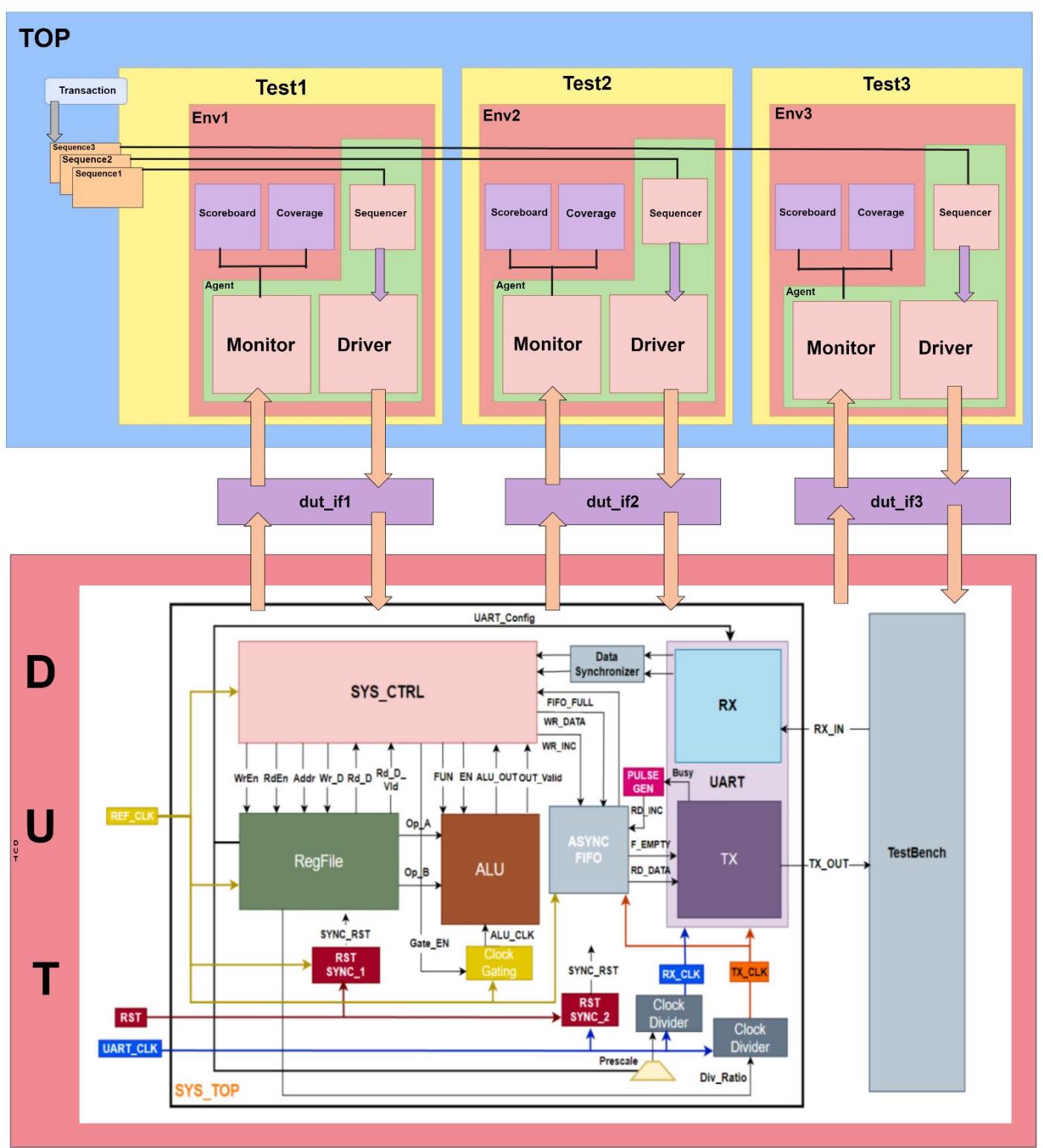
BY

**HASSAN KHALED**



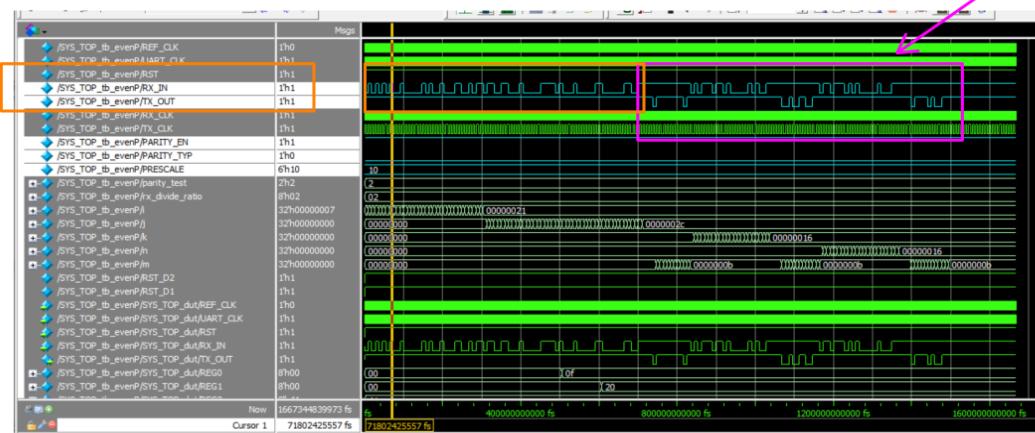
# Block Diagram

- UVM Verification Environment With Multiple Tests Connected With The full System..

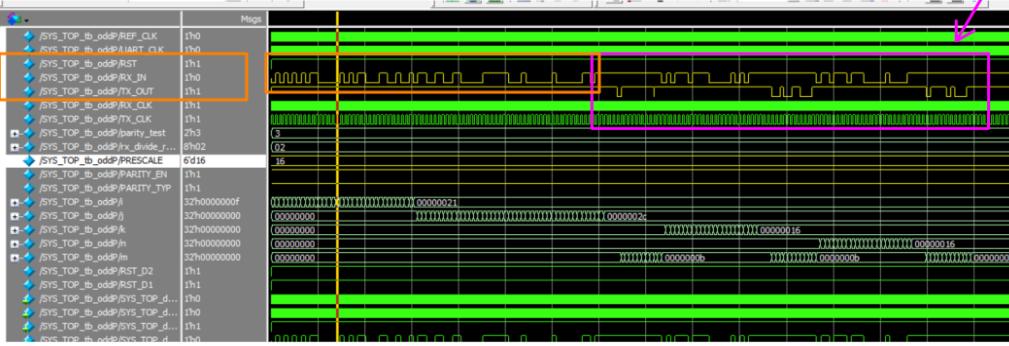


# Waveform Snippets

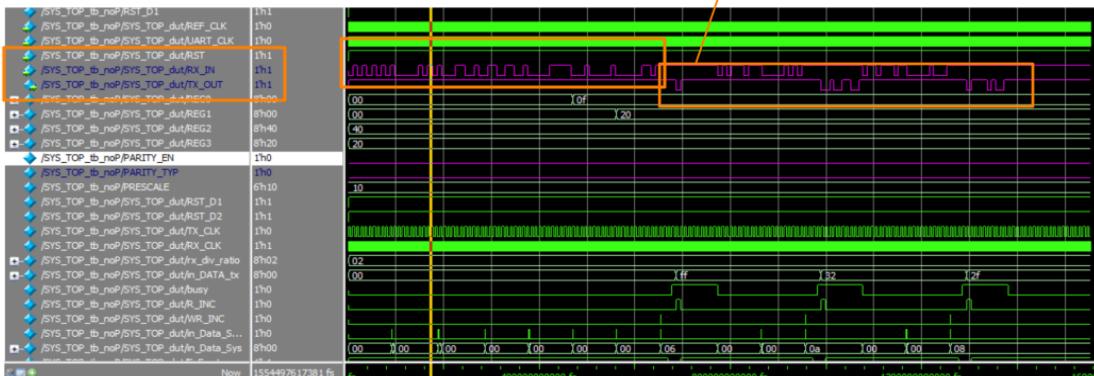
Even parity Rx to TX



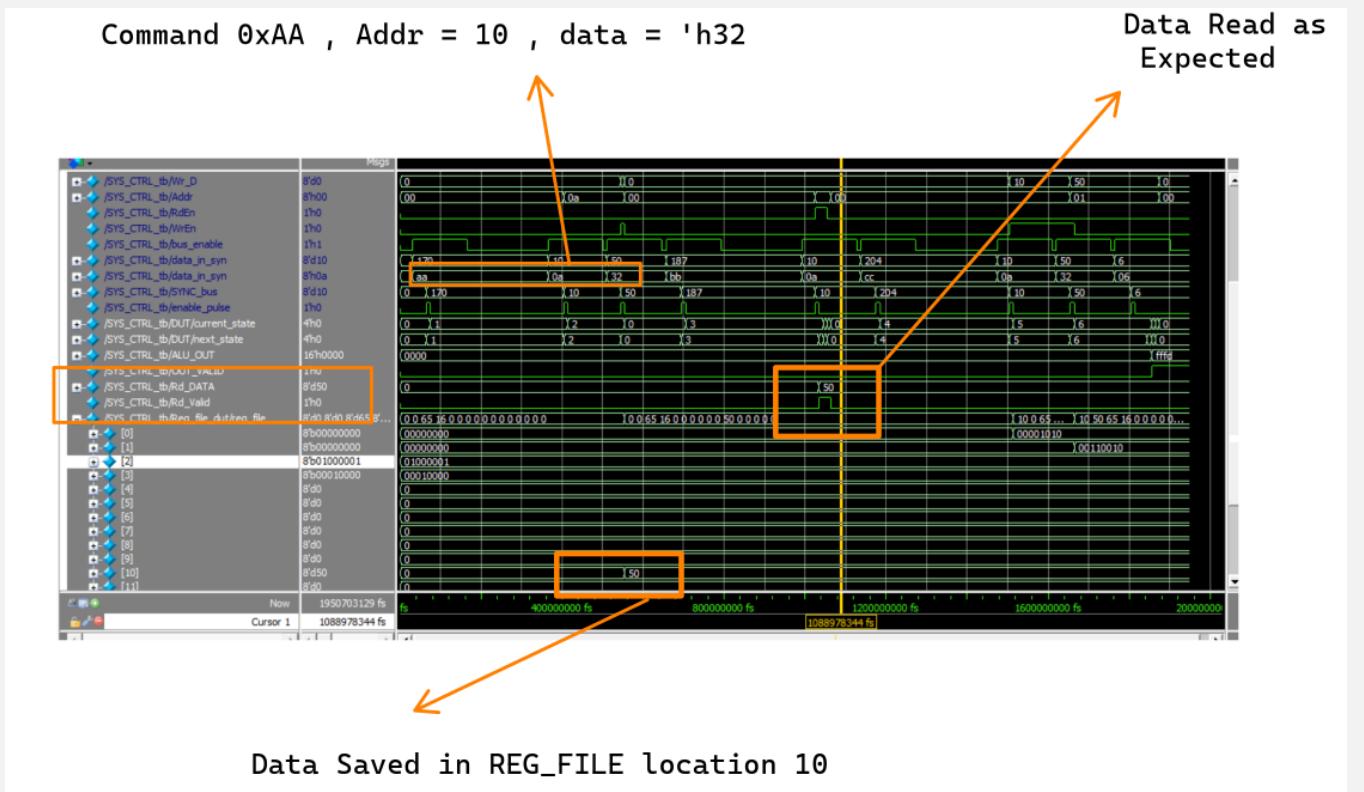
ODD parity Rx to TX



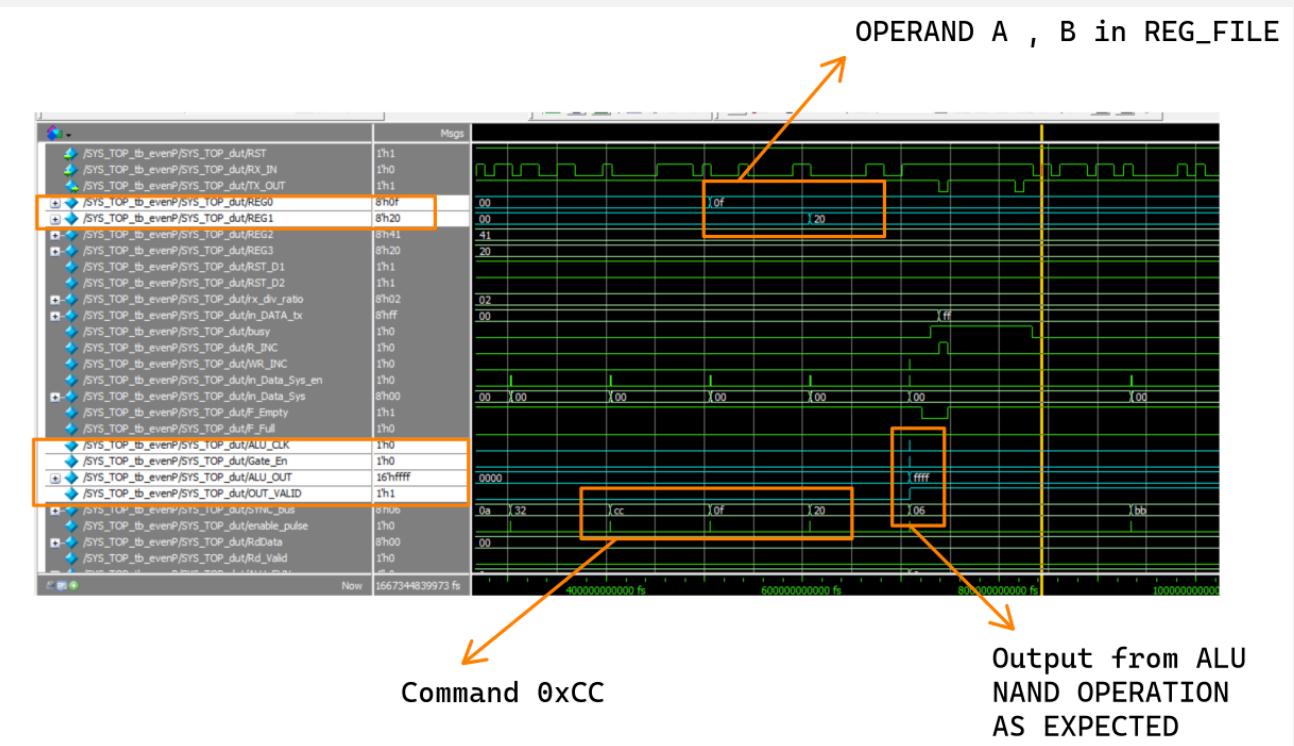
No parity Rx to TX

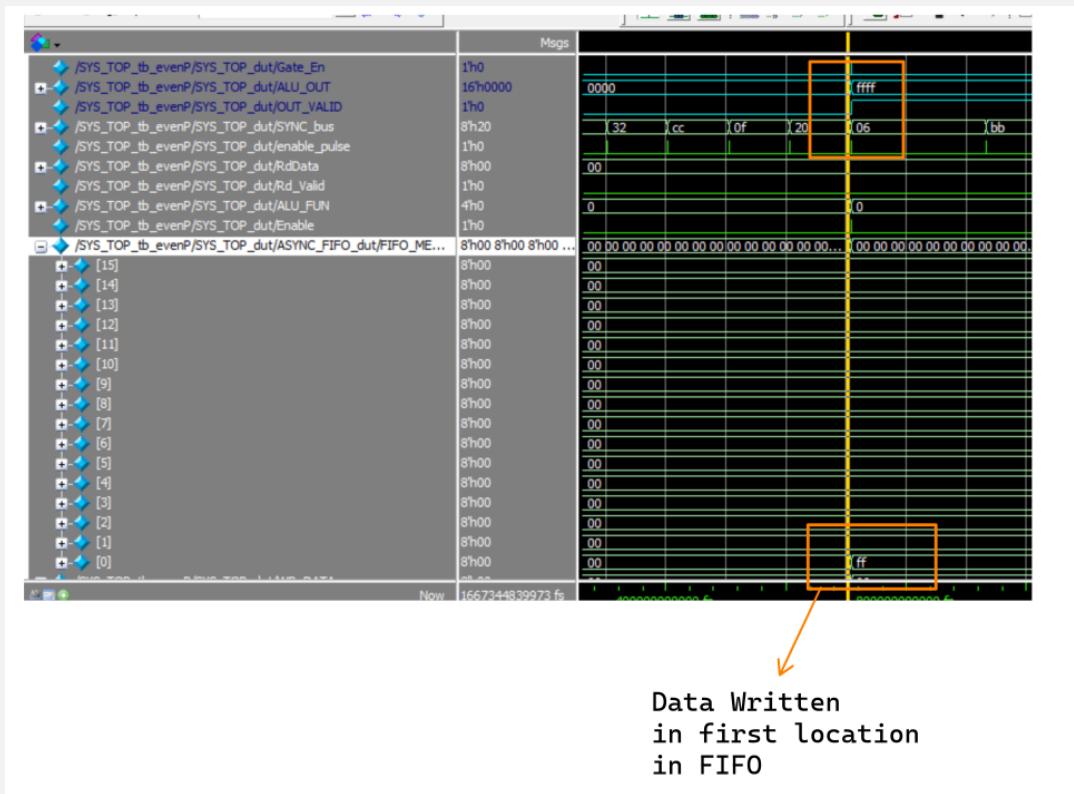


- Reg\_File Write operation , CMD = 0xAA

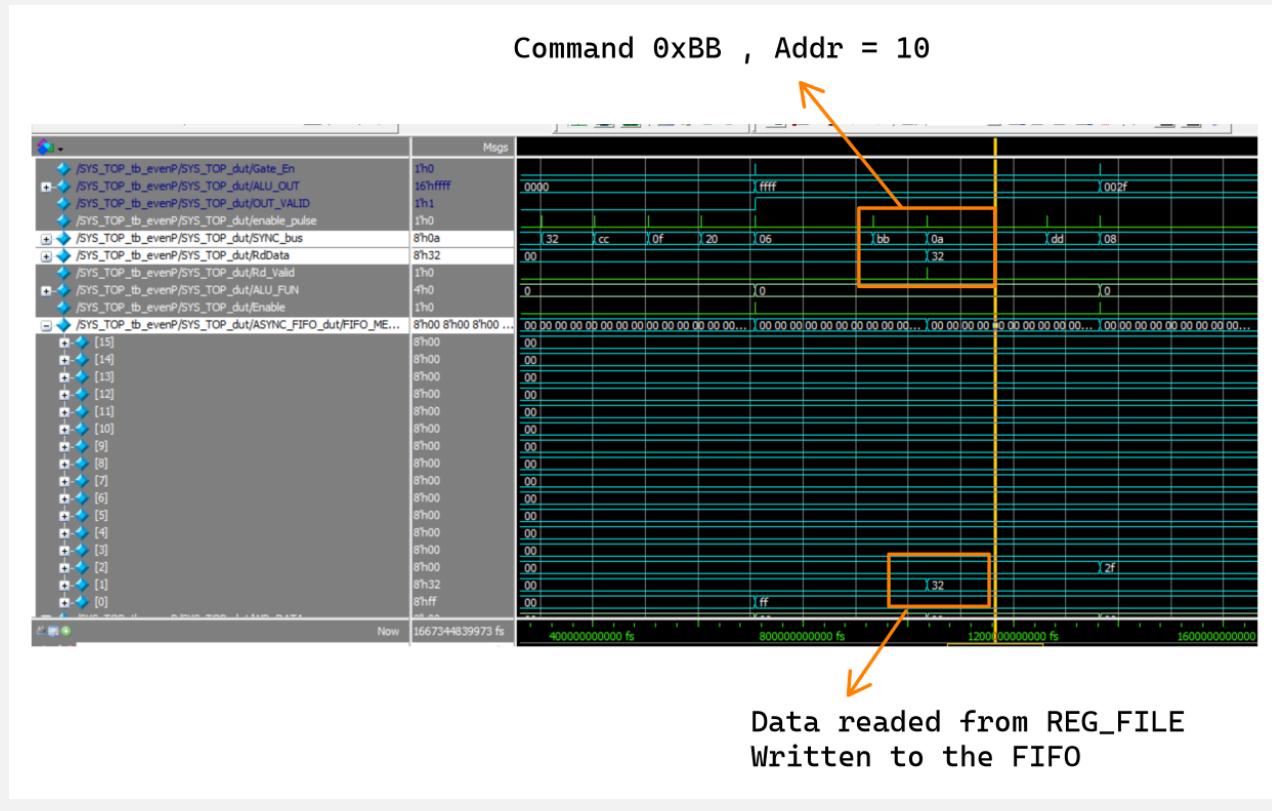


- ALU Write operation With Operands , CMD = 0xCC

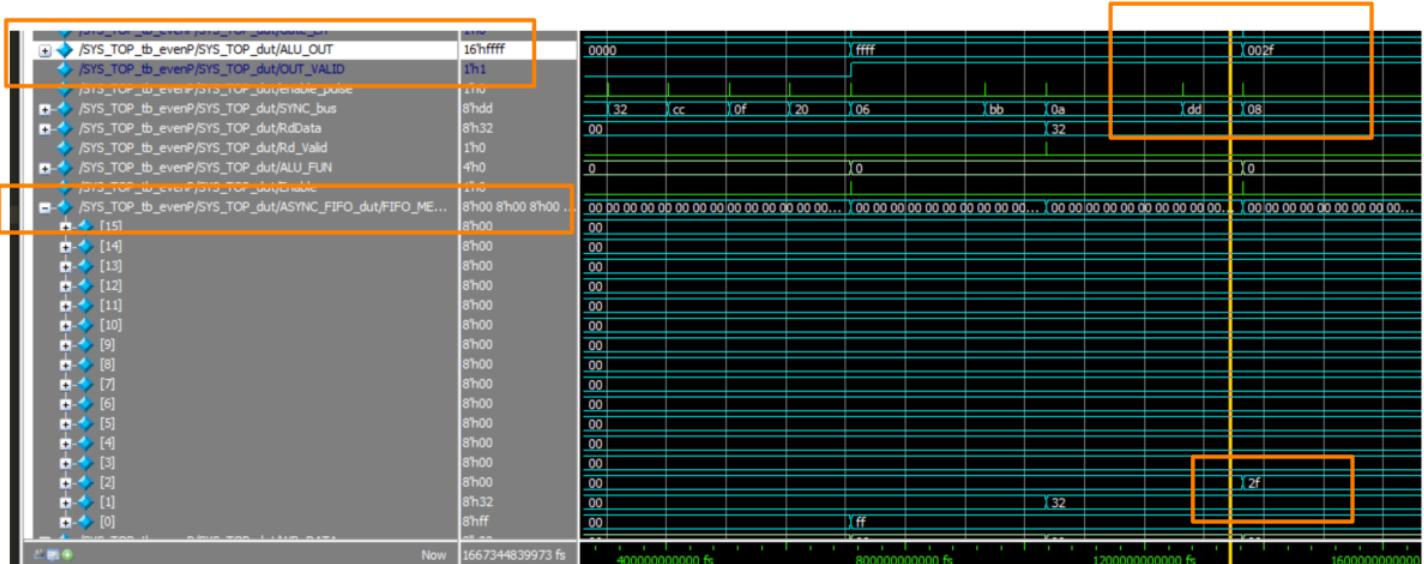




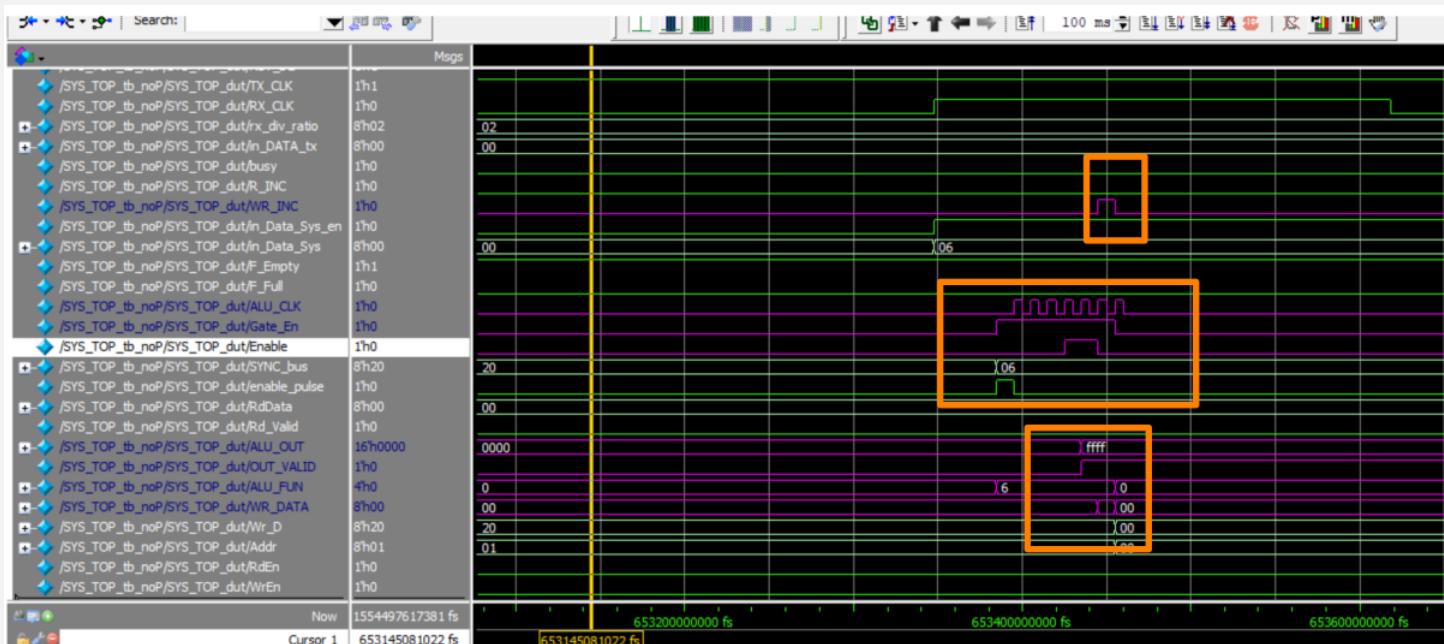
- Reg\_File Read operation , CMD = 0xBB



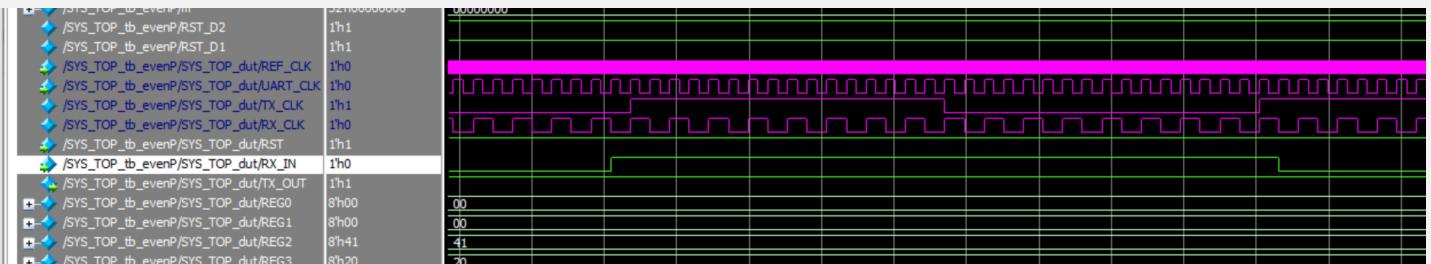
- ALU Write operation with no Operands , CMD = 0xDD



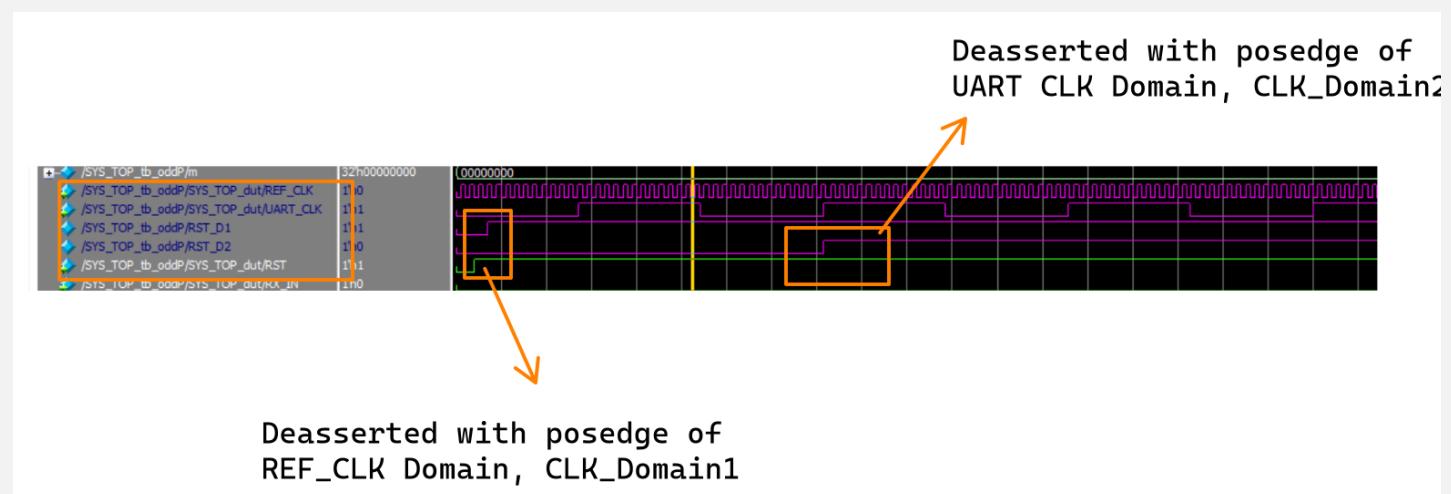
- ALU CLOCK Enabling With Clock Gating



- Prescale = 16
- Clock Divider



- RST Synchronisers for The Two Clock Domains



## Verification Report snippets

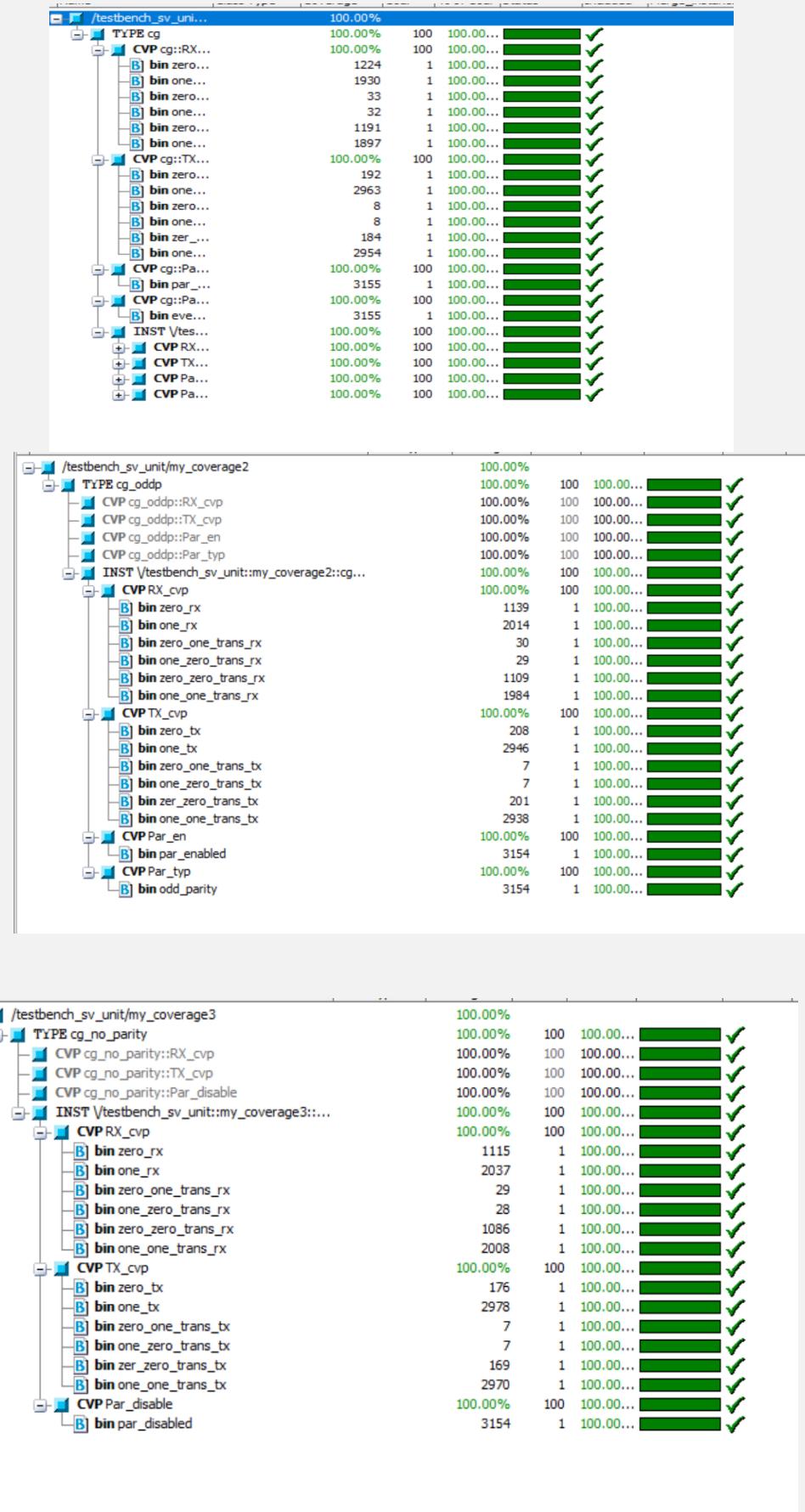
```
VM_WARNING my_test.sv(34) @ 0: uvm_test_top [] Starting TEST_1 -- PARITY_ENABLED EVEN_PARITY --
VM_INFO my_scoreboard.sv(76) @ 836264: uvm_test_top.env.scoreboard [SCOREBOARD] ----- TESTCASE PARITY ENABLE EVEN CONFIGURATION -----
VM_INFO my_scoreboard.sv(79) @ 836264: uvm_test_top.env.scoreboard [SCOREBOARD] ----- TEST_CASE SUCCEEDED , Data_EXPECTED = 5fe ,
VM_INFO my_scoreboard.sv(76) @ 1036456: uvm_test_top.env.scoreboard [SCOREBOARD] ----- TESTCASE PARITY ENABLE EVEN CONFIGURATION -----
VM_INFO my_scoreboard.sv(79) @ 1036456: uvm_test_top.env.scoreboard [SCOREBOARD] ----- TEST_CASE SUCCEEDED , Data_EXPECTED = 664 ,
VM_INFO my_scoreboard.sv(76) @ 1245352: uvm_test_top.env.scoreboard [SCOREBOARD] ----- TESTCASE PARITY ENABLE EVEN CONFIGURATION -----
VM_INFO my_scoreboard.sv(79) @ 1245352: uvm_test_top.env.scoreboard [SCOREBOARD] ----- TEST CASE SUCCEEDED Data EXPECTED = 5fe
```

```
UVM_INFO my_driver.sv(340) @ 283288: uvm_test_top.env3.agent.driver [DRIVER_1_] i = 1
UVM_INFO my_scoreboard.sv(276) @ 784040: uvm_test_top.env3.scoreboard [SCOREBOARD] ----- TESTCASE PARITY DISABLED CONFIGURATION -----
UVM_INFO my_scoreboard.sv(279) @ 784040: uvm_test_top.env3.scoreboard [SCOREBOARD] ----- TEST_CASE SUCCEEDED , Data_EXPECTED = 3fe , Data_COLLECTED = 3fe
UVM_INFO my_scoreboard.sv(276) @ 966824: uvm_test_top.env3.scoreboard [SCOREBOARD] ----- TESTCASE PARITY DISABLED CONFIGURATION -----
UVM_INFO my_scoreboard.sv(279) @ 966824: uvm_test_top.env3.scoreboard [SCOREBOARD] ----- TEST_CASE SUCCEEDED , Data_EXPECTED = 264 , Data_COLLECTED = 264
UVM_INFO my_scoreboard.sv(276) @ 1158312: uvm_test_top.env3.scoreboard [SCOREBOARD] ----- TESTCASE PARITY DISABLED CONFIGURATION -----
UVM_INFO my_scoreboard.sv(279) @ 1158312: uvm_test_top.env3.scoreboard [SCOREBOARD] ----- TEST_CASE SUCCEEDED , Data_EXPECTED = 25e , Data_COLLECTED = 25e
** Note: $stop : E:/Digital_Tem/sys/uvm_system/testbench.sv(270)
Time: 1715268 ns Traversal: 3 Iterance: /top
```

```
VM_INFO my_scoreboard.sv(178) @ 836264: uvm_test_top.env2.scoreboard [SCOREBOARD] ----- TESTCASE PARITY ENABLE ODD CONFIGURATION -----
VM_INFO my_scoreboard.sv(181) @ 836264: uvm_test_top.env2.scoreboard [SCOREBOARD] ----- TEST_CASE SUCCEEDED , Data_EXPECTED = 7fe , Data_COLLECTED = 7fe
VM_INFO my_scoreboard.sv(178) @ 1036456: uvm_test_top.env2.scoreboard [SCOREBOARD] ----- TESTCASE PARITY ENABLE ODD CONFIGURATION -----
VM_INFO my_scoreboard.sv(181) @ 1036456: uvm_test_top.env2.scoreboard [SCOREBOARD] ----- TEST_CASE SUCCEEDED , Data_EXPECTED = 464 , Data_COLLECTED = 464
VM_INFO my_scoreboard.sv(178) @ 1245352: uvm_test_top.env2.scoreboard [SCOREBOARD] ----- TESTCASE PARITY ENABLE ODD CONFIGURATION -----
VM_INFO my_scoreboard.sv(181) @ 1245352: uvm_test_top.env2.scoreboard [SCOREBOARD] ----- TEST_CASE SUCCEEDED , Data_EXPECTED = 45e , Data_COLLECTED = 45e
** Note: $stop : E:/Digital_Tem/sys/uvm_system/testbench.sv(270)
```

```
# UVM_INFO my_coverage.sv(103) @ 1249160: uvm_test_top.env.coverage [COVERAGE] THE COVERAGE PERCENTAGE = 100
# UVM_INFO my_coverage.sv(103) @ 1249704: uvm_test_top.env.coverage [COVERAGE] THE COVERAGE PERCENTAGE = 100
# UVM_INFO my_coverage.sv(103) @ 1250248: uvm_test_top.env.coverage [COVERAGE] THE COVERAGE PERCENTAGE = 100
# UVM_INFO my_coverage.sv(103) @ 1250792: uvm_test_top.env.coverage [COVERAGE] THE COVERAGE PERCENTAGE = 100
# UVM_INFO my_coverage.sv(103) @ 1251336: uvm_test_top.env.coverage [COVERAGE] THE COVERAGE PERCENTAGE = 100
# UVM_INFO my_coverage.sv(103) @ 1251880: uvm_test_top.env.coverage [COVERAGE] THE COVERAGE PERCENTAGE = 100
# UVM_INFO my_coverage.sv(103) @ 1252424: uvm_test_top.env.coverage [COVERAGE] THE COVERAGE PERCENTAGE = 100
# UVM_INFO my_coverage.sv(103) @ 1252968: uvm_test_top.env.coverage [COVERAGE] THE COVERAGE PERCENTAGE = 100
# UVM_INFO my_coverage.sv(103) @ 1253512: uvm_test_top.env.coverage [COVERAGE] THE COVERAGE PERCENTAGE = 100
# UVM_INFO my_coverage.sv(103) @ 1254056: uvm_test_top.env.coverage [COVERAGE] THE COVERAGE PERCENTAGE = 100
# UVM_INFO my_coverage.sv(103) @ 1254600: uvm_test_top.env.coverage [COVERAGE] THE COVERAGE PERCENTAGE = 100
# UVM_INFO my_coverage.sv(103) @ 1255144: uvm_test_top.env.coverage [COVERAGE] THE COVERAGE PERCENTAGE = 100
# UVM_INFO my_coverage.sv(103) @ 1255688: uvm_test_top.env.coverage [COVERAGE] THE COVERAGE PERCENTAGE = 100
# UVM_INFO my_coverage.sv(103) @ 1256232: uvm_test_top.env.coverage [COVERAGE] THE COVERAGE PERCENTAGE = 100
# UVM_INFO my_coverage.sv(103) @ 1256776: uvm_test_top.env.coverage [COVERAGE] THE COVERAGE PERCENTAGE = 100
# UVM_INFO my_coverage.sv(103) @ 1257320: uvm_test_top.env.coverage [COVERAGE] THE COVERAGE PERCENTAGE = 100
# UVM_INFO my_coverage.sv(103) @ 1257864: uvm_test_top.env.coverage [COVERAGE] THE COVERAGE PERCENTAGE = 100
# UVM_INFO my_coverage.sv(103) @ 1258408: uvm_test_top.env.coverage [COVERAGE] THE COVERAGE PERCENTAGE = 100
# UVM_INFO my_coverage.sv(103) @ 1258952: uvm_test_top.env.coverage [COVERAGE] THE COVERAGE PERCENTAGE = 100
# UVM_INFO my_coverage.sv(103) @ 1259496: uvm_test_top.env.coverage [COVERAGE] THE COVERAGE PERCENTAGE = 100
# UVM_INFO my_coverage.sv(103) @ 1260040: uvm_test_top.env.coverage [COVERAGE] THE COVERAGE PERCENTAGE = 100
```

## Functional Coverage



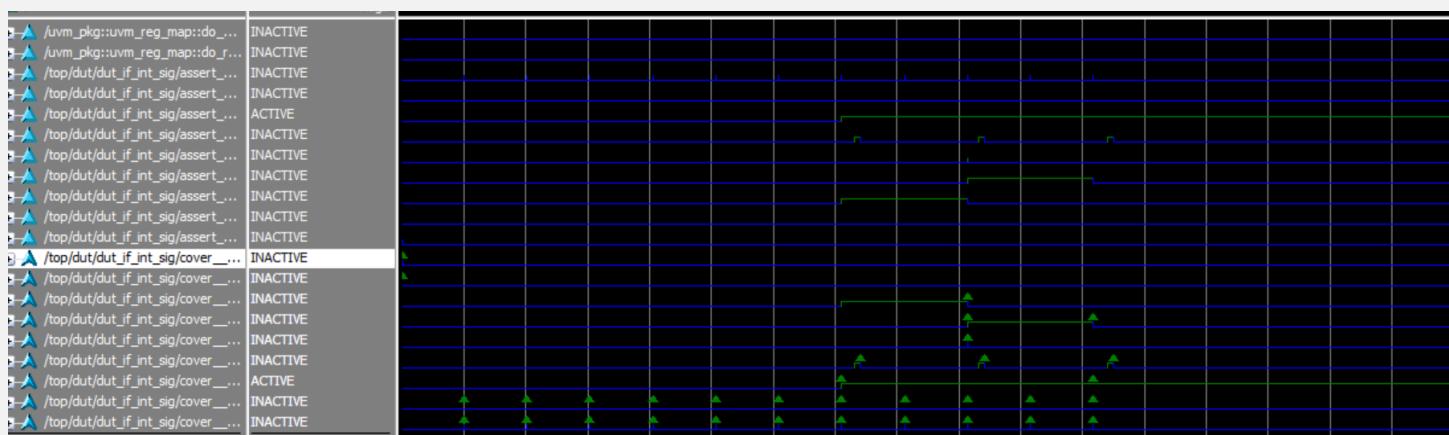
# SVA – System Verilog Assertion

**Assertions**

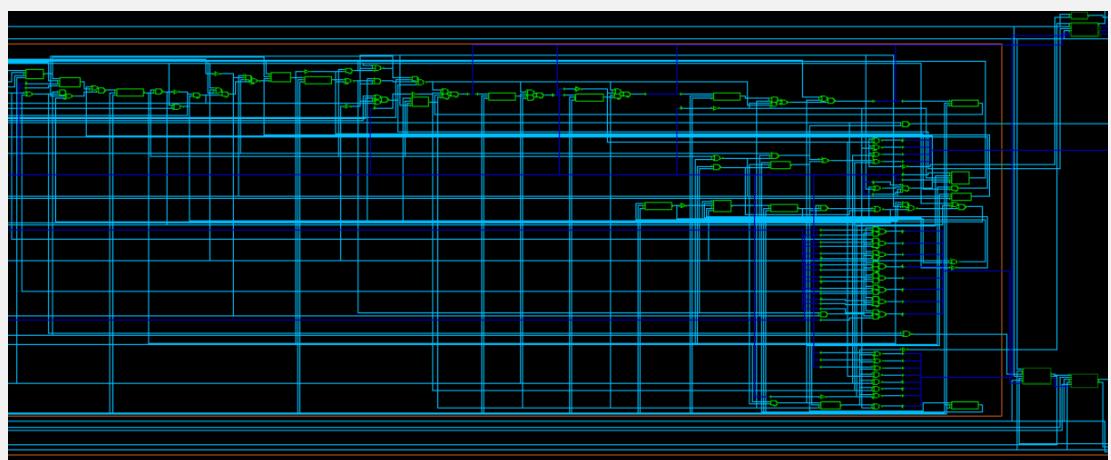
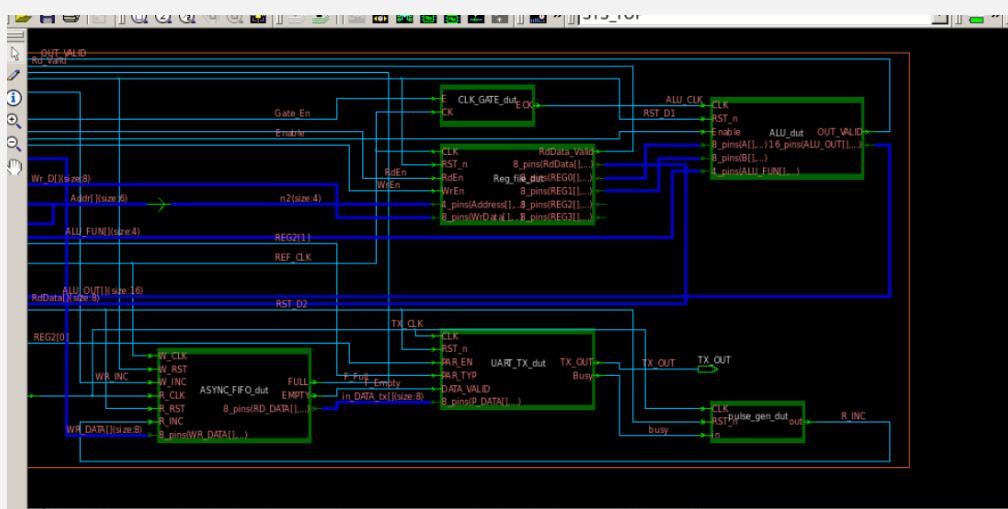
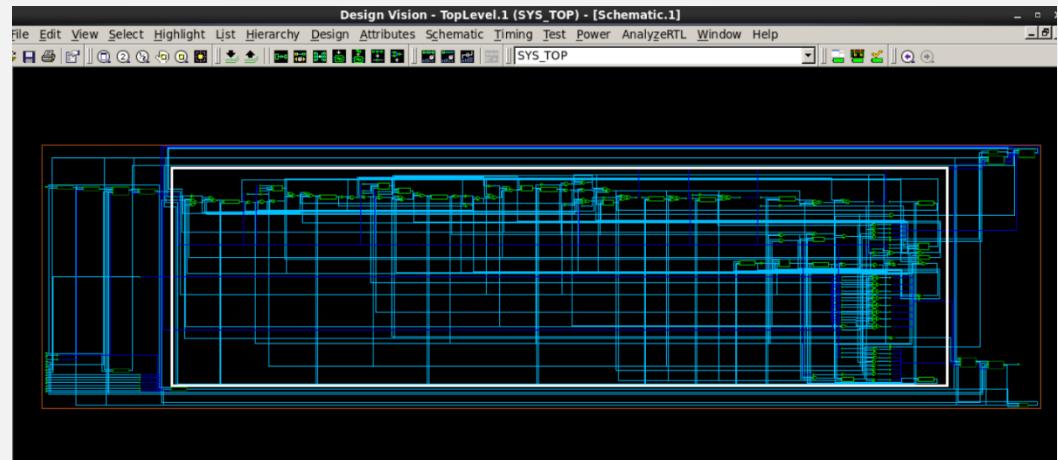
Name	Assertion Type	Language	Enable	Failure Count	Pass Count	Active Count	Memory	Peak Memory	Peak Memory Time	Cumulative Threads	ATV	Asse
/uvm_pkg::uvm_reg_map::do_write#(ublk#(215181159#1731)immed_1735	Immediate	SVA	on	0	0	-	-	-	-	0 ns	off	asse
/uvm_pkg::uvm_reg_map::do_read#(ublk#(215181159#1771)immed_1775	Immediate	SVA	on	0	0	-	-	-	-	0 ns	off	asse
/top/dut/dut_if_int_sig/assert_enable_pulse_prop	Concurrent	SVA	on	0	1	-	0B	0B	0 ns	0 off	asse	
+ P] /top/dut/dut_if_int_sig/assert_enable_pulse_prop												
+ P] /top/dut/dut_if_int_sig/assert_sync_bus_prop	Concurrent	SVA	on	0	1	-	0B	0B	0 ns	0 off	asse	
+ P] /top/dut/dut_if_int_sig/assert_alu_en_prop	Concurrent	SVA	on	0	1	-	0B	0B	0 ns	0 off	asse	
+ P] /top/dut/dut_if_int_sig/assert_alu_en_prop	Concurrent	SVA	on	0	1	-	0B	0B	0 ns	0 off	asse	
+ P] /top/dut/dut_if_int_sig/assert_rd_increment_prop	Concurrent	SVA	on	0	1	-	0B	0B	0 ns	0 off	asse	
+ P] /top/dut/dut_if_int_sig/assert_rd_increment_prop	Concurrent	SVA	on	0	1	-	0B	0B	0 ns	0 off	asse	
+ P] /top/dut/dut_if_int_sig/assert_rd_en_prop	Concurrent	SVA	on	0	1	-	0B	0B	0 ns	0 off	asse	
+ P] /top/dut/dut_if_int_sig/assert_rf_rd_en_prop	Concurrent	SVA	on	0	1	-	0B	0B	0 ns	0 off	asse	
+ P] /top/dut/dut_if_int_sig/assert_f_wr_fifo_prop	Concurrent	SVA	on	0	1	-	0B	0B	0 ns	0 off	asse	
+ P] /top/dut/dut_if_int_sig/assert_alu_wr_fifo_prop	Concurrent	SVA	on	0	1	-	0B	0B	0 ns	0 off	asse	
+ P] /top/dut/dut_if_int_sig/assert_alu_wr_fifo_prop	Concurrent	SVA	on	0	1	-	0B	0B	0 ns	0 off	asse	
+ P] /top/dut/dut_if_int_sig/assert_rst_st_sync1_assertion_prop	Concurrent	SVA	on	0	1	-	0B	0B	0 ns	0 off	asse	
+ P] /top/dut/dut_if_int_sig/assert_rst_st_sync1_deassertion_prop	Concurrent	SVA	on	0	1	-	0B	0B	0 ns	0 off	asse	
+ P] /top/dut/dut_if_int_sig/rst_st_sync1_deassertion_prop	Concurrent	SVA	on	0	1	-	0B	0B	0 ns	0 off	asse	

**Cover Directives**

Name	Language	Enabled	Log	Count	AtLeast	Limit	Weight	Cmpl %	Cmpl graph	Included	Memory	Peak Memory	Peak Memory Time	Cum
/top/dut/dut_if_int_sig/cover__rst_sync1_deassertion_prop	SVA	✓	Off	1	1	Unli...	1	100%	✓	✓	0	0	0 ns	
/top/dut/dut_if_int_sig/cover__rst_sync1_assertion_prop	SVA	✓	Off	1	1	Unli...	1	100%	✓	✓	0	0	0 ns	
/top/dut/dut_if_int_sig/cover__alu_wr_fifo_prop	SVA	✓	Off	1	1	Unli...	1	100%	✓	✓	0	0	0 ns	
/top/dut/dut_if_int_sig/cover__rf_wr_fifo_prop	SVA	✓	Off	2	1	Unli...	1	100%	✓	✓	0	0	0 ns	
/top/dut/dut_if_int_sig/cover_rf_rd_en_prop	SVA	✓	Off	2	1	Unli...	1	100%	✓	✓	0	0	0 ns	
/top/dut/dut_if_int_sig/cover_rd_increment_prop	SVA	✓	Off	3	1	Unli...	1	100%	✓	✓	0	0	0 ns	
/top/dut/dut_if_int_sig/cover_alu_en_prop	SVA	✓	Off	8	1	Unli...	1	100%	✓	✓	0	0	0 ns	
/top/dut/dut_if_int_sig/cover_sync_bus_prop	SVA	✓	Off	11	1	Unli...	1	100%	✓	✓	0	0	0 ns	
+ P] /top/dut/dut_if_int_sig/cover__enable_pulse_prop	SVA	✓	Off	11	1	Unli...	1	100%	✓	✓	0	0	0 ns	



## Synthesis Snippets



## Formal Verification – Post Synthesizing

**Formality (R) Console - Synopsys Inc.**

File Edit View Designs Run ECO Window Help

Verification Succeeded

Reference: Ref:/WORK/SYS\_TOP  
Implementation: Imp:/WORK/SYS\_TOP

✓ 0. Guid. ✓ 1. Ref. ✓ 2. Impl. 3. Setup 4. Match 5. Verify 6. Debug

Failing Points	Passing Points	Aborted Points	Unverified Points	Probe Points	Analyses	Loops	Size	+/-
1 DFF ALU_dut/ALU_OUT_reg[0]					ALU_dut/ALU_OUT_reg[0]			
2 DFF ALU_dut/ALU_OUT_reg[1]					ALU_dut/ALU_OUT_reg[1]			
3 DFF ALU_dut/ALU_OUT_reg[2]					ALU_dut/ALU_OUT_reg[2]			
4 DFF ALU_dut/ALU_OUT_reg[3]					ALU_dut/ALU_OUT_reg[3]			
5 DFF ALU_dut/ALU_OUT_reg[4]					ALU_dut/ALU_OUT_reg[4]			
6 DFF ALU_dut/ALU_OUT_reg[5]					ALU_dut/ALU_OUT_reg[5]			
7 DFF ALU_dut/ALU_OUT_reg[6]					ALU_dut/ALU_OUT_reg[6]			
8 DFF ALU_dut/ALU_OUT_reg[7]					ALU_dut/ALU_OUT_reg[7]			
9 DFF ALU_dut/OUT_VALID_reg					ALU_dut/OUT_VALID_reg			
10 DFF ASYNC_FIFO_dut/FIFO_MEMORY_dut/FIFO_MEM_reg[0][0]					ASYNC_FIFO_dut/FIFO_MEMORY_dut/FIFO_MEM_reg[0][0]			
11 DFF ASYNC_FIFO_dut/FIFO_MEMORY_dut/FIFO_MEM_reg[0][1]					ASYNC_FIFO_dut/FIFO_MEMORY_dut/FIFO_MEM_reg[0][1]			

# of Passing Points: 405      Display names:  Original  Mapped      Analyze      Analyze Selected Points

```

7 DATE . Thu Sep 21 00:19:43 2023
8 ****
9
10 405 Passing compare points:
11
12 Ref LAT      Ref:/WORK/SYS_TOP/CLK_GATE_dut/ICG_DUT
13 Impl LAT     Imp:/WORK/SYS_TOP/CLK_GATE_dut/ICG_DUT
14
15 Ref DFF     Ref:/WORK/SYS_TOP/ALU_dut/ALU_OUT_reg[0]

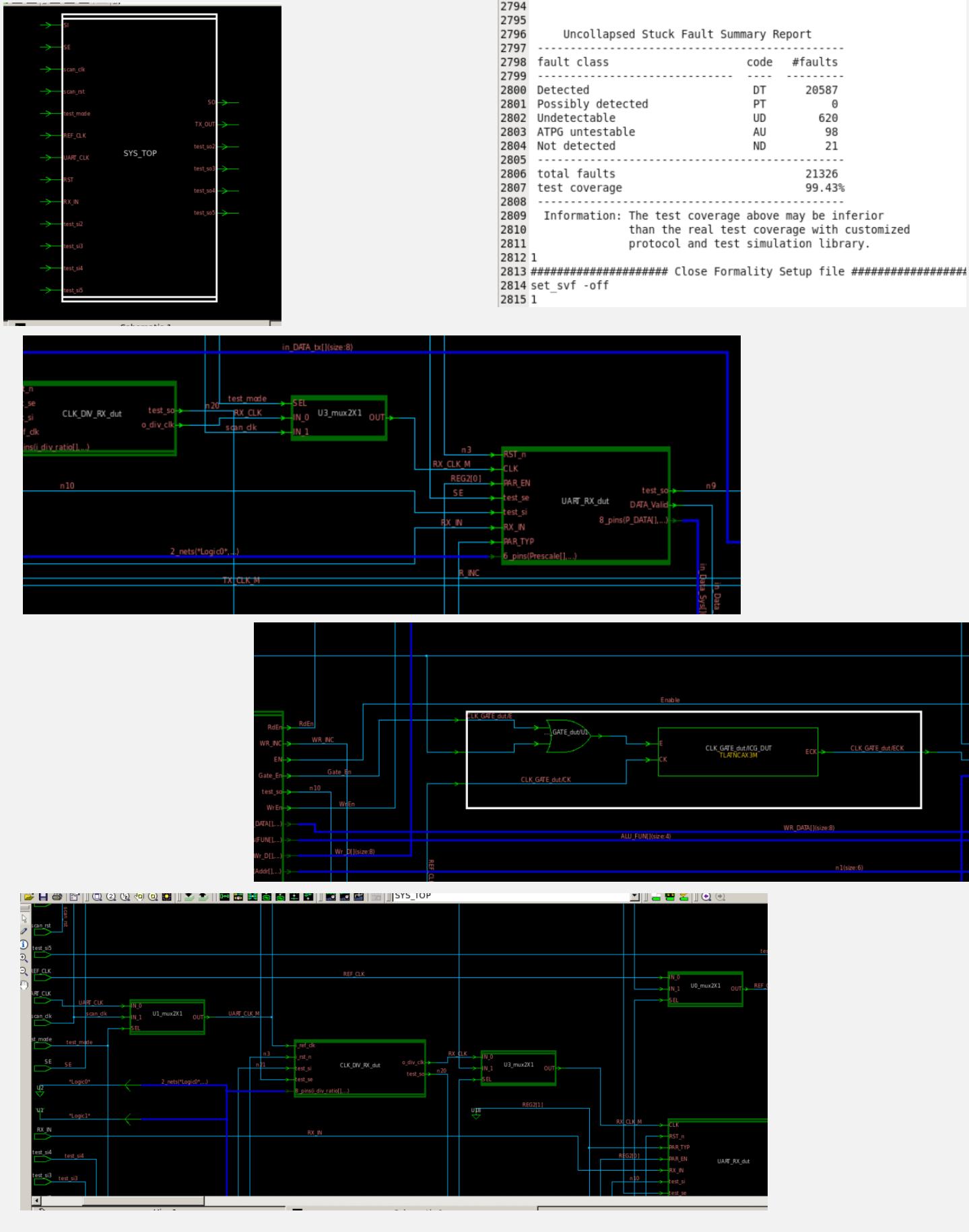
```

```

1 ****
2 Report      : failing_points
3
4 Reference   : Ref:/WORK/SYS_TOP
5 Implementation : Imp:/WORK/SYS_TOP
6 Version     : L-2016.03-SP1
7 Date        : Thu Sep 21 00:19:43 2023
8 ****
9
10 No failing compare points.
11
12 1

```

# DFT



## Formal Verification – Post DFT

Formality (R) Console - Synopsys Inc.

File Edit View Designs Run ECO Window Help

Verification Succeeded

Reference: Ref:/WORK/SYS\_TOP  
Implementation: Imp:/WORK/SYS\_TOP

✓ 0. Guid. ✓ 1. Ref. ✓ 2. Impl. 3. Setup 4. Match 5. Verify 6. Debug

Set Don't Verify Setup | Set Verify Setup | Failing Points | Aborted Points | Unverified Points | Loops |

	Object Name	Type
1	Ref:/WORK/SYS_TOP/SI	Port
2	Imp:/WORK/SYS_TOP/SI	Port
3	Ref:/WORK/SYS_TOP/SO	Port
4	Imp:/WORK/SYS_TOP/SO	Port

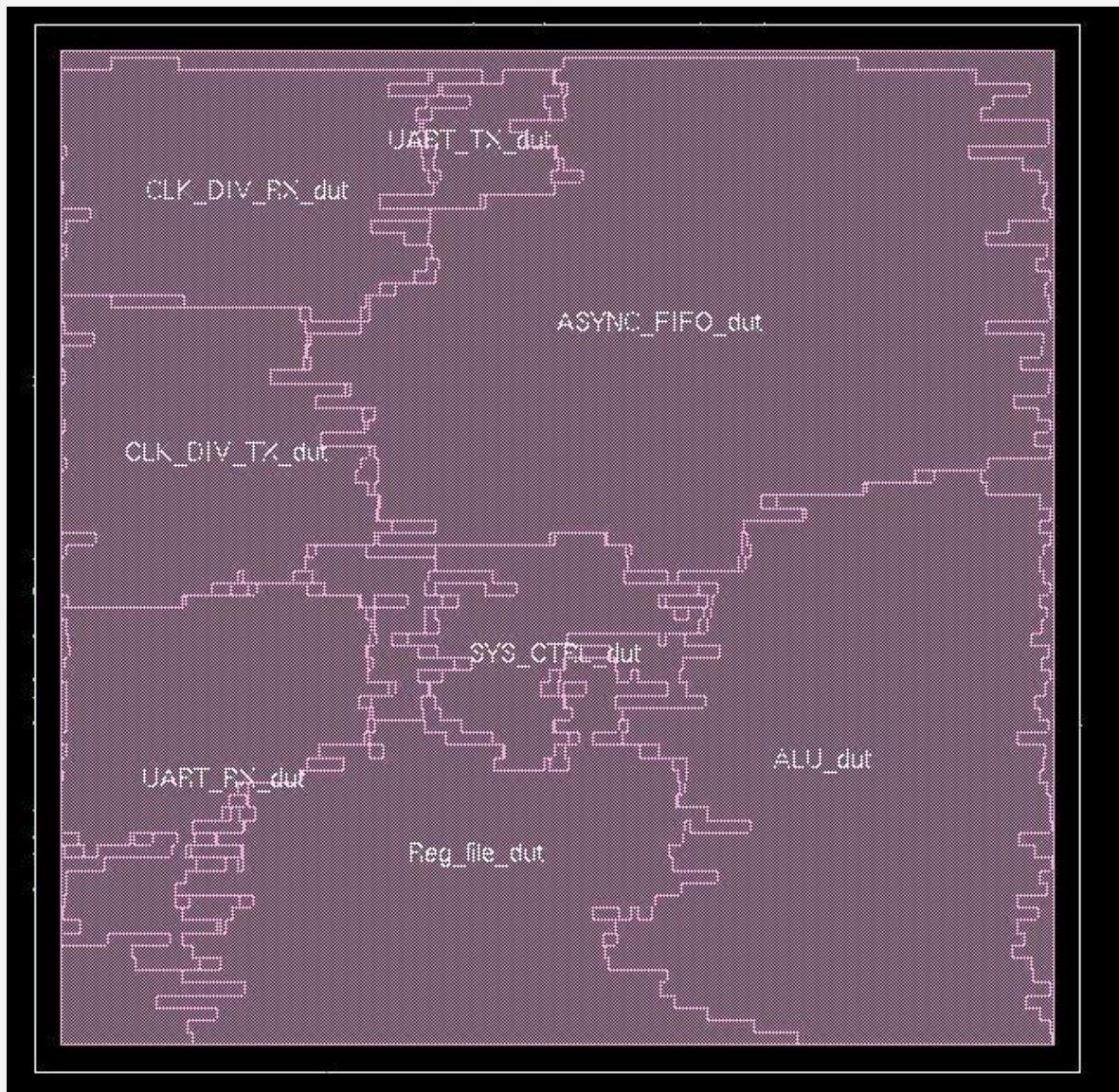
4

Filter: Continue Verify Selected Point Get Loop Data

```
399 Reference design: Ref:/WORK/SYS_TOP
400 Implementation design: Imp:/WORK/SYS_TOP
401 435 Passing compare points
402 -----
403 Matched Compare Points BBPin Loop BBNNet Cut Port DFF LAT TOTAL
404 -----
405 Passing (equivalent) 0 0 0 0 1 433 1 435
406 Failing (not equivalent) 0 0 0 0 0 0 0 0
407 Not Compared
408 Constant reg 34 0 34
409 Don't verify 0 0 0 1 0 0 1
410 Unread 0 0 0 0 0 12 0 12
411 ****
```

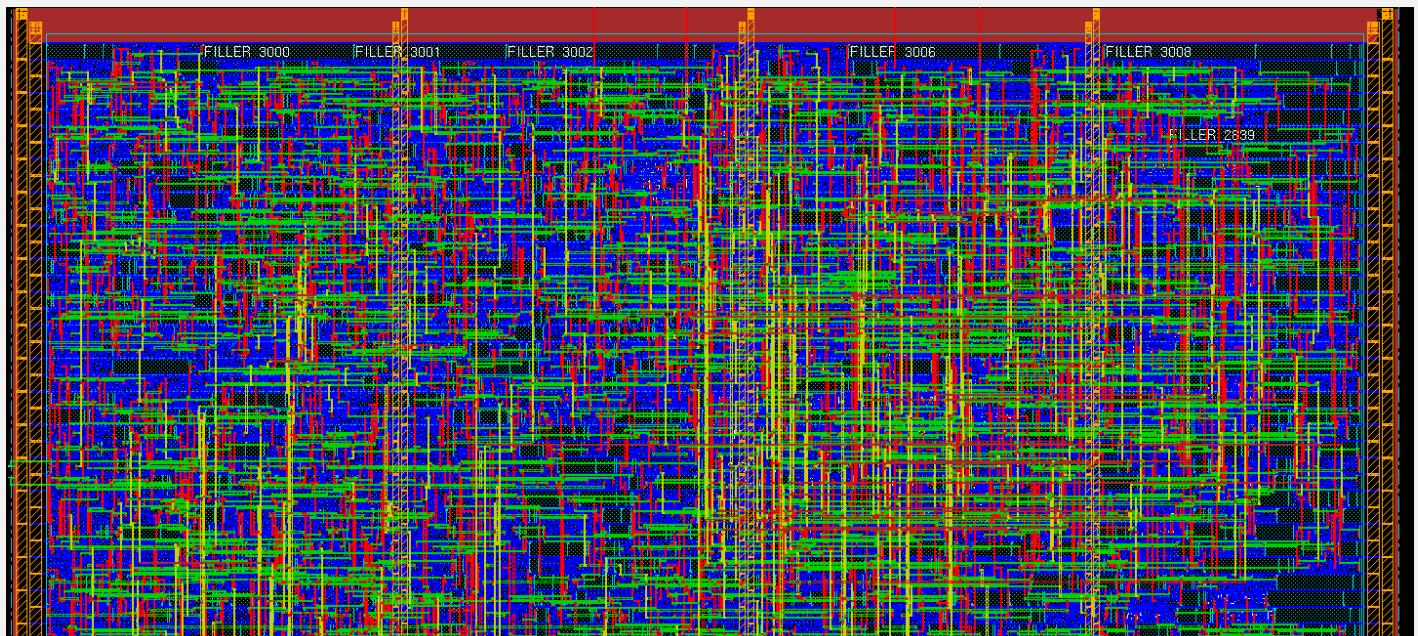
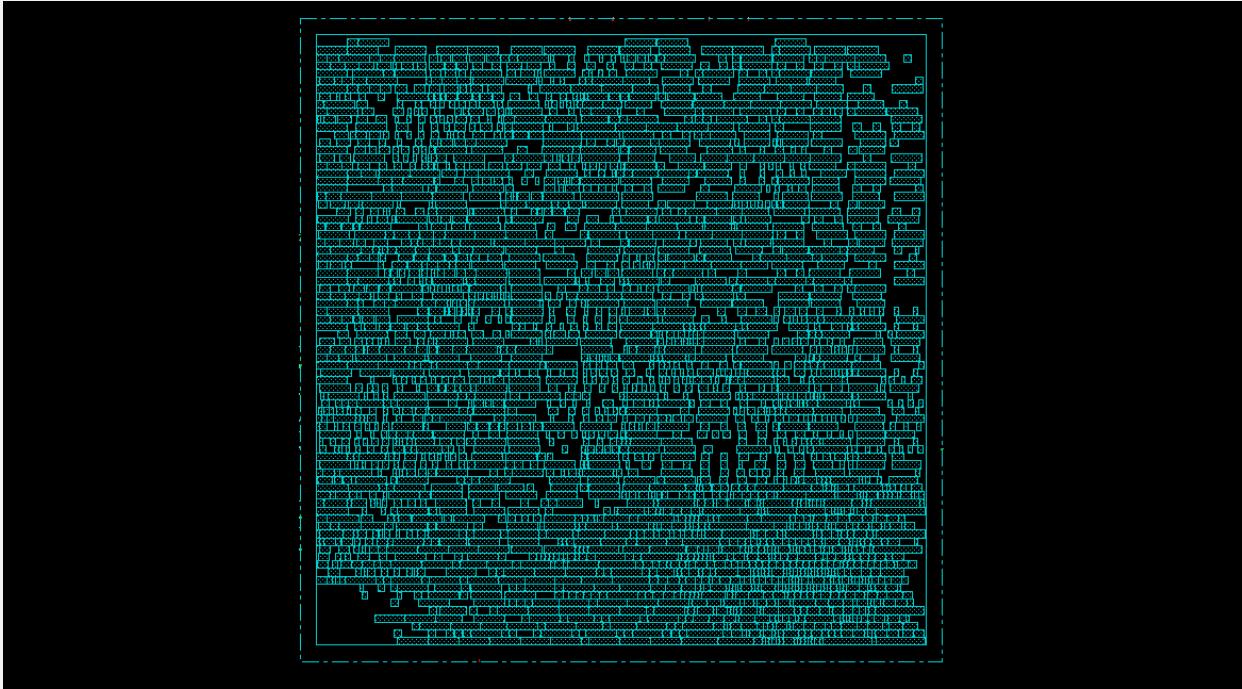
## Floor Planning

---



## Placing & Routing

---



## Final Schematic

---

