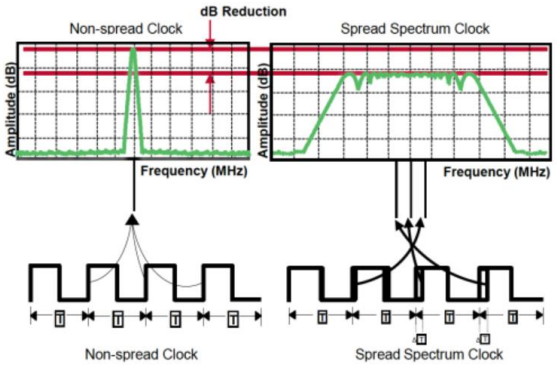
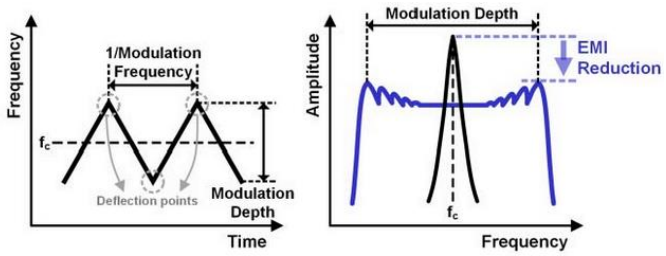
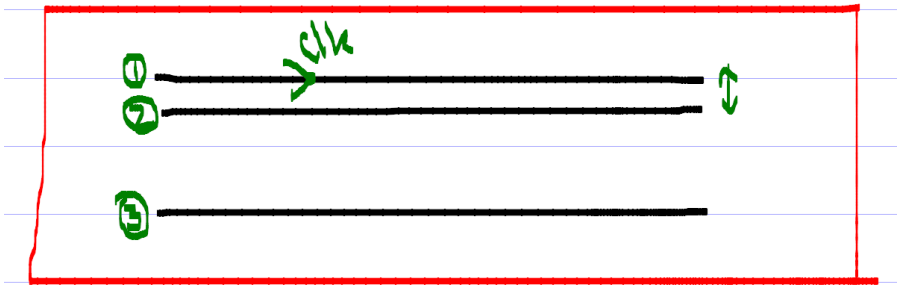
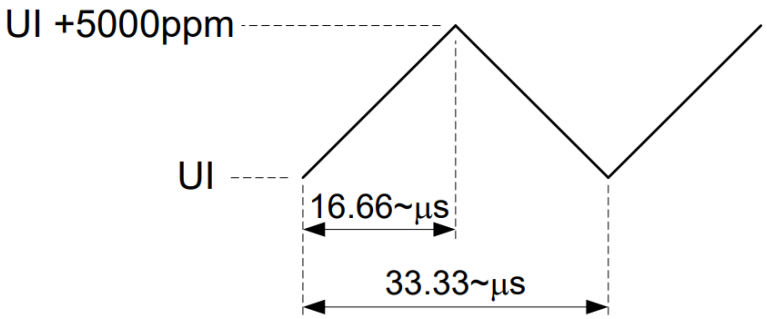
Spread Spectrum Clocking





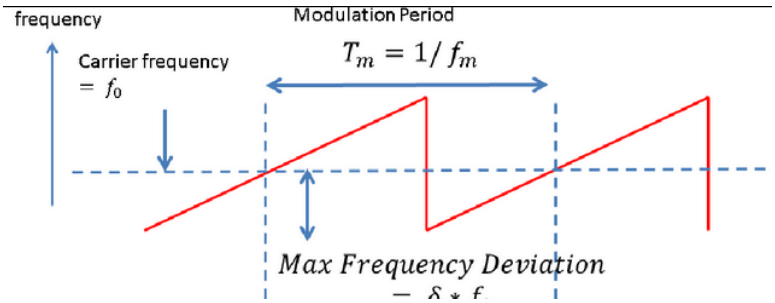
With high rate clocking the spacing among wires increases the power so as we see the central power in case of our implementation 5GHz the central maxima centralized at freq5 so we need to make spreading for the frequency in a way make the maxima under the maximum power to reduce the interference



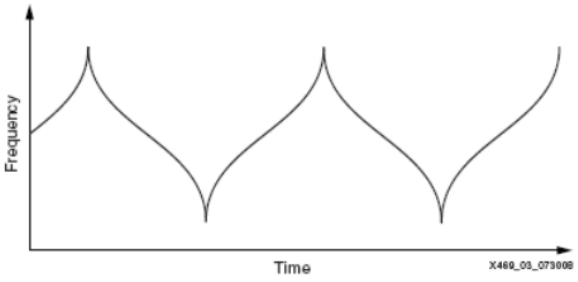


There are other profiles changing the freq like

- Assymetric trig

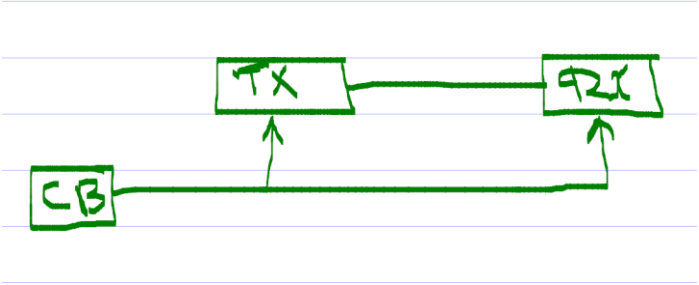


- Hershey kiss



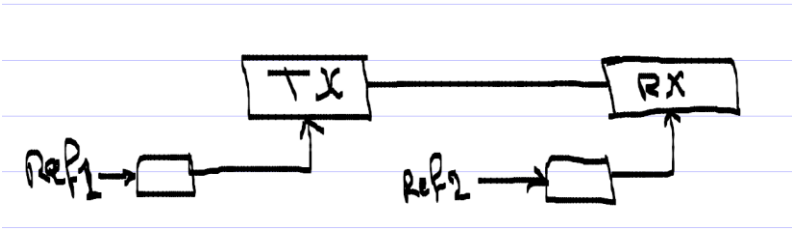
TYPES:

- **Common Clock Structure:**



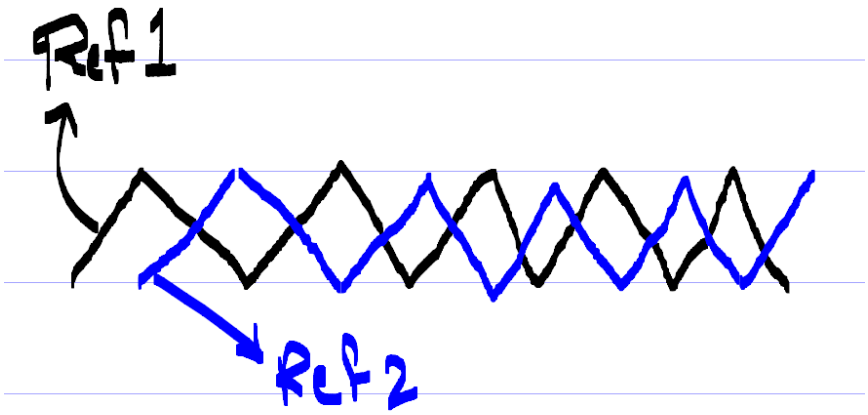
- **SRNS [Separate Ref Clock With No Spreading]:**

  Separate RF clk with PPM offset but no spreading



- **SRIS [Separate Ref Clock with independent Spreading]:**

  This case is most worse and makes more headache for the CDR to lock the data separate Ref clk with spreading for every Ref clk and this may make the next profile the increasing of the one is decreasing with the other.

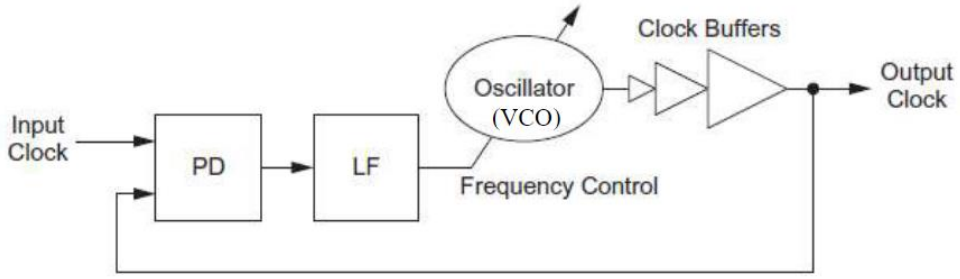


Sometimes We use VCO instead of making the Clk of CDR from PLL we make it from VCO to get rid of this problem and this is better as RX has its own oscillator, However, it has bad drifting caused by Temperature but it is still better. Its input is voltage.

PLL vs DLL

PLL

– PLL adjusts the frequency of the clock (subsequently its phase).



– DLL adjusts the delay of the clock.