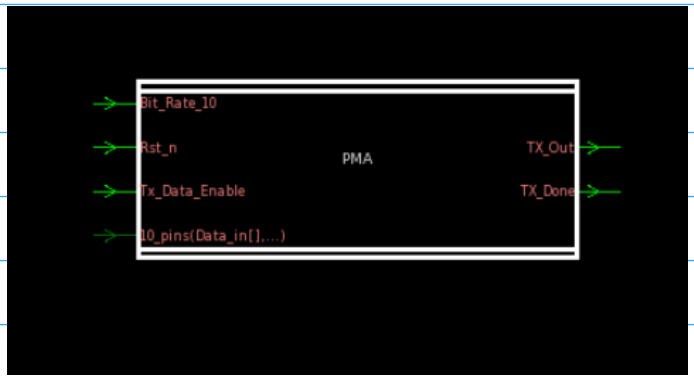
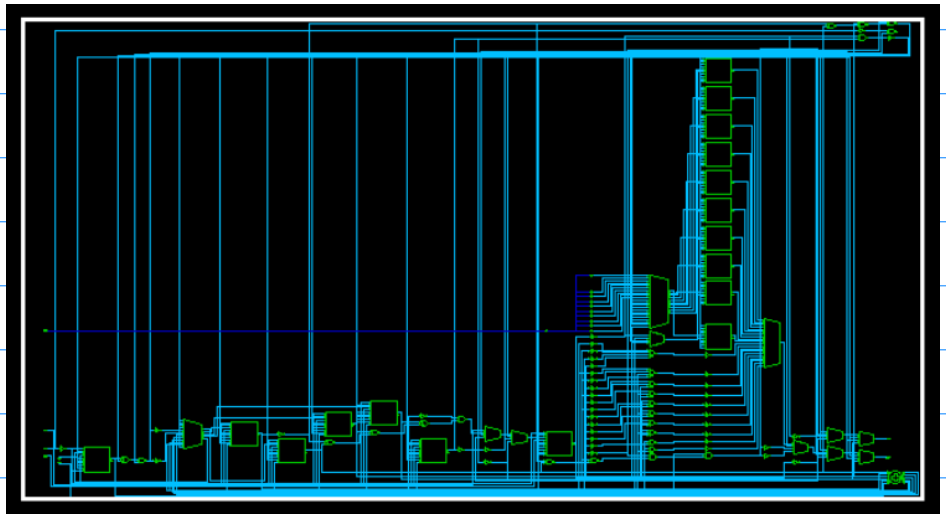
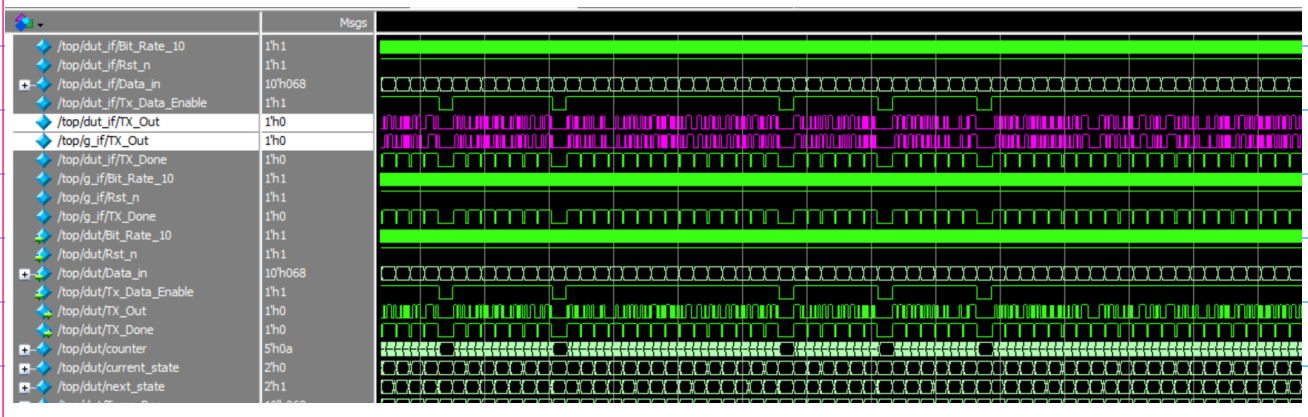

Bit_Rate_10
Rst_n
Tx_Data_Enable
10_pins(Data_in[],...)
PMA
TX_Out
TX_Done




Msgs
/top/dut_if/Bit_Rate_10 1'h1
/top/dut_if/Rst_n 1'h1
/top/dut_if/Data_in 10'h068
/top/dut_if/Tx_Data_Enable 1'h1
/top/dut_if/TX_Out 1'h0
/top/g_if/TX_Out 1'h0
/top/dut_if/TX_Done 1'h0
/top/g_if/Bit_Rate_10 1'h1
/top/g_if/Rst_n 1'h1
/top/g_if/TX_Done 1'h0
/top/dut/Bit_Rate_10 1'h1
/top/dut/Rst_n 1'h1
/top/dut/Data_in 10'h068
/top/dut/Tx_Data_Enable 1'h1
/top/dut/TX_Out 1'h0
/top/dut/TX_Done 1'h0
/top/dut/counter 5'h0a
/top/dut/current_state 2'h0
/top/dut/next_state 2'h1

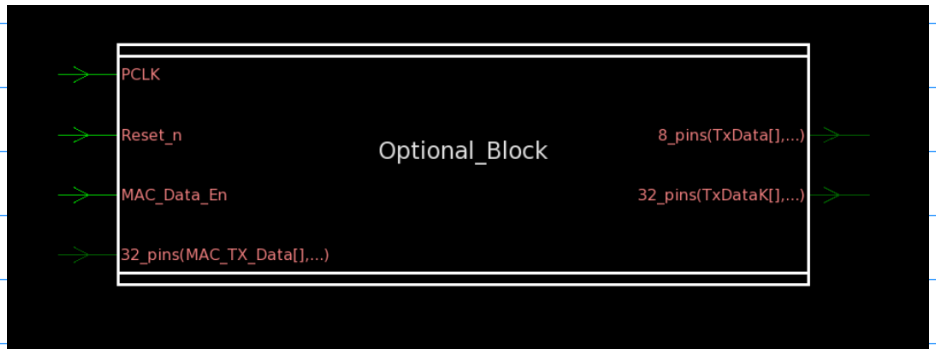
```
# UVM_WARNING E:/SerDes_GP/codes/my_test.sv(51) @ 2200450: uvm_test_top [MY_TEST] MAIN SEQ END
# UVM_INFO verilog_src/uvm-1.1d/src/base/uvm_objection.svh(1267) @ 2200450: reporter [TEST_DONE] 'run' phase is ready to proceed to the 'extract' phase
# UVM_INFO E:/SerDes_GP/codes/my_scoreboard.sv(140) @ 2200450: uvm_test_top.env.scoreboard [MY_SCOREBOARD] CORRECT_COUNT =       110018
# UVM_INFO E:/SerDes_GP/codes/my_scoreboard.sv(141) @ 2200450: uvm_test_top.env.scoreboard [MY_SCOREBOARD] ERROR_COUNT   =            4
# UVM_INFO E:/SerDes_GP/codes/my_scoreboard.sv(142) @ 2200450: uvm_test_top.env.scoreboard [MY_SCOREBOARD] CORRECT_COUNT =        55011
# UVM_INFO E:/SerDes_GP/codes/my_scoreboard.sv(143) @ 2200450: uvm_test_top.env.scoreboard [MY_SCOREBOARD] ERROR_COUNT   =            0
#
# --- UVM Report Summary ---
#
# ** Report counts by severity
# UVM_INFO :655149
# UVM_WARNING :    4
# UVM_ERROR :    0
# UVM_FATAL :    0
# ** Report counts by id
# [FAILED TEST]     4
# [MY_AGENT]     2
# [MY_COVERAGE]     1
# [MY_DRIVER] 20005
# [MY_ENV]     1
# [MY_MONITOR] 220047
# [MY_SCOREBOARD] 110028
# [MY_SCOREBOARD--] 110023
# [MY_SEQUENCE] 30004
# [MY_TEST]     5
# [Questa UVM]     2
# [RNTST]     1
# [SUCEEDED CLK_PEDIOD] 55011
# [SUCEEDED TEST] 110018
# [TEST_DONE]     1
# ** Note: $finish    : C:/questasim64_2021.1/win64/../verilog_src/uvm-1.1d/src/base/uvm_root.svh(430)
#    Time: 2200450 ns  Iteration: 62  Instance: /top
# 1
# Break in Task uvm_pkg/uvm_root::run_test at C:/questasim64_2021.1/win64/../verilog_src/uvm-1.1d/src/base/uvm_root.svh line 430
```

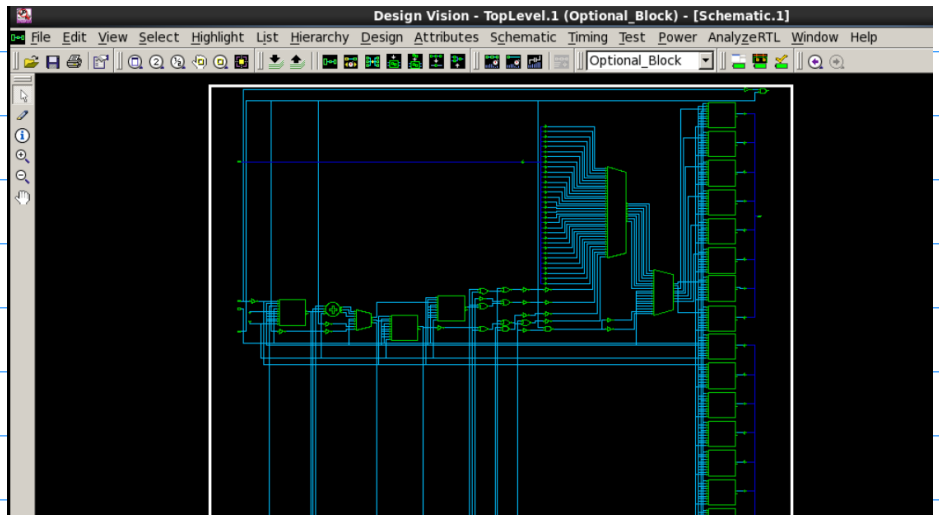
/my_coverage_pkg/my_coverage	100.00%						
TYPE cg	100.00%	100	100.00...	✓	auto(0)		
CVP cg::Data_in_cp	100.00%	100	100.00...	✓			
CVP cg::Tx_En_cp	100.00%	100	100.00...	✓			
CVP cg::Tx_out_cp	100.00%	100	100.00...	✓			
INST \/my_coverage_pkg::my_coverage:...	100.00%	100	100.00...	✓			0
CVP Data_in_cp	100.00%	100	100.00...	✓			
CVP Tx_En_cp	100.00%	100	100.00...	✓			
bin auto[0]	11209	1	100.00...	✓			
bin auto[1]	98714	1	100.00...	✓			
CVP Tx_out_cp	100.00%	100	100.00...	✓			
bin one	45022	1	100.00...	✓			
bin zero	64901	1	100.00...	✓			
bin one_zero	24670	1	100.00...	✓			
bin zero_one	24670	1	100.00...	✓			
TYPE cg_rst	100.00%	100	100.00...	✓	auto(0)		
CVP cg_rst::RST_cp	100.00%	100	100.00...	✓			
INST \/my_coverage_pkg::my_coverage:...	100.00%	100	100.00...	✓			0
CVP RST_cp	100.00%	100	100.00...	✓			
bin rst_one	109923	1	100.00...	✓			
bin rst_zero	99	1	100.00...	✓			
bin rst_one_zero	8	1	100.00...	✓			
bin rst_zero_one	9	1	100.00...	✓			

```
================================================================================
=== File: PMA.v
================================================================================
    Enabled Coverage              Bins      Hits    Misses  Coverage
    ----------------              ----      ----    ------  --------
    Branches                        18        17         1    94.44%
    Conditions                       4         3         1    75.00%
    FSM States                       2         2         0   100.00%
    FSM Transitions                  2         2         0   100.00%
    Statements                      24        22         2    91.66%
    Toggles                         68        62         6    91.17%

================================================================================
=== File: golden_model.sv
================================================================================
```

```
TOTAL COVERGROUP COVERAGE: 100.00%  COVERGROUP TYPES: 2
```

Optional Block



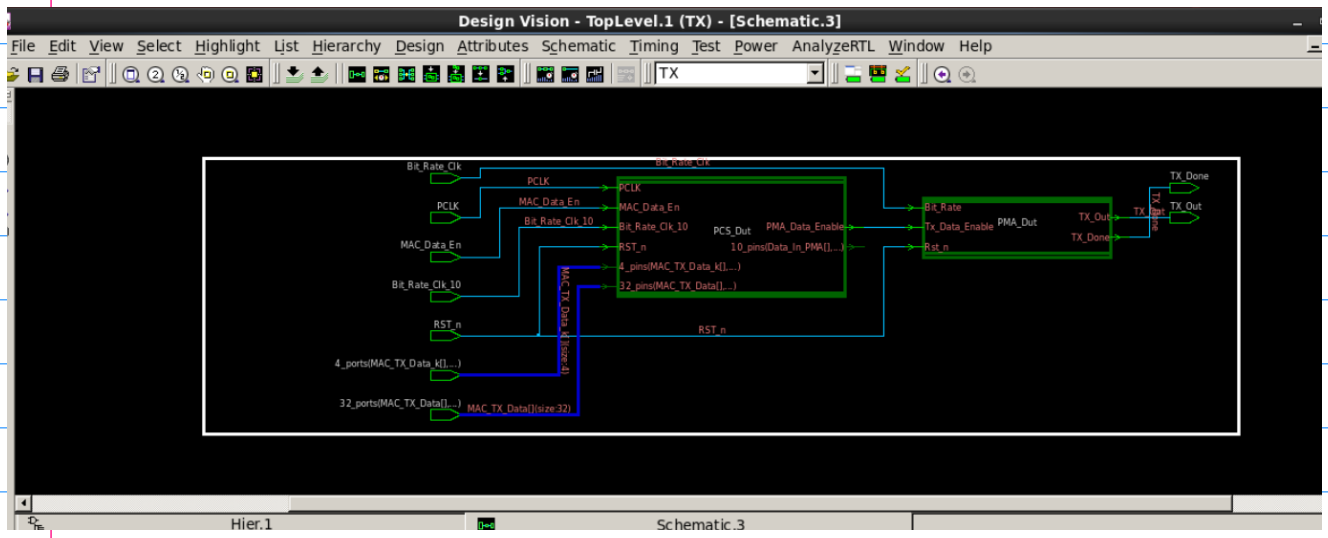


RTL

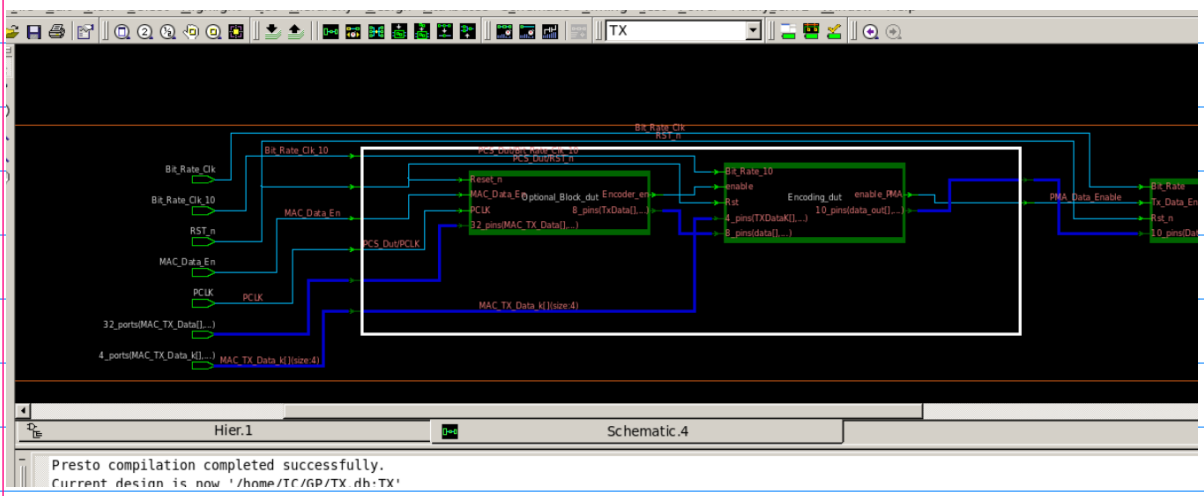
```
module Optional_Block #(parameter DataBusWidth = 'd32)
(
  input                                 PCLK                ,
  input                                 Reset_n             ,
  input       [31 : 0 ]                 MAC_TX_Data         ,
  input                                 MAC_Data_En         ,
  output  reg [7  : 0 ]                 TxData              ,
  output  reg [31 : 0 ]                 TxDataK

);

reg [7:0] Temp_Data                     ;
reg [2:0] Counter                       ;



always @(*) begin

if     (Counter == 0) Temp_Data = MAC_TX_Data [7  :0 ] ;
else if(Counter == 1) Temp_Data = MAC_TX_Data [15 :8 ] ;
else if(Counter == 2) Temp_Data = MAC_TX_Data [23 :16] ;
else                  Temp_Data = MAC_TX_Data [31 :24] ;

end




always @(posedge PCLK or negedge Reset_n)
begin

    if(!Reset_n) begin
    TxData   <= 0         ;
    TxDataK  <= 0         ;
    end

    else if (MAC_Data_En & Counter < (DataBusWidth/8)) begin
     TxDataK <= 0         ;
     TxData  <= Temp_Data ;
    end


    else begin
     TxDataK <= 0         ;
```

```
    if(!Reset_n) begin
    TxData   <= 0         ;
    TxDataK  <= 0         ;
    end

    else if (MAC_Data_En & Counter < (DataBusWidth/8)) begin
     TxDataK <= 0         ;
     TxData  <= Temp_Data ;
    end


    else begin
     TxDataK <= 0         ;
     TxData  <= 0         ;
    end

end




always @(posedge PCLK or negedge Reset_n) begin
    if (!Reset_n) begin
     Counter <= 0             ;
    end

    else if (MAC_Data_En && DataBusWidth) begin
     Counter <= Counter + 1    ;
    end

    else
     Counter <= 0             ;
end




endmodule
```

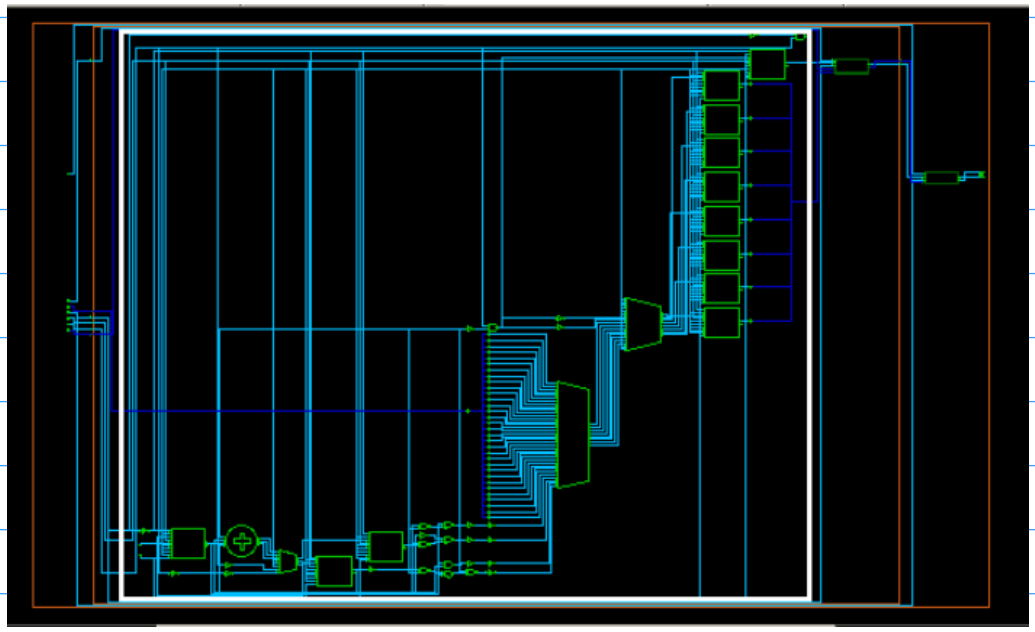

PCLK
RST_n
Bit_Rate_Clk_10
MAC_Data_En
Bit_Rate_Clk
32_ports(MAC_TX_Data[],...)
4_ports(MAC_TX_Data_k[],...)
TX
TX_Out
TX_Done


Design Vision - TopLevel.1 (TX) - [Schematic.3]
File Edit View Select Highlight List Hierarchy Design Attributes Schematic Timing Test Power AnalyzeRTL Window Help
TX
Hier.1
Schematic.3

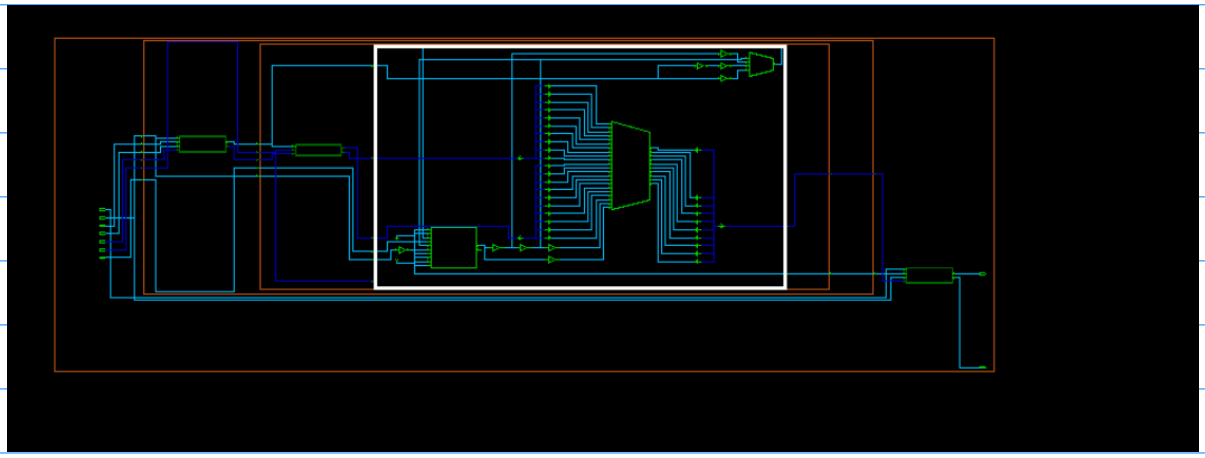
PCS


TX
Hier.1
Schematic.4
Presto compilation completed successfully.
Current design is now '/home/IC/GP/TX.db:TX'

Optional Block



Encoder FSM



PMA