Ain Shams University,
Faculty of Engineering,
Computer and Systems Engineering



Digital Design and Verification For SerDes System

Team members

Hassan Khaled Hassan
Abdelmagid Mohamed Abdelmagid
Alaa Salah Abd-Elfattah

Under Supervision of:

Dr. Ahmed M. Zaki

Associate professor, Ain-shams University, Egypt

Sponsored By:



USB-PHY

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 - 1. Gasket
 - a. Specs.
 - b. RTL
 - c. Schematic
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b. RX

i. PCS

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2. Comma Detection

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3. Decoder

- a. Specs.
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- c. Schematic
- d. Report Area, Power
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- f. Gasket UVM Environment
- g. Snippets Wave Form
- h. Coverage Reports [Functional & Code]

4. RX Status

- a. Specs.
- b. RTL
- c. Schematic
- d. Report Area, Power
- e. Test Plan
- f. Gasket UVM Environment
- g. Snippets Wave Form
- h. Coverage Reports [Functional & Code]

5. Gasket

- a. Specs.
- b. RTL
- c. Schematic
- d. Report Area, Power
- e. Test Plan
- f. Gasket UVM Environment
- g. Snippets Wave Form
- h. Coverage Reports [Functional & Code]

ii. PMA

- 1. CDR
 - a. Specs.
 - b. RTL
 - c. Schematic
 - d. Report Area, Power
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 - f. Gasket UVM Environment
 - g. Snippets Wave Form
 - h. Coverage Reports [Functional & Code]
- 2. Serial To Parallel
 - a. Specs.
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Introduction

A Serializer/Deserializer (SerDes) is a pair of functional blocks commonly used in high-speed communications to compensate for limited input/output. These blocks convert data between serial data and parallel interfaces in each direction. The term "SerDes" generically refers to interfaces used in various technologies and applications. The primary use of SerDes is to provide data transmission over a single line or a differential pair to minimize the number of I/O pins and interconnects. The basic SerDes function is made up of two functional blocks: the Parallel In Serial Out (PISO) block (aka Parallel-to-Serial converter) and the Serial In Parallel Out (SIPO) block (aka Serial-to-Parallel converter). There are 4 different SerDes architectures: (1) Parallel clock SerDes, (2) Embedded clock SerDes, (3) 8b/10b SerDes, (4) Bit interleaved SerDes.