

Report Generated by Test Manager

Title: Testing_Report
Author: Hassan Mohamed
Date: 15-Feb-2025 14:35:45

Summary

Name

Outcome

Duration
(Seconds)

 [TC_1](#)



17.11

TC_1


Test Result Information

Result Type: Test Case Result
Parent: None
Start Time: 15-Feb-2025 14:32:52
End Time: 15-Feb-2025 14:33:09
Outcome: **Passed**















Test Case Information

Name: TC_1
Type: Baseline Test

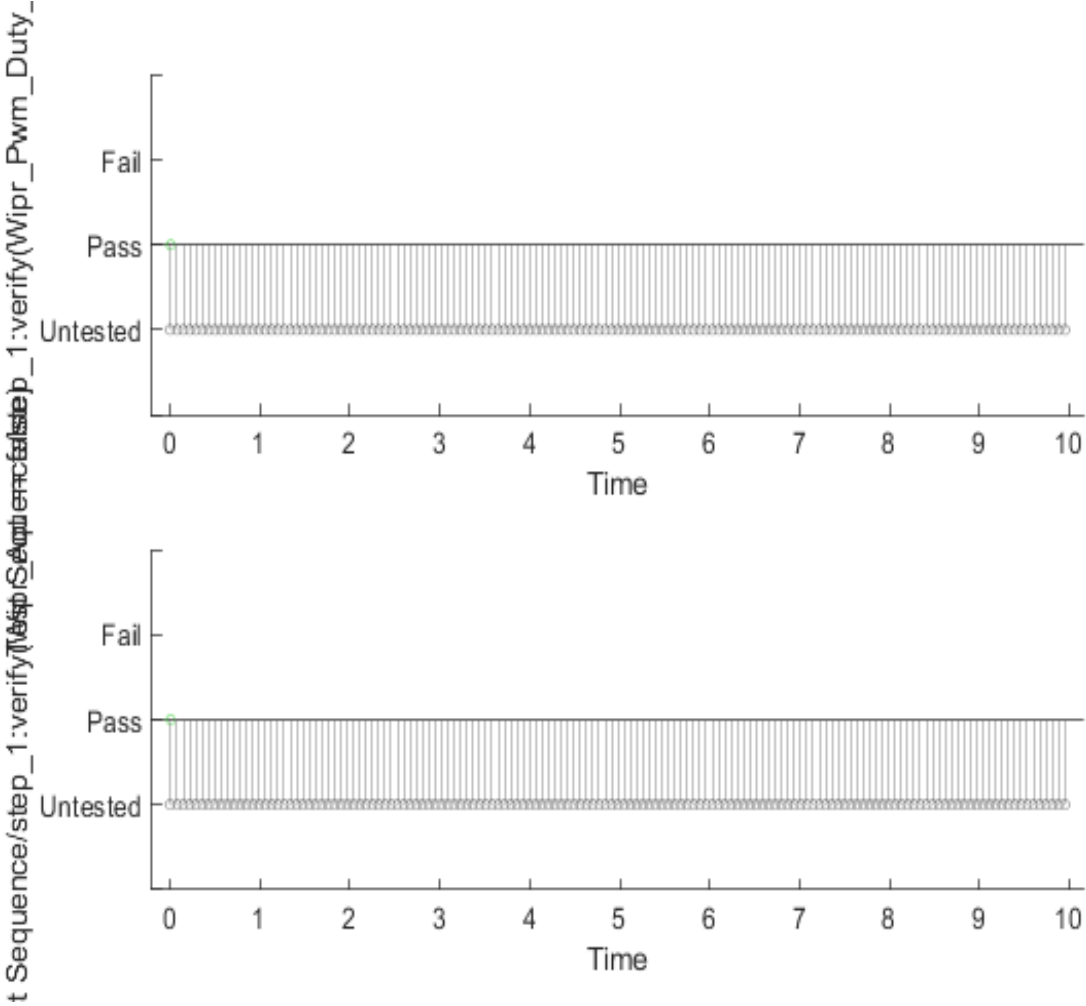
Aggregated Coverage Results

Analyzed Model	Sim Mode	Complexity	Decision	Condition	Execution
 wipr_ctrl_sys.mdl	Normal	20	96%	83%	100%

Verify Result

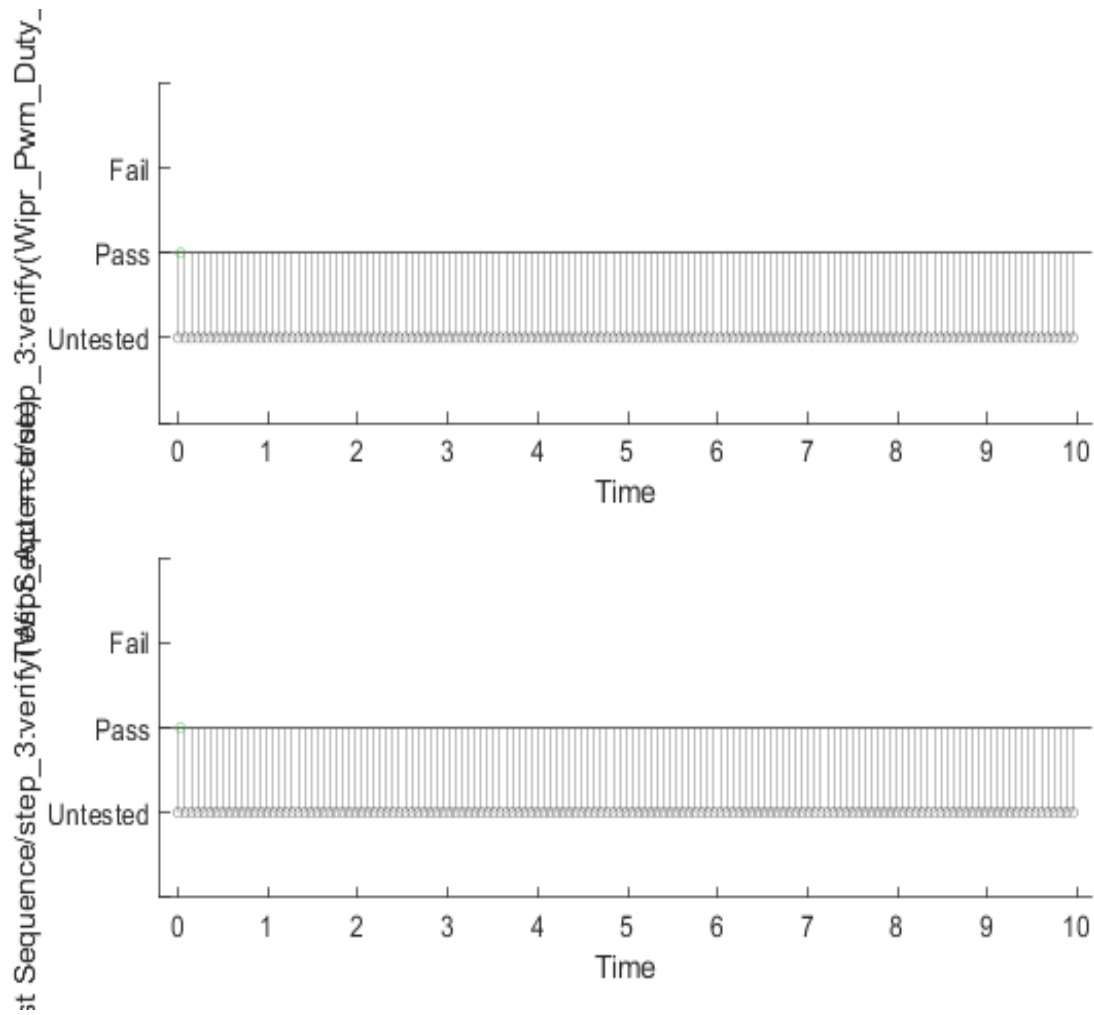
Name	Link to Plot
 Test Sequence/step_1:verify(Wipr_Pwm_Duty_Cyc == 0)	Link
 Test Sequence/step_1:verify(Wipr_Act == false)	Link
 Test Sequence/step_3:verify(Wipr_Pwm_Duty_Cyc == single(0.4))	Link
 Test Sequence/step_3:verify(Wipr_Act == true)	Link
 Test Sequence/step_5:verify(Wipr_Pwm_Duty_Cyc == single(0.7))	Link
 Test Sequence/step_5:verify(Wipr_Act == true)	Link
 Test Sequence/step_7:verify(Wipr_Pwm_Duty_Cyc == 0)	Link
 Test Sequence/step_7:verify(Wipr_Act == 0)	Link
 Test Sequence/step_9:verify(Wipr_Pwm_Duty_Cyc == single(0.45))	Link
 Test Sequence/step_9:verify(Wipr_Act == 1)	Link
 Test Sequence/step_11:verify(Wipr_Pwm_Duty_Cyc == single(0.65))	Link
 Test Sequence/step_11:verify(Wipr_Act == 1)	Link
 Test Sequence/step_13:verify(Wipr_Pwm_Duty_Cyc == 0)	Link
 Test Sequence/step_13:verify(Wipr_Act == 0)	Link

Name	
✔	Test Sequence/step_1:verify(Wipr_Pwm_Duty_Cyc == 0)
✔	Test Sequence/step_1:verify(Wipr_Act == false)



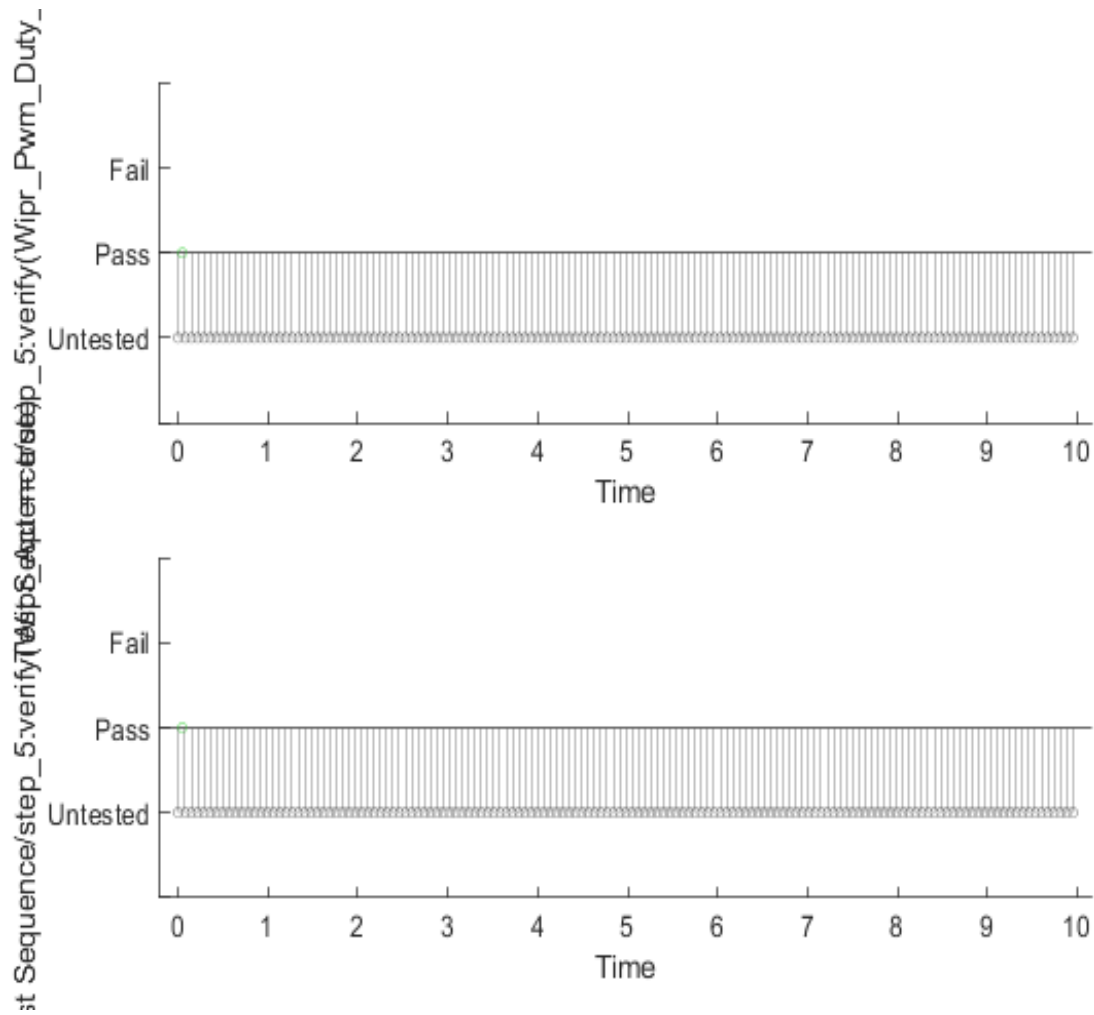
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Name	
✔	Test Sequence/step_3:verify(Wipr_Pwm_Duty_Cyc == single(0.4))
✔	Test Sequence/step_3:verify(Wipr_Act == true)



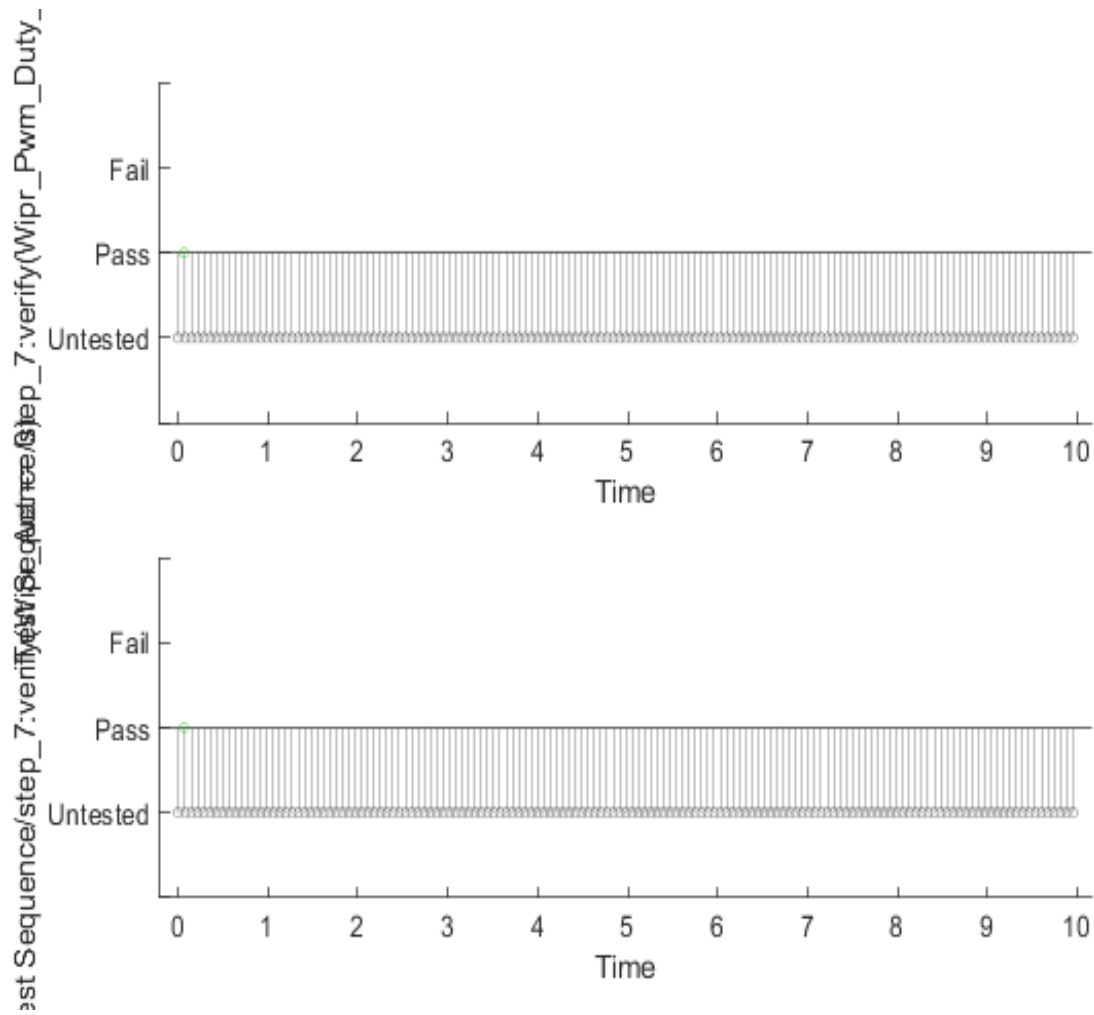
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Name	
✔	Test Sequence/step_5:verify(Wipr_Pwm_Duty_Cyc == single(0.7))
✔	Test Sequence/step_5:verify(Wipr_Act == true)



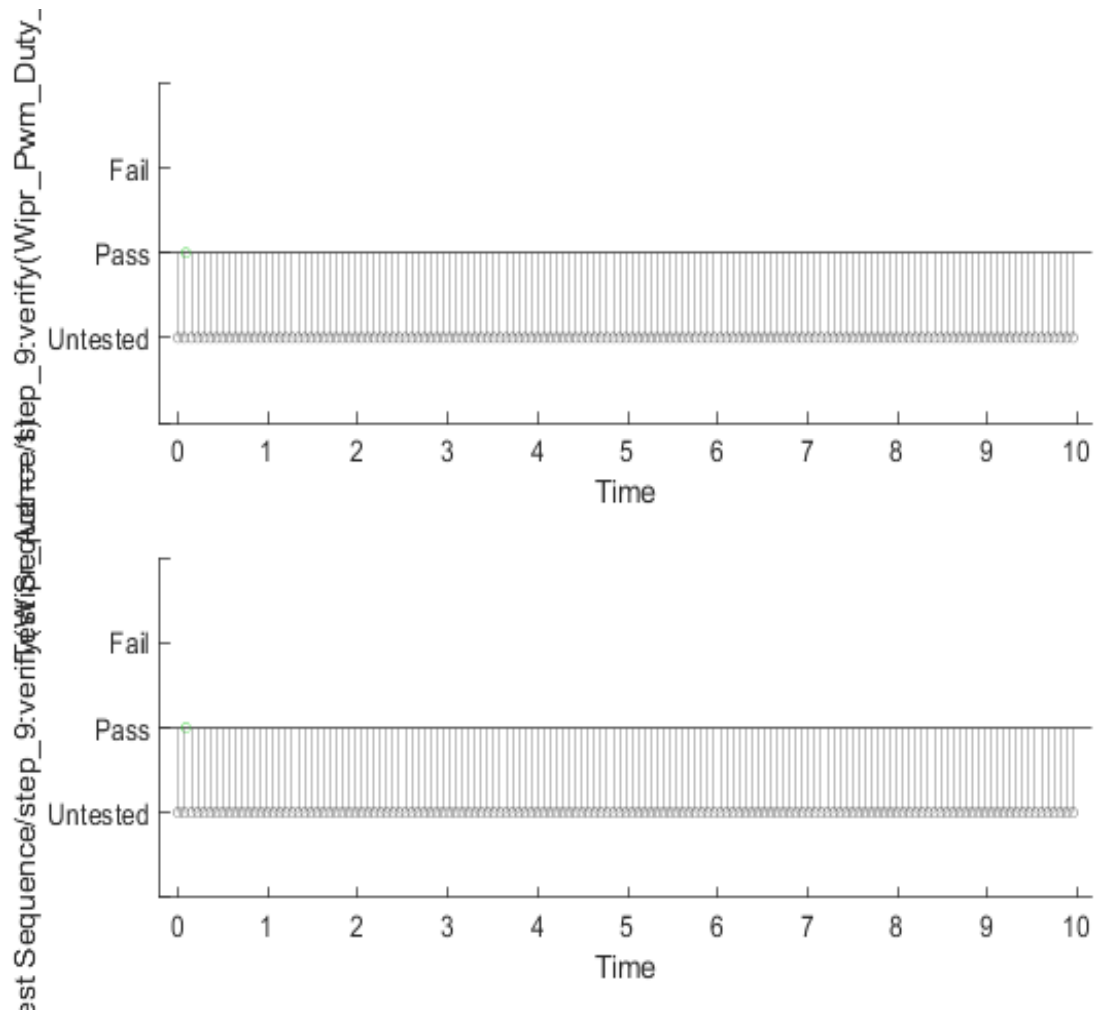
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Name	
✔	Test Sequence/step_7:verify(Wipr_Pwm_Duty_Cyc == 0)
✔	Test Sequence/step_7:verify(Wipr_Act == 0)



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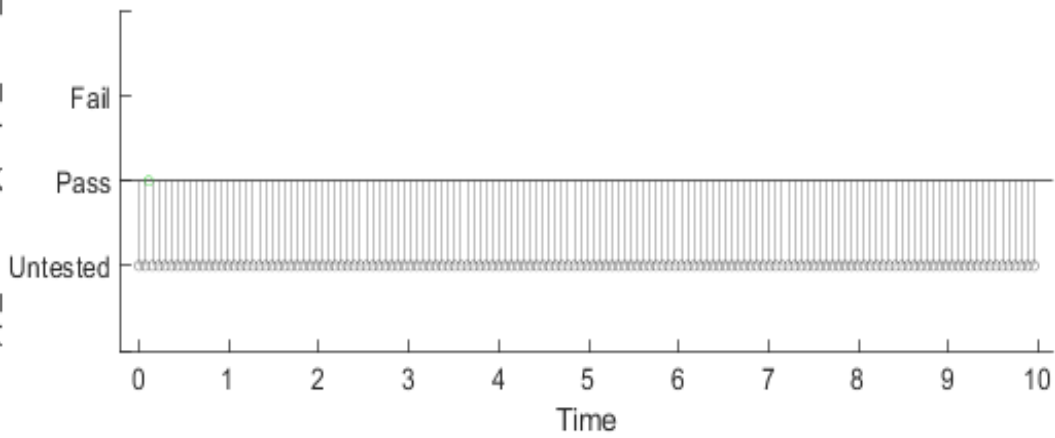
Name	
✓	Test Sequence/step_9:verify(Wipr_Pwm_Duty_Cyc == single(0.45))
✓	Test Sequence/step_9:verify(Wipr_Act == 1)



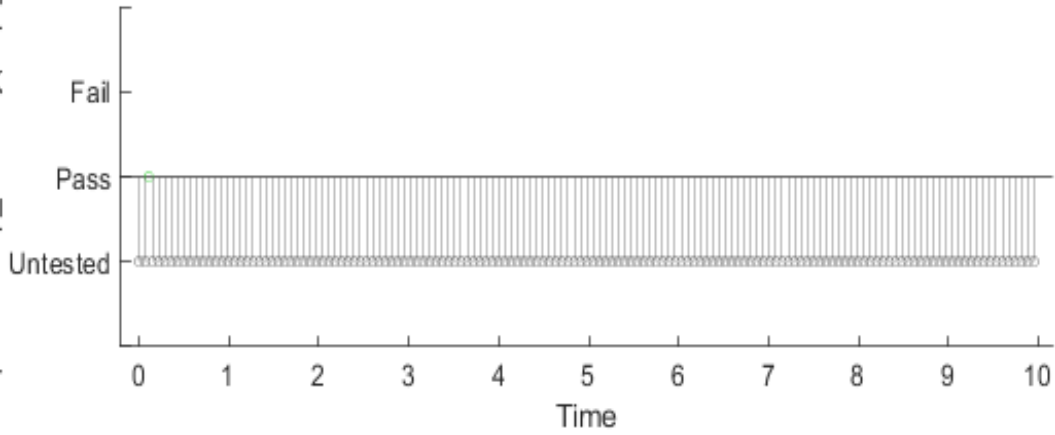
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Name	
✓	Test Sequence/step_11:verify(Wipr_Pwm_Duty_Cyc == single(0.65))
✓	Test Sequence/step_11:verify(Wipr_Act == 1)

Test Sequence/step_11:verify(Wipr_Pwm_Duty_Cyc == 0)



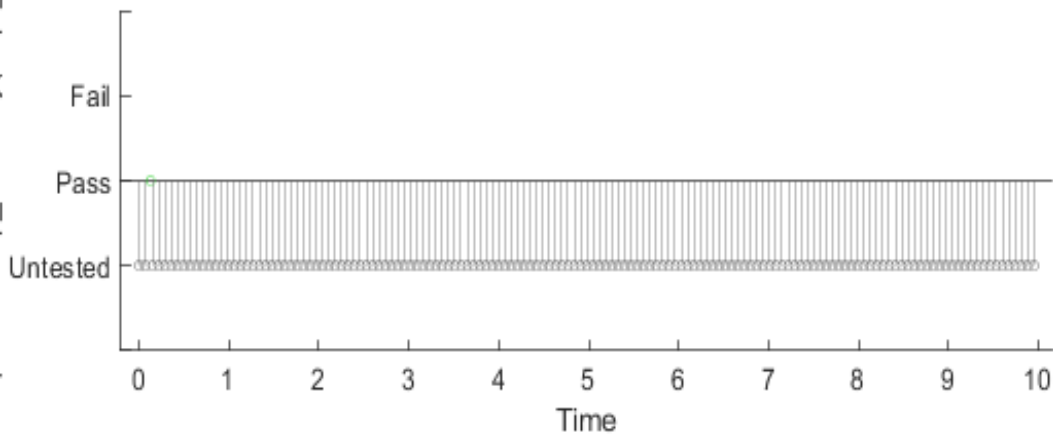
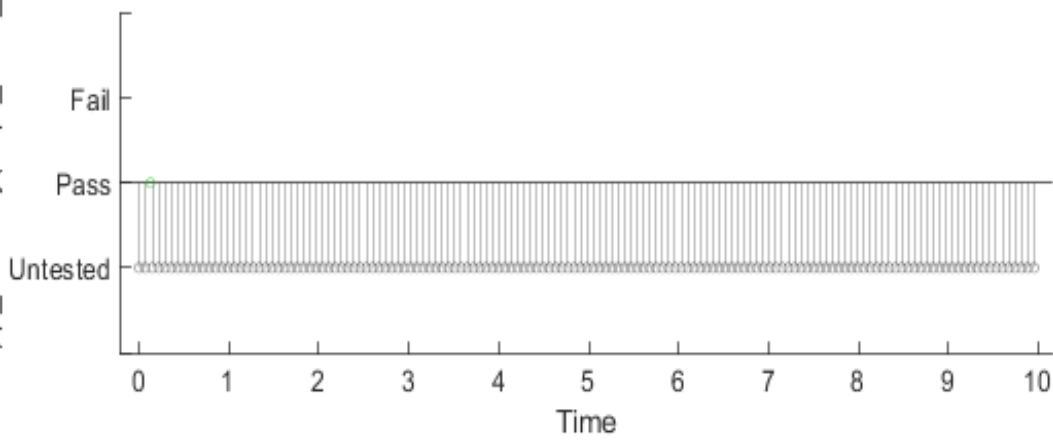
Test Sequence/step_11:verify(Wipr_Act == 0)



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Name	
✔	Test Sequence/step_13:verify(Wipr_Pwm_Duty_Cyc == 0)
✔	Test Sequence/step_13:verify(Wipr_Act == 0)

st Sequence/step_13:verify(Wipr_Pwm_Duty



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Simulation

System Under Test Information

Model:	wipr_ctrl_sys_mdl
Harness:	wipr_ctrl_sys_mdl_Harness2
Harness Owner:	wipr_ctrl_sys_mdl
Release:	Current
Simulation Mode:	normal

Override SIL or PIL Mode:	0
Configuration Set:	Configuration1
Start Time:	0
Stop Time:	10
Checksum:	531196555 3908021997 4280819077 4096374367
Simulink Version:	24.2
Model Version:	1.3
Model Author:	Hassan Mohamed
Date:	Sat Feb 15 14:20:00 2025
User ID:	Hassan Mohamed
Model Path:	F:\MyPractices\Simulink\Stateflow\Stateflow_Final_Project\wipr_ctrl_sys mdl.slx
Machine Name:	DESKTOP-IS5IP5L
Solver Name:	FixedStepDiscrete
Solver Type:	Fixed-Step
Fixed Step Size:	0.01
Simulation Start Time:	2025-02-15 14:32:55
Simulation Stop Time:	2025-02-15 14:33:05
Platform:	PCWIN64

Simulation Logs:

Parameter precision loss occurred 6 times for 'Table' of '[wipr_ctrl_sys mdl/Wiper System Controller/Chart/calcDuty_cyc/PWM Table](#)'. First occurrence: The original value of the parameter, 0.4, cannot be represented exactly using the run-time data type single. The value is quantized to 0.4000000059604645. Quantization error occurred with an absolute difference of 5.960464455334602e-9 and a relative difference of 1.49011611383365e-08.

Using the '==' operator to compare expressions of type single in the 'verify' statement can produce unexpected results.

Step '[step_1](#)' in Test Sequence '[wipr_ctrl_sys mdl Harness2/Test Sequence](#)':

```
verify(Wipr_Pwm_Duty_Cyc == 0);
```

Using the '==' operator to compare expressions of type single in the 'verify' statement can produce unexpected results.

Step '[step_3](#)' in Test Sequence '[wipr_ctrl_sys_mdl Harness2/Test Sequence](#)':

```
verify(Wipr_Pwm_Duty_Cyc == single(0.4));
```

Using the '==' operator to compare expressions of type single in the 'verify' statement can produce unexpected results.

Step '[step_5](#)' in Test Sequence '[wipr_ctrl_sys_mdl Harness2/Test Sequence](#)':

```
verify(Wipr_Pwm_Duty_Cyc == single(0.7));
```

Using the '==' operator to compare expressions of type single in the 'verify' statement can produce unexpected results.

Step '[step_7](#)' in Test Sequence '[wipr_ctrl_sys_mdl Harness2/Test Sequence](#)':

```
verify(Wipr_Pwm_Duty_Cyc == 0);
```

Using the '==' operator to compare expressions of type single in the 'verify' statement can produce unexpected results.

Step '[step_9](#)' in Test Sequence '[wipr_ctrl_sys_mdl Harness2/Test Sequence](#)':

```
verify(Wipr_Pwm_Duty_Cyc == single(0.45));
```

Using the '==' operator to compare expressions of type single in the 'verify' statement can produce unexpected results.

Step '[step_11](#)' in Test Sequence '[wipr_ctrl_sys mdl Harness2/Test Sequence](#)':

```
verify(Wipr_Pwm_Duty_Cyc == single(0.65));
```

Using the '==' operator to compare expressions of type single in the 'verify' statement can produce unexpected results.

Step '[step_13](#)' in Test Sequence '[wipr_ctrl_sys mdl Harness2/Test Sequence](#)':

```
verify(Wipr_Pwm_Duty_Cyc == 0);
```

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Test Logs:

No baseline criteria evaluation performed as no baseline data is available for this test.

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