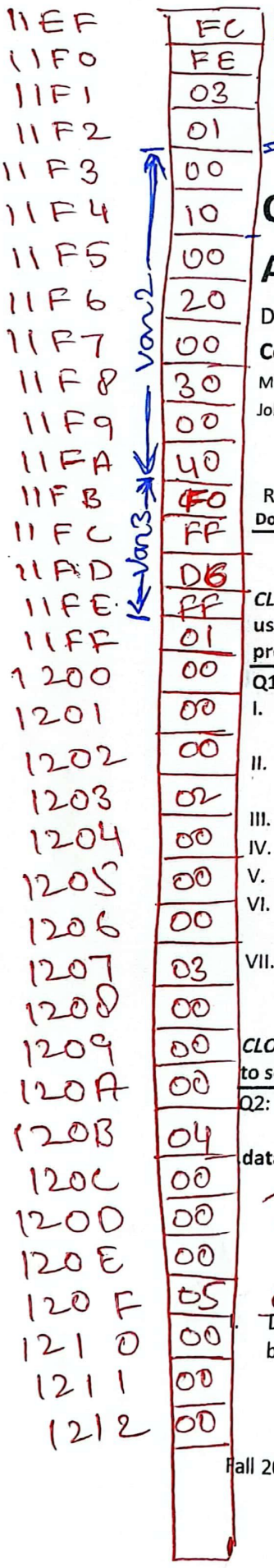

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National University of Computer and Emerging Sciences

Karachi Campus

Computer Organization and Assembly language

Sessional-I Exam

Total Time (Hrs): 1
Total Marks: 30
Total Questions: 3

Date: September 24th 2024

Course Instructor(s)

Mr. Shoaib Rauf, Mr.Kashan Hussain, Mr. Aashir Mahboob, Ms. Atiya Jokhio, Mr. M.Kariz Kamal, Mr. M.Usman, Mr. Nauraiz Subhan

Roll No Section Student Signature

Do not write below this line

Attempt all the questions.

CLO #1 & 2: **Illustrate micro-architecture of x86 and RISC processors. Create basic assembly code using different type of addressing modes in x86 and RISC ISA(s) to solve simple-moderate problems.**

Q1: Answer the following questions. **[Marks: 7*2 = 14]**

I. What is meant by a one-to-many and one-to-one relationship in context of x86 assembly. Use a coding example to support your answer.
II. Explain the Direct, In-Direct and Indexed Modes of accessing a memory in x86 assemblies using an example instruction.
III. Briefly explain the role of Virtual Machine(s) in execution of a high level language code.
IV. Why Assembly language is not portable?
V. Explain the difference(s) between Real and Protected modes of x86 processors.
VI. What is the role of memory segmentation in x86 Intel processors regarding mismatch in register size and address bus size?
VII. How many clock cycles are required in order to read a single value from main memory upon CPU request?

CLO # 2: **Create basic assembly code using different type of addressing modes in x86 and RISC ISAs to solve simple-moderate problems.**

Q2: Using the following variable definitions answer the questions given below. **[Marks: 5+5 = 10]**

.data

var1 SBYTE -4,-2,3,1
var2 WORD 1000h,2000h,3000h,4000h
var3 SWORD -16,-42
var4 DWORD 1,2,3,4,5

FFF0, FFD6

00400
0DEF
11EFh

Physical Adress.

00 00 00 01

Draw a memory map and assign proper physical addresses (using a real address mode) to each byte stored in the above data segment (Assume DS= 0040h, and the starting offset is 0DEFh).

a. FCh
b. 20h
c. 0000 1000h
d. 3000h
e. FFF0h
f. 4000h
g. 0000 0001h
h. 3001h
i. 00h
j. 0000 3FFCh

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total = 5 marks

II. What will be the hexadecimal value(s) of the destination operand after each of the following instructions are executed in sequence? {0.5 marks each}

a. mov ah, var1 — FCh
b. mov ah, byte ptr[var2+3] — 20h
c. movzx ebx, var2 — 0000 1000h
d. xchg cx, [var2+4] — 3000h
e. mov ax, var3 — FFF0h
f. mov ax,[var3-2] — 4000h
g. movsx, ebx, word ptr var4 — 0000 0001h
h. add cx, var3[type var4] — 3001h
i. mov al, [var1+6] — 00h
j. sub edx, [var4 + 12] ; Here value of edx = 4000h — 0000 3FFCh

word ptr var4 → 0001

CX = 3000h + 0001h = 3001h

CLO # 2: **Create basic assembly code using different type of addressing modes in x86 and RISC ISA(s) to solve simple-moderate problems.**

Q3: You have three different size arrays, each having 5 elements. You need to write the code to perform the following operation for each index value (X) ranging from 0 to 4, by using indirect addressing methods. **[Marks: 6]**

arrD[X] = arrD[X] - (arrB[X] + arrW[X])

The data segment has already been defined for you.
While writing code feel free to add any suitable comments to explain your steps.

```
.data
        arrB    BYTE   08h, A4h, A6h, B6h, 10h
        arrW    WORD   2 Dup(12h), 2 Dup(0Ah), 01h
        arrD    DWORD  5 Dup(FFh)

.code
;start coding from here
```

```
.code
Main PROC
mov esi, 0
mov edi, 0
mov ebx, 0
L1: mov eax, 0
mov ebx, 0
movzx eax, [arrB + esi]
movzx ebx, [arrW + edi]
add ebx, eax
sub arrD[ebx] - ebx
add esi, 1
add esi, 2
add ebx, 4
Loop L1
```

mov ecx, 4