

***COMPLEX ENGINEERING PROBLEM***

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***DEPARTMENT:*** *ELECTRONICS*

***COURSE:*** *MICROPROCESSOR PROGRAMMING & INTERFACE (MPI)*

***CODE:***

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**DISPLAYING 7 SEGMENTS USING 8088 MICROPROCESSORS**

**COMPONENTS:**

***MICROPROCESSOR (8088):***

The 8088 processor, also known as Intel 8088, is a 16-bit microprocessor introduced by Intel in 1979. It is part of the Intel 8086 family and was one of the earliest x86 microprocessors. The 8088 is widely known for its use in the original IBM PC, which was released in 1981

***LATCH (74SC373):***

The 74SC373 is an octal transparent latch with three-state outputs. It has eight data inputs (D0 to D7) and eight outputs (Q0 to Q7). When the latch is enabled (by the latch enable input, LE), the data at the inputs passes to the outputs. When disabled, the outputs are in a high-impedance state (three-state)

***PPI (8255A):***

The 8255A Programmable Peripheral Interface (PPI) is an integrated circuit that provides parallel I/O capabilities for microprocessors. It has three 8-bit ports (Port A, Port B, and Port C) that can be configured as inputs or outputs, making it versatile for interfacing with various devices in embedded systems.

The other circuitry components include push buttons, resistors, and a 7-segment display.

***EEPROM (2816)***

The EEPROM (2816) is a type of electrically erasable programmable read-only memory with a capacity of 2 kilobits (256 bytes). It can be both electrically erased and reprogrammed, making it suitable for non-volatile data storage in various electronic systems.

***BUFFERS (74245)***

Used in digital systems to amplify and isolate signals. They serve as intermediaries between different parts of a circuit, preventing signal degradation and maintaining signal integrity. These devices can be crucial in scenarios where a weak or high-impedance output needs to drive multiple inputs or long transmission lines. By providing a low-impedance output, buffers help prevent loading effects and ensure efficient data transfer between various components in a system

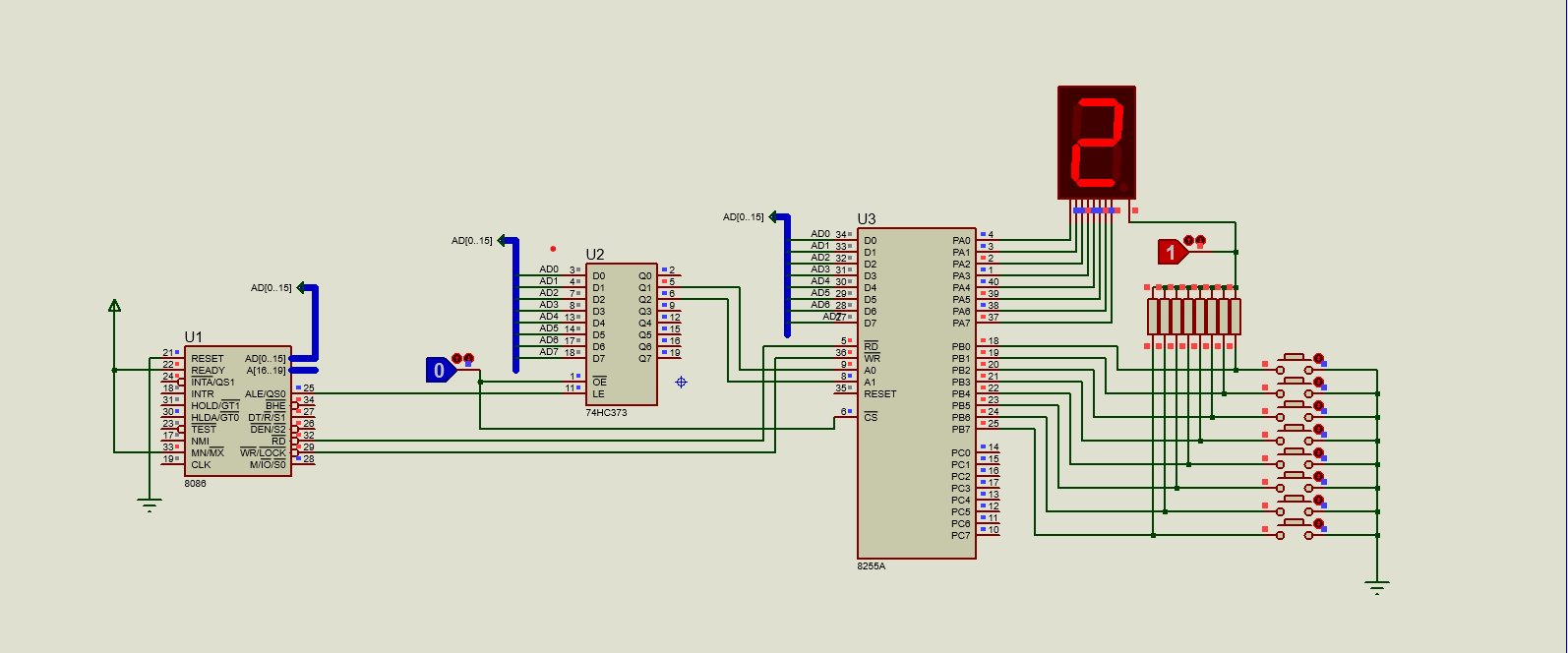
***CLK GENERATOR (8284)***

Is a peripheral integrated circuit (IC) used to produce stable and precise clock signals in microprocessor-based systems. It generates various clock frequencies and control signals required for the proper functioning of the microprocessor. The 8284 chip is commonly employed with Intel 8086 and 8088 microprocessors, ensuring synchronization and timing accuracy, which are critical for reliable system operation. By providing a steady clock source, the 8284 facilitates efficient data transfer and coordination between different components, enhancing overall system performance and stability

***7-SEGMENT***

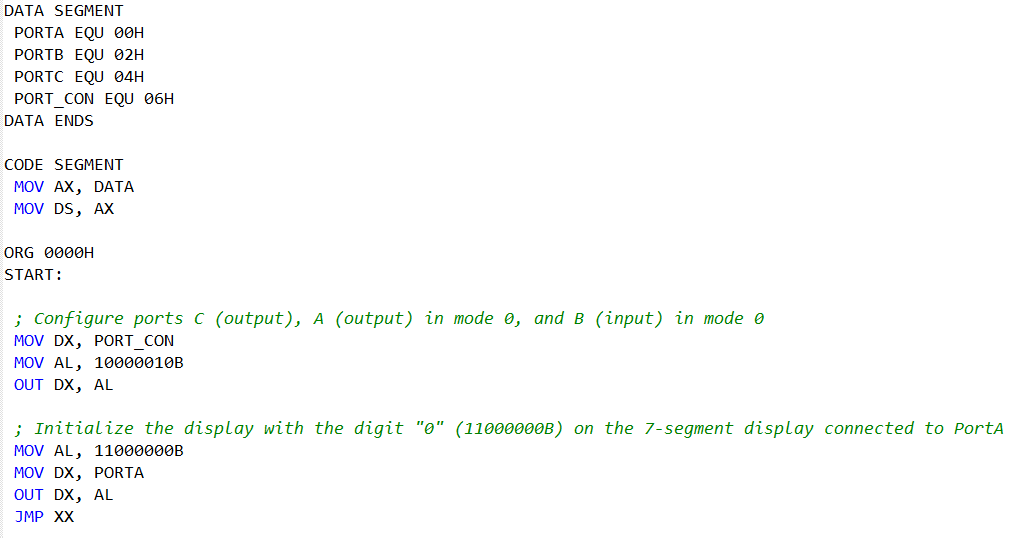
A 7-segment display is a type of electronic display device that can show decimal digits (0-9) using seven segments. It is commonly used for digital displays in various applications such as clocks, calculators, and digital counters. Each segment can be individually activated to form the desired digit.

**SIMULATION:**

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* The connections of the circuitry are explained below.
* The RESET pin is grounded or kept LOW to initiate a system reset, enabling the 8088 to start from a predefined address, usually the start of the program memory.
* The READY pin and MIN/pins are kept High. The READY pin is used for bus synchronization and indicates that 8088 is ready to accept or provide data (HIGH state).
* The MN/pins enable two different modes of operation for the microprocessor at two different logics.
* The AD[0…7] indicates the bus of the microprocessor and both the latch and the peripheral.
* The ALE/Qso (Address Latch Enable/Queue Status Output) pin of the 8086 microprocessor is connected to the LE (Latch Enable) pin of the latch to facilitate the latching of address information during the microprocessor's operation.
* By connecting the ALE/Qso pin of the 8088 microprocessor with the LE pin of the latch, the latch can take advantage of the timing of the ALE signal. During the first clock cycle of an operation, when the ALE signal is active, the latch's LE pin is asserted, allowing the input data (in this case, the address on the address bus) to pass through and be latched by the latch.
* Then the latched address information is used by the 8255A peripheral device, to perform operations specific to that address.
* The pin of the 8088 is connected with the pin of the 8255. Both are active low logic. A low input on the 8088 RD pin allows it to read the data sent by the RD pin of the 8255, at low input.
* The pin of the 8088 is connected with the pin of the PPI. When the input is low on the pin, it allows the CPU to write data or control it into the 8255.
* The A0 and A1 (input pins of the PPI) are connected with the output pins (Q1 and Q2 respectively) of the 74HC373 and control the selection of the three ports or the control word register.
  + If A0=0 and A1=0, then Port A is selected.
  + If A0=1 and A1=0, then Port B is selected.
  + If A0=0 and A1=1, then Port C is selected.
  + If A0=1 and A1=1, then CONTROL is selected.
* The OE (Output Enable) pin of the latch and CS(Chip Select) pin of the PPI are connected with the logic state.
* When the OE pin is kept low, the outputs become active, allowing the latched data to be propagated to the external circuit. Conversely, reasserting the OE pin (typically HIGH or 1) puts the outputs in a high-impedance state, effectively disconnecting them from the external circuit. This high-impedance state is useful when multiple devices are connected to a common bus, as it prevents conflicts and allows other devices to drive the bus without interference.
* Similarly, when the CS pin is kept low, it enables communication between the 8255 and the microprocessor. In this state, the PPI responds to the control and data signals from the microprocessor or other controlling device. When the CS pin is de-asserted (typically HIGH or 1), it indicates that the PPI is deselected or disabled, and the PPI does not respond to any control or data signals.

**ASSEMBLY LANGUAGE CODE:**

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