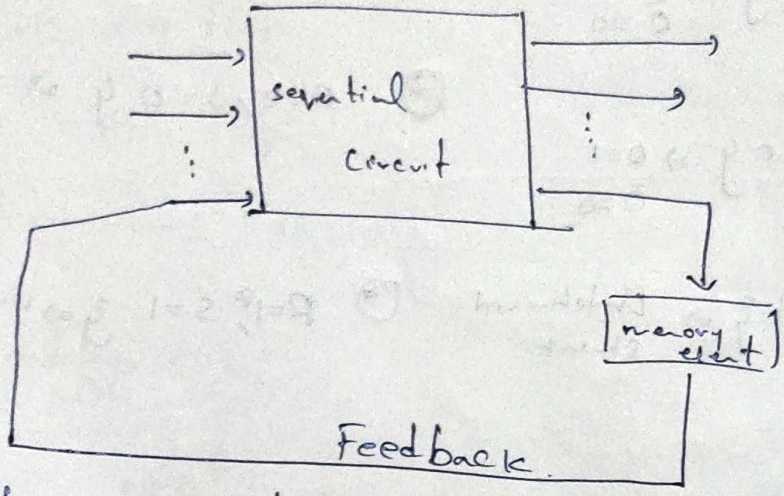
Sequential circuit

In Sequential Circuit present o/p depends on present i/p as well as previous o/p.



* Present o/p = present i/p + previous o/p
* Sequential Circuit = Combinational circuit + memory element

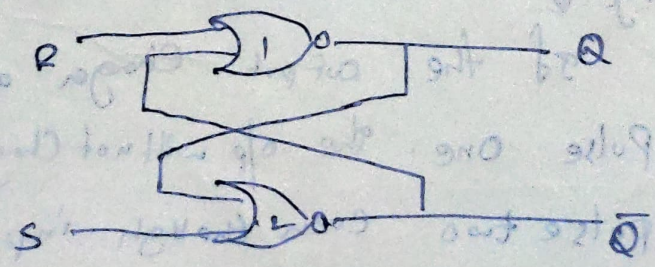
Flip Flop

→ Flip-flop is a basic memory element which is used to store 1 bit of data.

Latch

→ latch is a basic memory element which is used to store 1 bit of data.

~~Basic latch~~ Basic diagram of latch



Sequence ①

① $\{R=1, S=0\} \Rightarrow Q=0, \bar{Q}=1$

② $\{R=0, S=1\} \Rightarrow Q=1, \bar{Q}=0$

③ $\{R=0, S=0\} \Rightarrow Q=1, \bar{Q}=0$

④ $\{R=1, S=1\} \Rightarrow$ undefined state.

Sequence ②

① $\{R=0, S=1\} \Rightarrow Q=1, \bar{Q}=0$

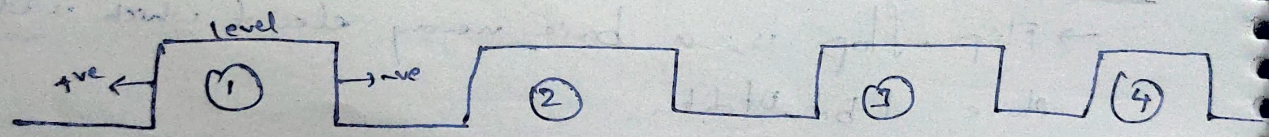
② $\{R=1, S=0\} \Rightarrow Q=0, \bar{Q}=1$

③ $\{R=0, S=0\} \Rightarrow Q=0, \bar{Q}=1$

④ $\{R=1, S=1\} \Rightarrow$ undefined statement.

Clock signal

The appl" clock pulse (or clock signal) is triggering which means output Changes according to the Input at the occurance of clock signal



1. Rising edge (+ve edge)
2. falling edge (-ve edge)
3. level edge

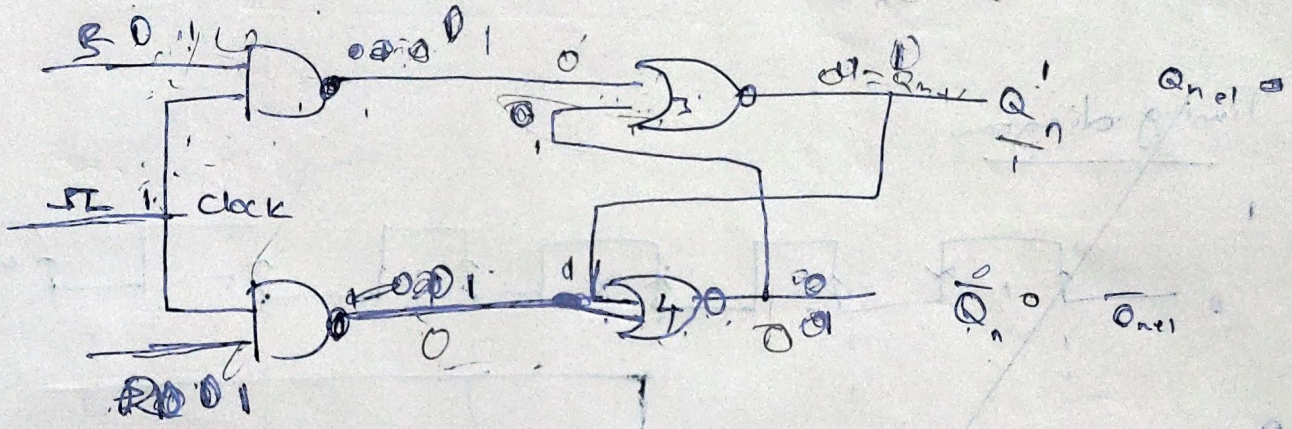
If the output Changes at the +ve edge of Clock Pulse one. the o/p will not Change upto +ve edeg of clock Pulse two even though input changes.

Flip Flops :

There are 4 types of flip flops
↳ flipflop has a clock & Latch doesnot have clock.

1. R-S flip flop
2. D flip flop → Data / Delay.
3. J-K flip flop
4. T flip flop.
   → Toggle :

R-S flipflop :



Characteristic table

Q_n	R	S	Q_{n+1}
0	0	0	0
0	0	1	1
0	1	0	0
0	1	1	X
1	0	0	1
1	0	1	1
1	1	0	0
1	1	1	X

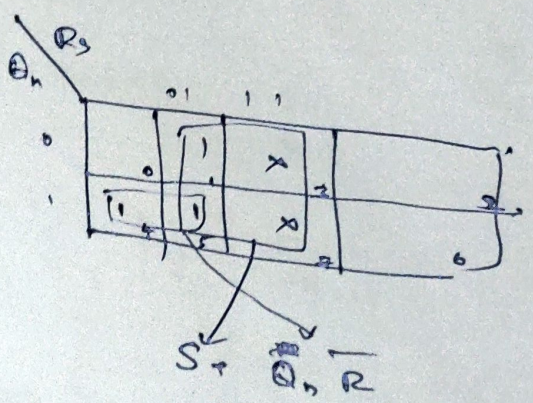
Truth table

R	S	Q_{n+1}
0	0	Q_n → Hold
0	1	1 → set
1	0	0 → Reset
1	1	X → un defined

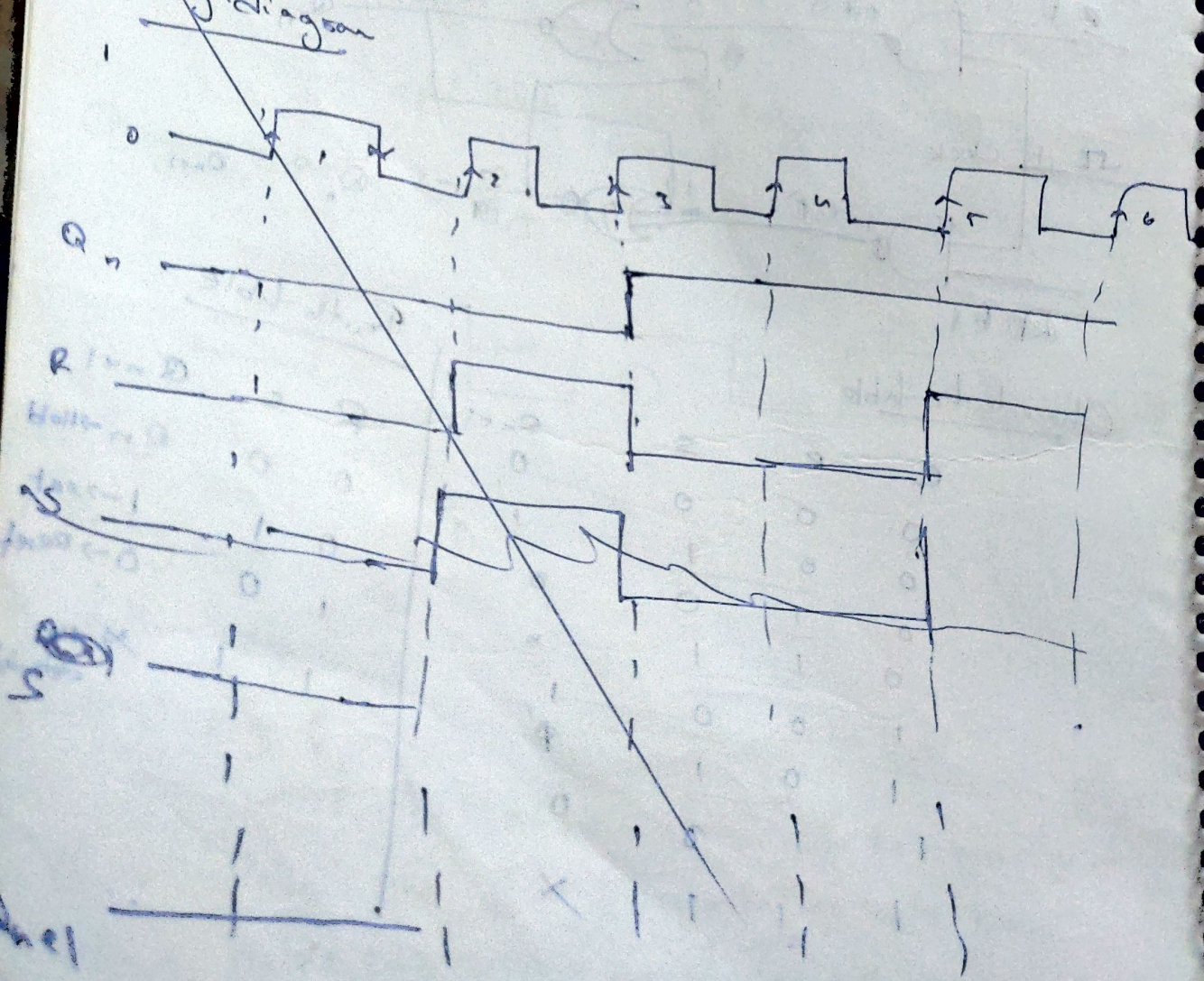
Characterstic equation:

~~$Q_{n+1}(Q_n, R, S) = \Sigma m(\ ) + \Sigma d(\ )$~~

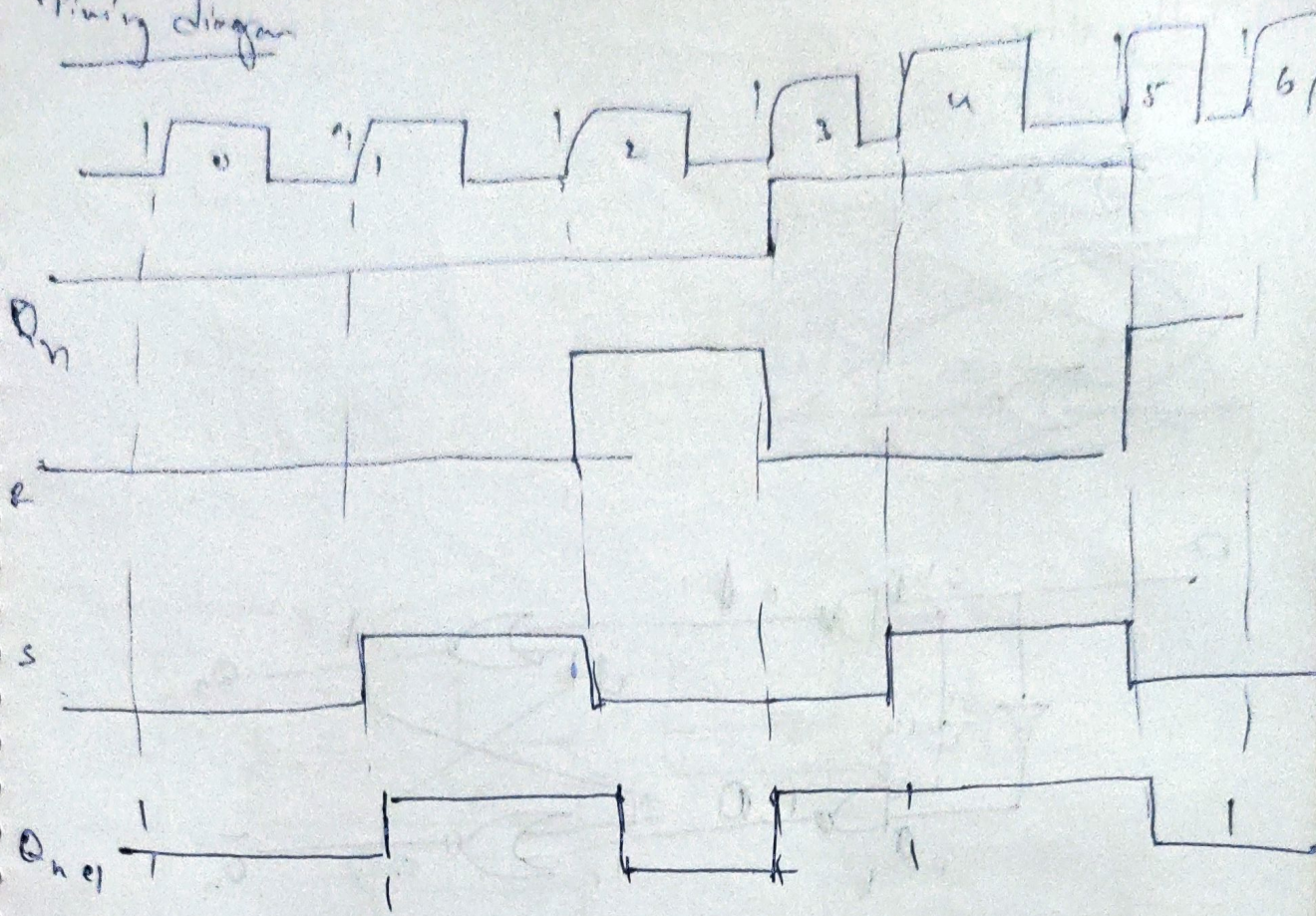
$$Q_{n+1}(Q_n, R, S) = \Sigma m(1,4,5) + \Sigma d(3,7)$$



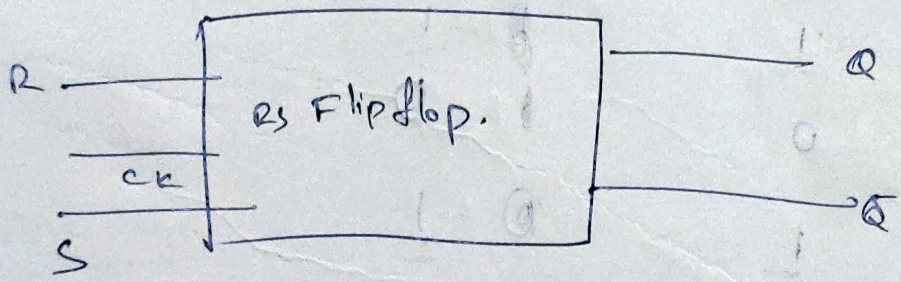
Timing diagram



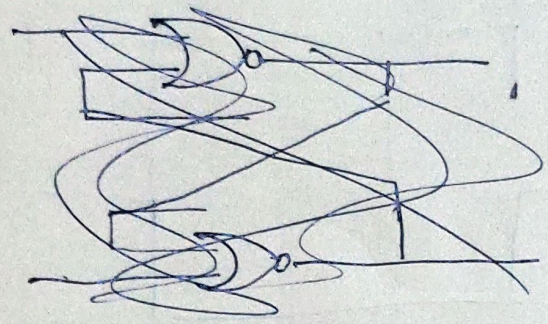
Timing diagram

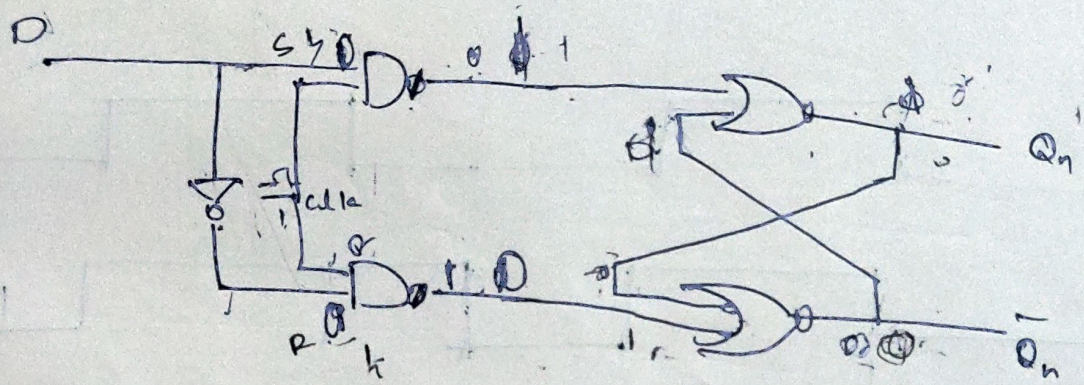


Block Diagram



D flip flop:





Charecterstic table

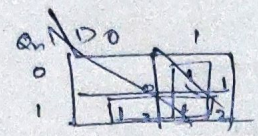
Q_n	D	Q_{n+1}
0	0	0
0	1	1
1	0	0
1	1	1

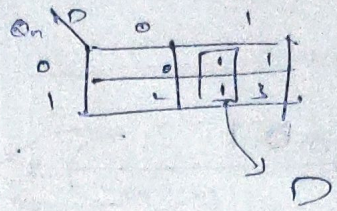
Truth table

D	Q_{n+1}
0	0
1	1

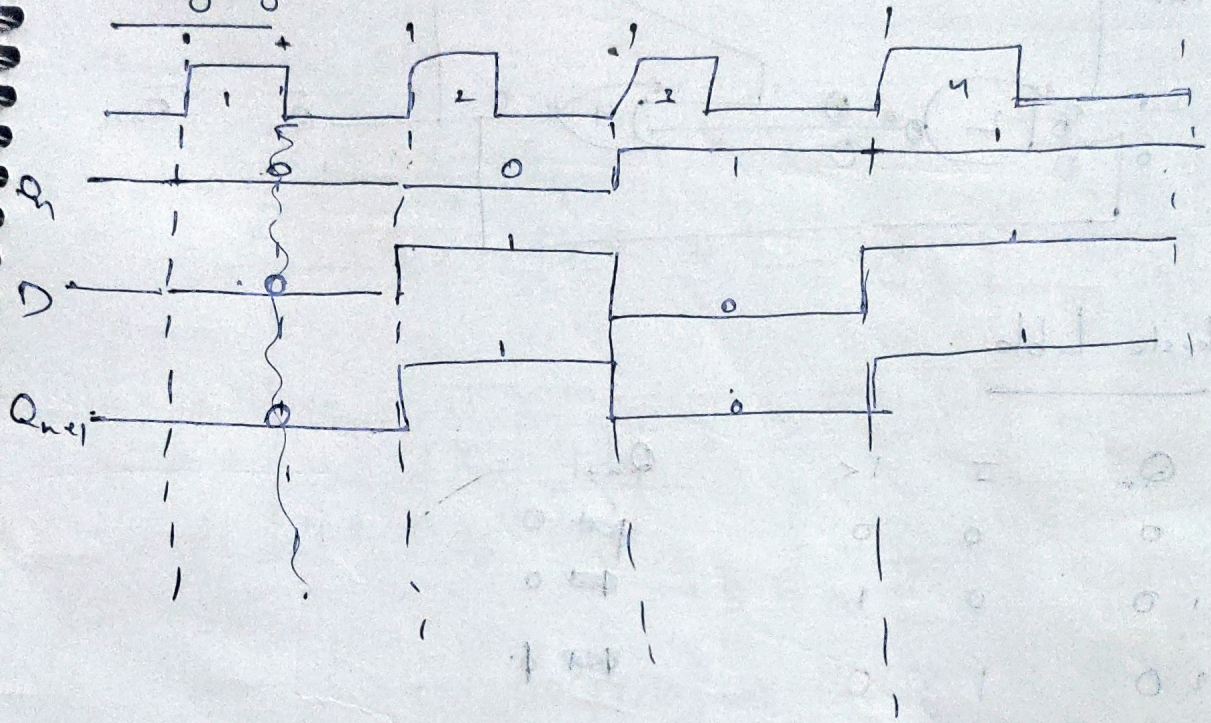
Characteristic eqn

$$Q_{n+1}(Q_n, D) = \Sigma m(1, 3)$$

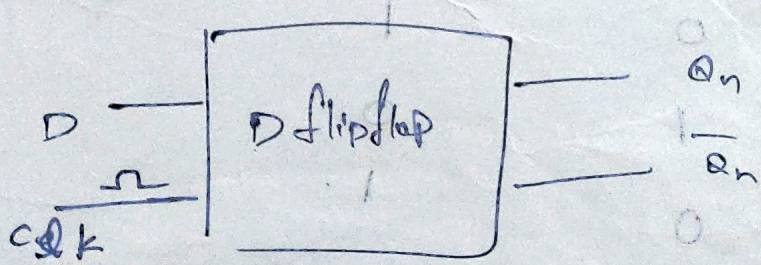




Timing diagram

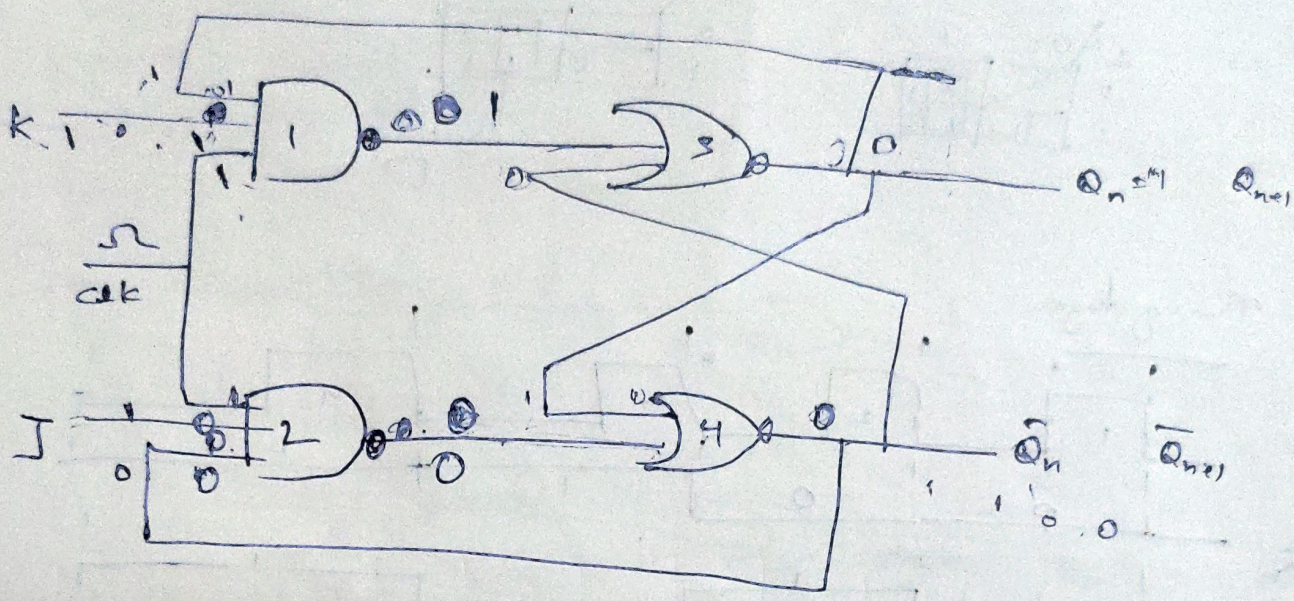


Block diagram



J - K flip flop:

→ Jack - kilby ~~flipflop~~ flipflop.



Charterstic table

	Q_n	J	K	Q_{n+1}
0	0	0	0	0
1	0	0	1	0
2	0	1	0	1
3	0	1	1	1
4	1	0	0	1
5	1	0	1	0
6	1	1	0	1
7	1	1	1	0

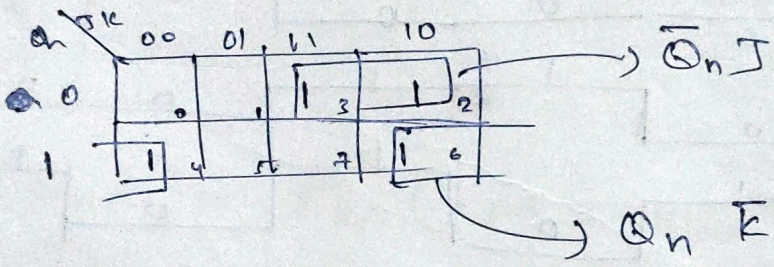
Truth table

J	K	Q_{n+1}
0	0	Q_n → no change
0	1	0
1	0	1
1	1	$\overline{Q_n}$ → Toggle

Characteristic eqn

~~$Q_{n+1}(J,K) = Q_n(0)$~~ +

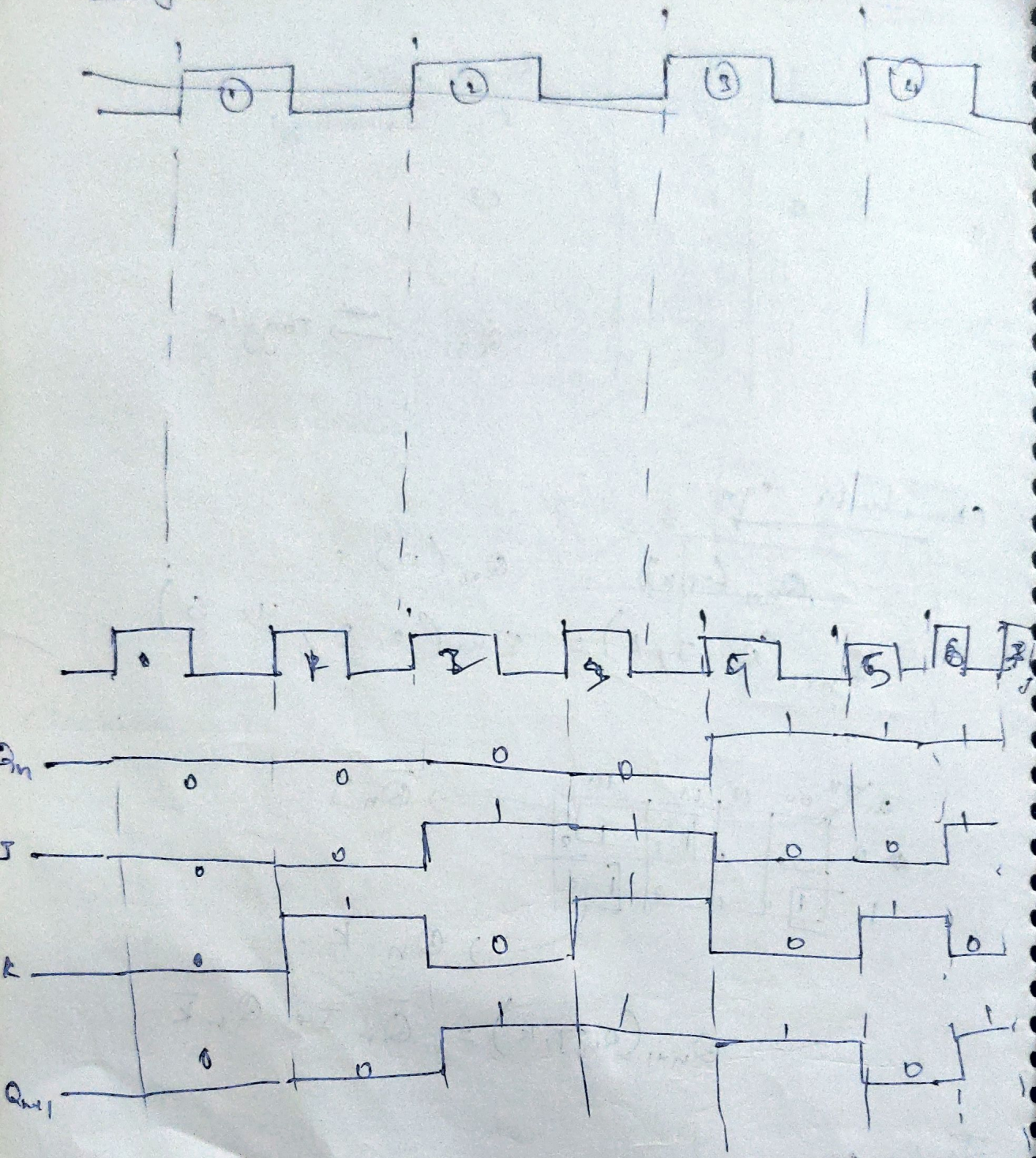
$$Q_{n+1}(Q_n, J, K) = \Sigma m(2, 3, 4, 6)$$



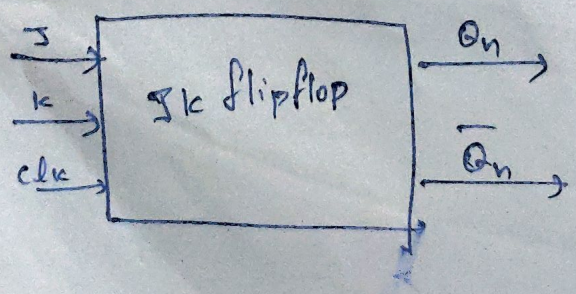
$$Q_{n+1}(Q_n, J, K) = \overline{Q_n}J + Q_n\overline{K}$$

~~Timing eqn~~

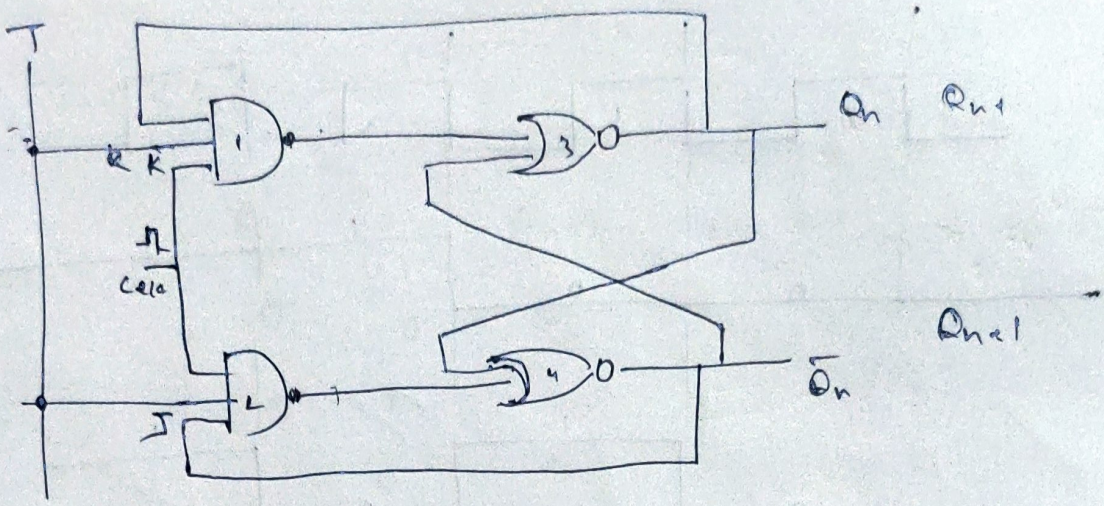
Timing diagram



Block diagram



T- flip flop



Characteristic table

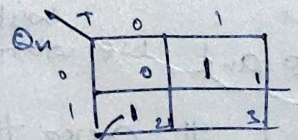
	Q_n	T	Q_{n+1}
0	0	0	0
1	0	1	1
2	1	0	1
3	1	1	0

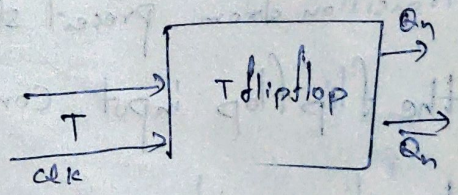
Truth table

T	Q_{n+1}
0	Q_n
1	$\bar{Q}_n$

$$Q_{n+1}(Q_n, T) = \Sigma m(1, 2)$$

Block Diagram

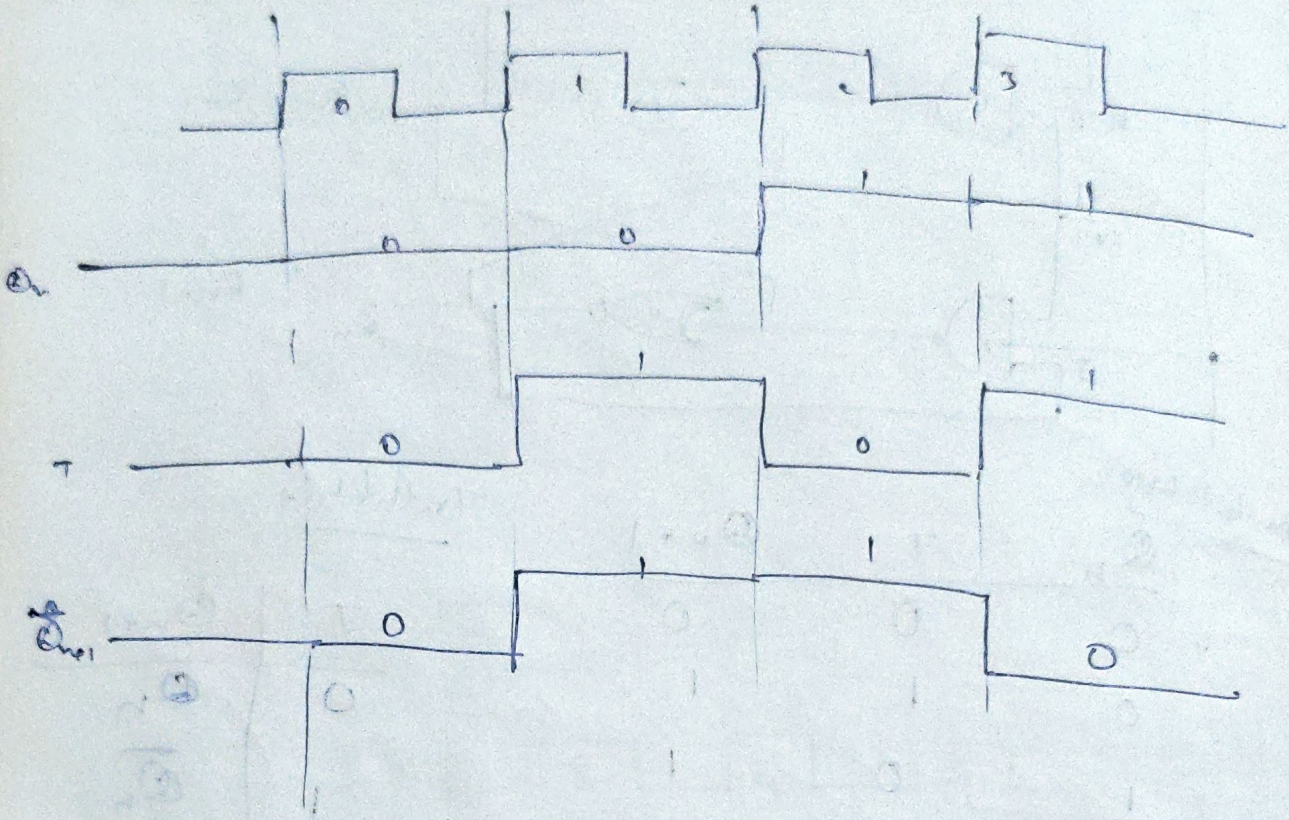




$$Q_n\bar{T} + \bar{Q}_n T$$

$$Q_{n+1} = \bar{Q}_n T + Q_n \bar{T}$$

Timing diagram



Excitation Table:

~~There the a design proc~~ during

During a design procedure the designer knows the transition from present state to next state and we ~~wish to~~ wish find the flip flop input conditions that will cause the required transition. We need a table that lists the required inputs for the given changes of states (present/next). The table is called an excitation table.

R-S flip flop excitation table

Truth table

R	S	Q_{n+1}
0	0	Q_n
0	1	1
1	0	0
1	1	∞

Excitation table

Q_n	Q_{n+1}	R	S
0	0	x	0
0	1	0	1
1	0	1	0
1	1	0	x

R	S	Q_{n+1}	$Q_n=0$, $Q_{n+1}=0$: 0	$Q_n=0$, $Q_{n+1}=1$: 1	$Q_n=1$, $Q_{n+1}=0$: 0	$Q_n=1$, $Q_{n+1}=1$: 1
0	0	Q_n	0 ✓	0	1	1 ✓
0	1	1	1	1 ✓	1	1 ✓
1	0	0	0 ✓	0	0 ✓	0
1	1	x	x	x	x	x

D flip flop excitation table

Truth table

D	Q_{n+1}
0	0
1	1

Excitation table

Q_n	Q_{n+1}	D
0	0	0
0	1	1
1	0	0
1	1	1

D	Q_{n+1}	$Q_n=0$, $Q_{n+1}=0$	$Q_n=0$, $Q_{n+1}=1$	$Q_n=1$, $Q_{n+1}=0$	$Q_n=1$, $Q_{n+1}=1$
0	0	0 ✓	1	0 ✓	1
1	1	1	0 ✓	1	0 ✓

J-K flip flop excitation table

Truth table

J	K	Q_{n+1}
0	0	Q_n
0	1	0
1	0	1
1	1	$\bar{Q}_n$

Excitation table

Q_n	Q_{n+1}	J	K
0	0	0	X
0	1	1	X
1	0	X	1
1	1	X	0

D	J	K	Q_{n+1}	$Q_n=0$, $Q_{n+1}=0$	$Q_n=0$, $Q_{n+1}=1$	$Q_n=1$, $Q_{n+1}=0$	$Q_n=1$, $Q_{n+1}=1$
				0	1	0	1
0	0		Q_n	0 ✓	0	1	1 ✓
0	1		0	0 ✓		0 ✓	0
1	0		1	1	1 ✓	1	1 ✓
1	1		$\overline{Q_n}$	1	1 ✓	0 ✓	0

T flip-flop

T	Q_{n+1}
0	Q_n
1	$\overline{Q_n}$

T	Q_{n+1}	$Q_n=0$, $Q_{n+1}=0$	$Q_n=0$, $Q_{n+1}=1$	$Q_n=1$, $Q_{n+1}=0$	$Q_n=1$, $Q_{n+1}=1$
		0	1	0	1
0	Q_n	0 ✓	0	1	1 ✓
1	$\overline{Q_n}$	1	1 ✓	0 ✓	0

Excitation table

Q_n	Q_{n+1}	T
0	0	0
0	1	1
1	0	1
1	1	0

→ When clock = 0, for T = 0 previous o/p is retained, by circuit when T = 1 along with the clock pulse the o/p toggles from to previous value. as given in the characteristic table below.

~~Conversion~~

Conversion of flipflops

Q_n	Q_{n+1}	R	S	D	J	K	T
0	0	x	0	0	0	x	0
0	1	0	1	1	1	x	1
1	0	1	0	0	x	1	1
1	1	0	x	1	x	0	0

~~Convex~~

Conversion

Q) Convert T flip flop into D flip flop.

Convert a given type of flip flop into Desired type of flipflop by adding some conversion logic.

Excitation table of T & D

$T = Q_n \oplus D$

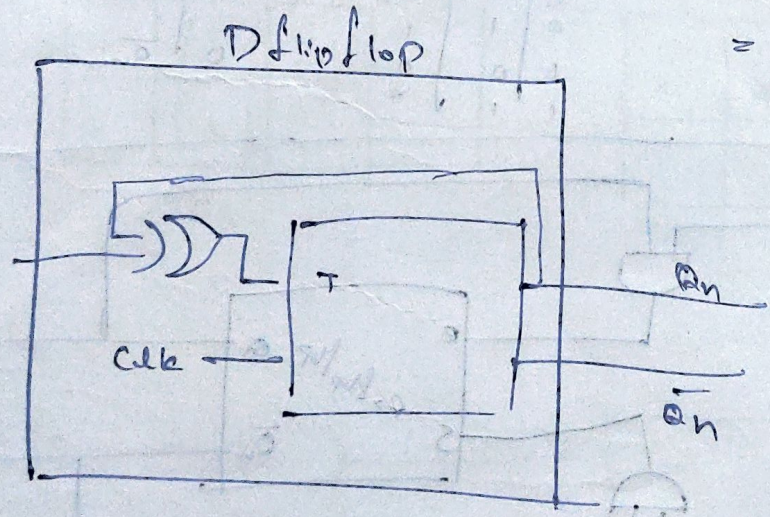
Q_n	Q_{n+1}	D	T
0	0	0	0
0	1	1	1
1	0	0	1
1	1	1	0

$T(Q_n, D) = \Sigma m(1,2)$

$Q_n \backslash D$	0	1
0	0	1
1	2	3

$T = \bar{Q}_n D + Q_n \bar{D}$

$= Q_n \oplus D.$



Conversion of RS flipflop into T flipflop

Excitation tables

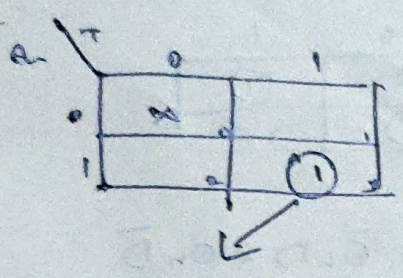
PS Q_n	NS Q_{n+1}	Control T	R	S
0	0	0	x	0
0	1	1	0	1
1	0	1	1	0
1	1	0	0	x

(R, S: required flipflop)

$R(Q_n, T) = \Sigma m(3) + \Sigma d(0)$
$= Q_n \cdot T$

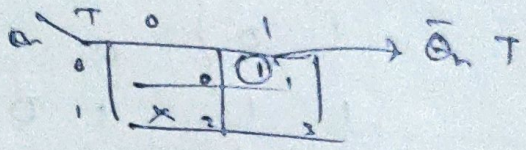
$S(Q_n, T) = \Sigma m(1) + \Sigma d(2)$
$= \overline{Q_n} \cdot T$

R



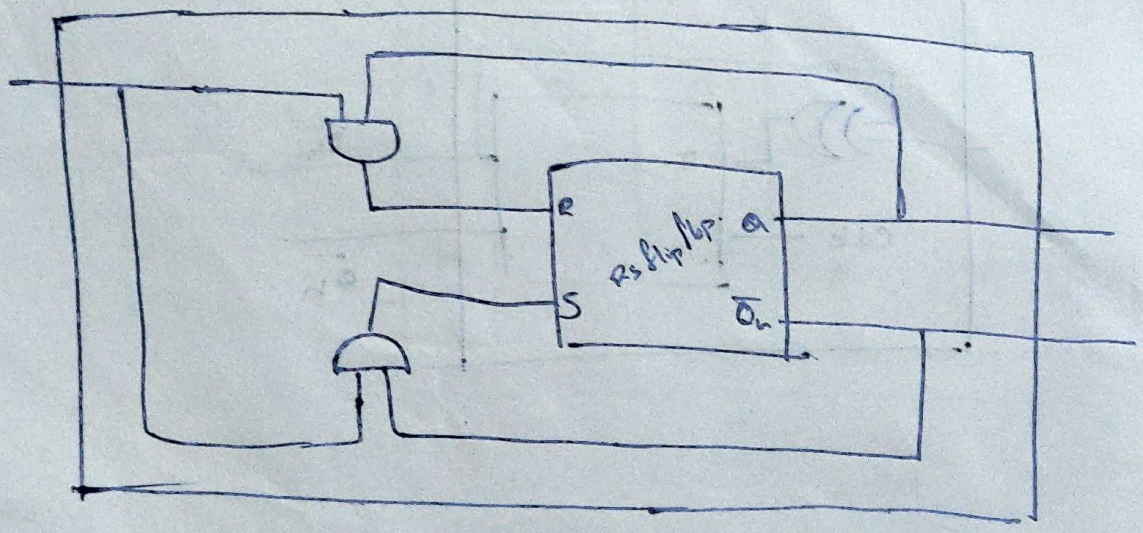
$Q_n \cdot T$

S



R	S	Q_{n+1}
0	0	Q_n
0	1	1
1	0	0
1	1	x

T	Q_{n+1}
1	Q_n
0	$\overline{Q_n}$



T flipflop

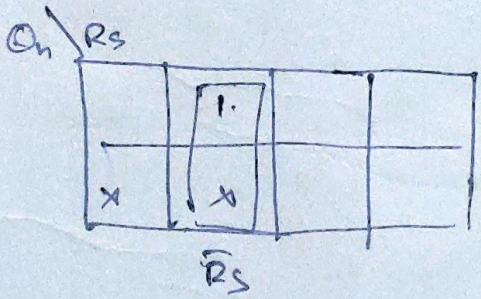
Conversion of J K into RS

		device		switching	
Q_n	Q_{n+1}	R	S	J	K
0	0	x	0	0	x
0	1	0	1	1	x
6 — 1	0	1	0	x /	1
1	1	0	x	x	0

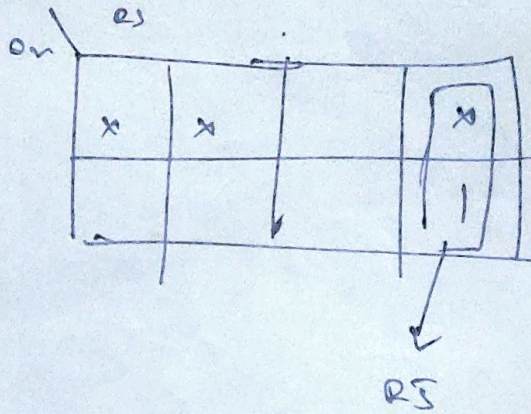
$$J(Q_n, R, S) = \Sigma m(1) + \Sigma d(4,5,6)$$

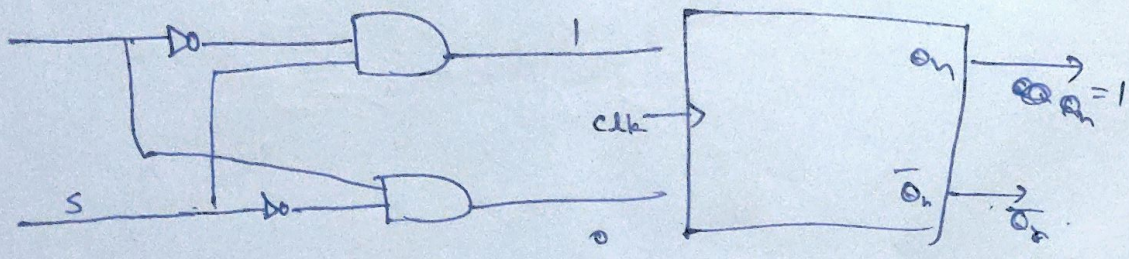
$$K(Q_n, R, S) = \Sigma m(6) + \Sigma d(0,1,2)$$

J



K



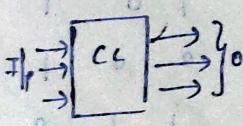


Combinational vs Sequential Circuit.

→ o/p depends on the present i/p

eg: Adder

$$\begin{array}{r} 1 \\ +0 \\ \hline 1 \end{array}$$

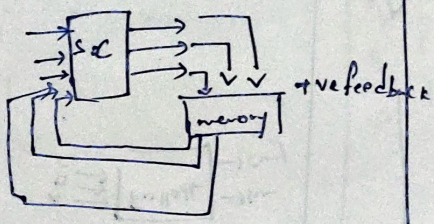


→ o/p depends on present i/p and also previous o/p.

eg: Counter

+1 prev op

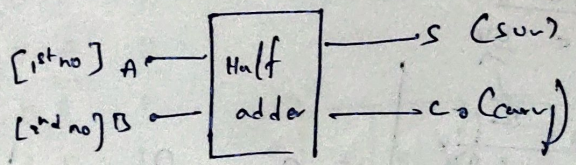
$$\begin{array}{r} 5 \\ +1 \\ \hline +6 \end{array}$$



Half adder (Combinational Circuit).

→ used to add single bit number.

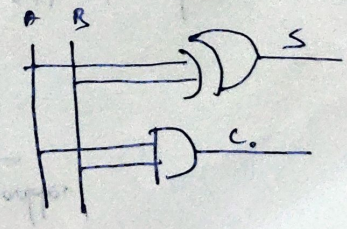
→ It does not take carry from previous sum



A	B	S	C_0
0	0	0	0
0	1	1	0
1	0	1	0
1	1	0	1

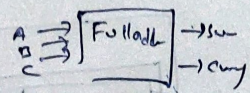
$S = A \oplus B$

$C_0 = A \cdot B$



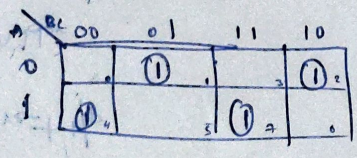
Full adder

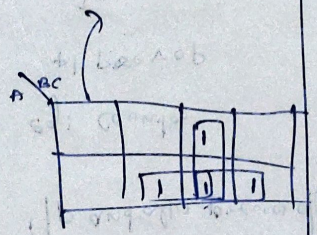
	A	B	C	S	C_o
0	0	0	0	0	0
1	0	0	1	1	0
2	0	1	0	1	0
3	0	1	1	0	1
4	1	0	0	1	0
5	1	0	1	0	1
6	1	1	0	0	1
7	1	1	1	1	1



$C_o = BC + AB + AC$

for S





$\bar{A}\bar{B}\bar{C} + \bar{A}\bar{B}C + ABC + \bar{A}B\bar{C}$

$\bar{A}(\bar{B}C + B\bar{C}) + A(\bar{B}\bar{C} + B \cdot C)$

$\bar{A}(\overset{B \oplus C}{\cancel{BC + B\bar{C}}}) + A(\overline{\cancel{B \oplus C}})$

$= \bar{A} \oplus B \oplus C$

~~Full adder with half adder~~

Half subtractor

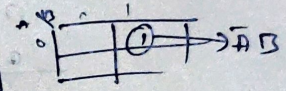
half subtraction is subtraction of 2 single bits.

No. of i/p = 2

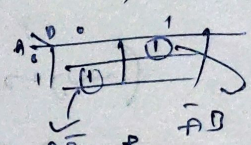
No. of op = 2 (borrow, diff).

	A	B	borrow	difference
0	0	0	0	0
1	0	1	1	1
2	1	0	0	1
3	1	1	0	0

borrow (A,B) = Σm (1)



diff (A,B) = Σm (1,2)



$\boxed{A \oplus B}$

Full subtractor

→ subtracts 3 bits.

I/p = 3

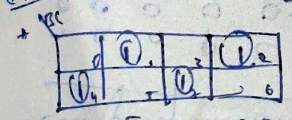
O/p = 2 (diff, borrow)

	A	B	C	borrow	diff
0	0	0	0	0	0
1	0	0	1	1	1
2	0	1	0	1	1
3	0	1	1	1	0
4	1	0	0	0	1
5	1	0	1	0	0
6	1	1	0	0	0
7	1	1	1	1	1

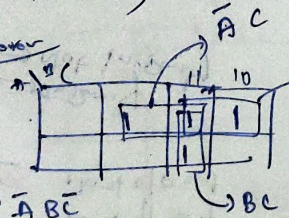
diff (A,B,C) = Σm(1, 2, 4, 7)

borrow (A,B,C) = Σm(1, 2, 3, 7)

diff



borrow



$A\bar{B}\bar{C} + \bar{A}\bar{B}C + A\bar{B}\bar{C} + \bar{A}B\bar{C}$

$A(B \oplus C) + \bar{A}(B \oplus C)$ = $A \oplus B \oplus C$

$\bar{A}C + \bar{A}B + BC$

$\bar{A}C + B(\bar{A}+C)$

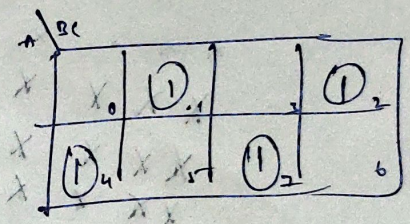
Even Parity generator for 3 bits

I/p = 3

O/p = 1

	A	B	C	P
0	0	0	0	0
1	0	0	1	1
2	0	1	0	1
3	0	1	1	0
4	1	0	0	1
5	1	0	1	0
6	1	1	0	0
7	1	1	1	1

$\Sigma p(A,B,C) = \Sigma m(1, 2, 4, 7)$



$A \oplus B \oplus C$

Even Parity checker

No. of i/p = 4
No. of o/p = 1

	A	B	C	D	P
0	0	0	0	0	0 → In Parity
1	0	0	0	1	1 → Not in Parity
2	0	0	1	0	1
3	0	0	1	1	0
4	0	1	0	0	1
5	0	1	0	1	0
6	0	1	1	0	0
7	0	1	1	1	1
8	1	0	0	0	1
9	1	0	0	1	0
10	1	0	1	0	0
11	1	0	1	1	1
12	1	1	0	0	0
13	1	1	0	1	1
14	1	1	1	0	1
15	1	1	1	1	0

$Y(A,B,C,D)$

$= \Sigma m(1,2,4,7,8,11,13,14)$

0	1	3	1
1	5	1	6
12	1	15	1
1	9	1	10

$A \oplus B \oplus C \oplus D$.

BCD to Ex-3 Converter

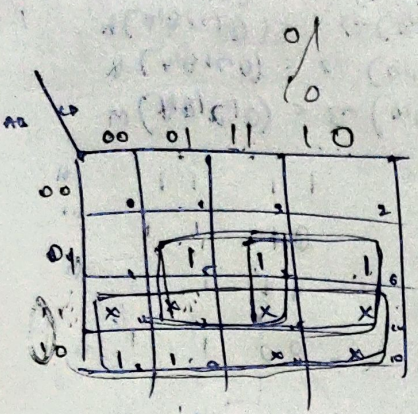
	A	B	C	D	P	Q	R	S
0	0	0	0	0	0	0	1	1
1	0	0	0	1	0	1	0	0
2	0	0	1	0	0	1	0	1
3	0	0	1	1	0	1	1	0
4	0	1	0	0	0	1	1	1
5	0	1	0	1	1	0	0	0
	0	1	1	0	1	0	0	1
	0	1	1	1	1	0	1	0
	1	0	0	0	1	0	1	1
	1	0	0	1	1	1	0	0
	1	0	1	0	X	X	X	X
	1	0	1	1	X	X	X	X
	1	1	0	0	X	X	X	X
	1	1	0	1	X	X	X	X
	1	1	1	0	X	X	X	X
	1	1	1	1	X	X	X	X

$P(A,B,C,D) = \Sigma m(5,6,7,8,9) + \Sigma d(10,11,12,13,14,15)$

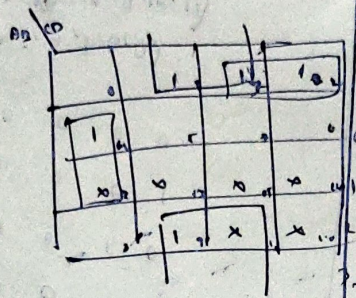
$Q(A,B,C,D) = \Sigma m(1,2,3,4,9) + \Sigma d(10,11,12,13,14,15)$

$R(A,B,C,D) = \Sigma m(0,3,4,7,8) + \Sigma d(10,11,12,13,14,15)$

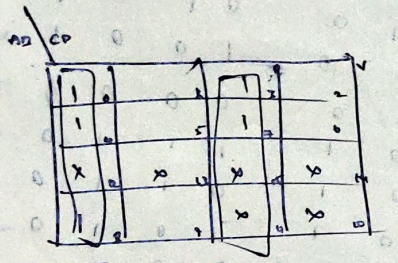
$S(A,B,C,D) = \Sigma m(0,2,4,6,8) + \Sigma d(10,11,12,13,14,15)$.



$A + BD + BC$

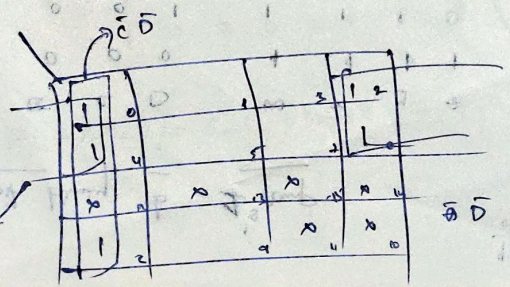


$\bar{B}A + B\bar{C}D + \bar{A}\bar{B}C$



$\bar{C}\bar{D}$ CD

$C \odot D$



$\bar{A}\bar{D} + \bar{C}\bar{D}$

2 Bit word Comparator

A (A_0A_1)	B (B_0B_1)	A<B	A=B	A>B
00	00	0	1	0
00	01	1	0	0
00	10	1	0	0
00	11	1	0	0
01	00	0	0	1
01	01	0	1	0
01	10	1	0	0
01	11	1	0	0
10	00	0	0	1
10	01	0	0	1
10	10	0	1	0
10	11	1	0	0
11	00	0	0	1
11	01	0	0	1
11	10	0	0	1
11	11	0	1	0

$A<B(A_0A_1, B_0B_1) = \Sigma m(1,2,3,6,7,9,14)$

$A=B(A_0A_1, B_0B_1) = \Sigma m(0,5,10,15)$

$A>B(A_0A_1, B_0B_1) = \Sigma m(4,8,9,12,13,14)$

4 bit binary to 1's comp

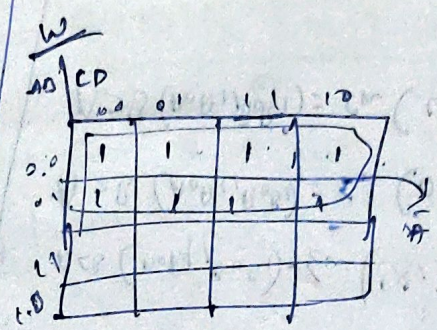
	A	B	C	D	w	x	y	z
0	0	0	0	0	1	1	1	1
1	0	0	0	1	1	1	1	0
2	0	0	1	0	1	1	0	1
3	0	0	1	1	1	1	0	0
4	0	1	0	0	1	0	1	1
5	0	1	0	1	1	0	1	0
6	0	1	1	0	1	0	0	1
7	0	1	1	1	1	0	0	0
8	1	0	0	0	0	1	1	1
9	1	0	0	1	0	1	1	0
10	1	0	1	0	0	1	0	1
11	1	0	1	1	0	1	0	0
12	1	1	0	0	0	0	1	1
13	1	1	0	1	0	0	1	0
14	1	1	1	0	0	0	0	1
15	1	1	1	1	0	0	0	0

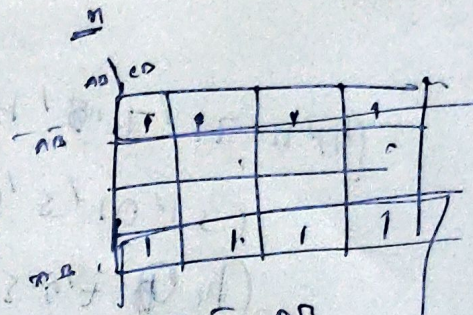
$w(A,B,C,D) = \Sigma m(0,1,2,3,4,5,6,7)$

$x(A,B,C,D) = \Sigma m(0,1,2,3,8,9,10,11)$

$y(A,B,C,D) = \Sigma m(0,1,4,5,8,9,12,13)$

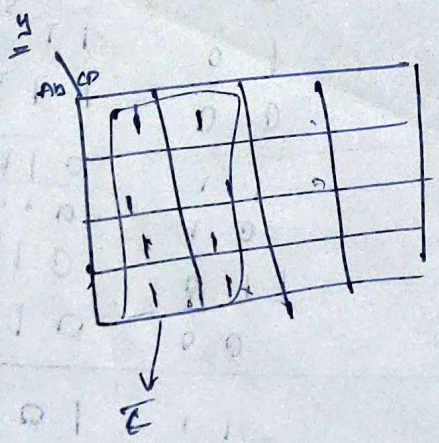
$z(A,B,C,D) = \Sigma m(0,2,4,6,8,10,12,14)$

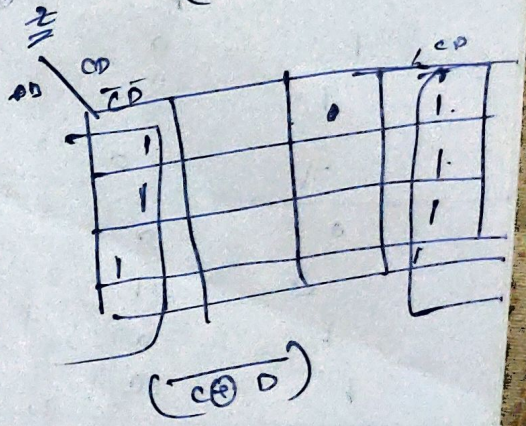




$\bar{A}\bar{B} + AB$

$= \overline{(A \oplus B)}$





$(C \oplus D)$

4 bit 2's Compliment

	A	B	C	D	P	Q	R	S
0	0	0	0	0	0	0	0	0
1	0	0	0	1	1	1	1	1
2	0	0	1	0	1	1	1	0
3	0	0	1	1	1	1	0	1
4	0	1	0	0	1	1	0	0
5	0	1	0	1	0	1	1	0
6	0	1	1	0	0	1	1	1
7	0	1	1	1	1	0	0	0
8	1	0	0	0	1	0	0	1
9	1	0	0	1	P	0	1	0
10	1	0	1	0	1	0	1	1
11	1	0	1	1	1	1	0	0
12	1	1	0	0	1	1	0	1
13	1	1	0	1	1	1	1	0
14	1	1	1	0	1	1	1	1
15	1	1	1	1	0	0	0	0

$P(A,B,C,D) = \Sigma m(1,2,3,4,7,8,9,10,11,12,13,14)$

1110
1
1111

0000
1111
1

10000

1110
1
1011
1
1110

10000

4 bit 2's Compliment

	A	B	C	D	P	Q	R	S
0	0	0	0	0	0	0	0	0
1	0	0	0	1	1	1	1	1
2	0	0	1	0	1	1	1	0
3	0	0	1	1	1	1	0	1
4	0	1	0	0	1	1	0	0
5	0	1	0	1	1	0	1	1
6	0	1	1	0	1	0	1	0
7	0	1	1	1	1	0	0	1
8	1	0	0	0	1	0	0	0
9	1	0	0	1	0	1	1	1
10	1	0	1	0	0	1	1	0
11	1	0	1	1	0	1	0	1
12	1	1	0	0	0	1	0	0
13	1	1	0	1	0	0	1	1
14	1	1	1	0	0	0	1	0
15	1	1	1	1	0	0	0	1

1 0000

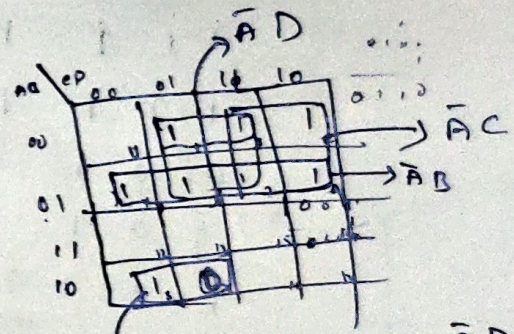
$P(A,B,C,D) = \Sigma m(1,2,3,4,5,6,7,8)$

0111
1
1000

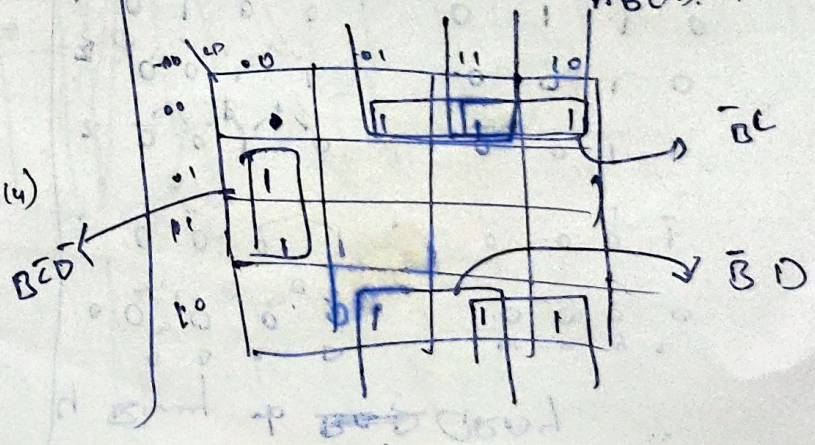
$Q(A,B,C,D) = (1,2,3,4,9,10,11,12)$

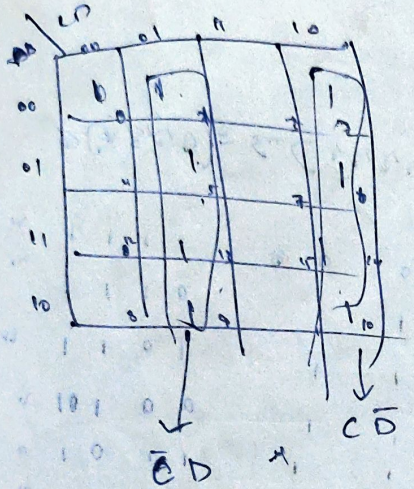
$R(A,B,C,D) = (1,2,5,6,9,10,13,14)$

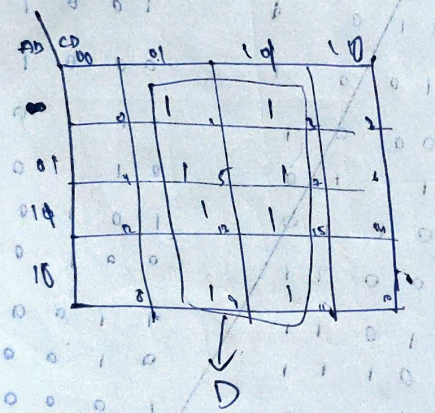
$S(A,B,C,D) = (1,3,5,7,9,11,13,15)$



$A\bar{B}\bar{C}\bar{D} + \bar{A}B + \bar{A}C + \bar{A}D$







4 Binary to ~~Bcd~~ GRAY

	A	B	C	D	W	X	Y	Z
0	0	0	0	0	0	0	0	0
1	0	0	0	1	0	0	0	1
2	0	0	1	0	0	0	1	1
3	0	0	1	1	0	0	1	0
4	0	1	0	0	0	1	1	0
5	0	1	0	1	0	1	1	1
6	0	1	1	0	0	1	0	1
7	0	1	1	1	0	1	0	0
8	1	0	0	0	1	1	0	0
9	1	0	0	1	1	1	0	1
10	1	0	1	0	1	1	1	1
11	1	0	1	1	1	1	1	0
12	1	1	0	0	1	0	1	0
13	1	1	0	1	1	0	1	1
14	1	1	1	0	1	0	0	1
15	1	1	1	1	1	0	0	0

$W = \Sigma m(8, 9, 10, 11, 12, 13, 14, 15)$

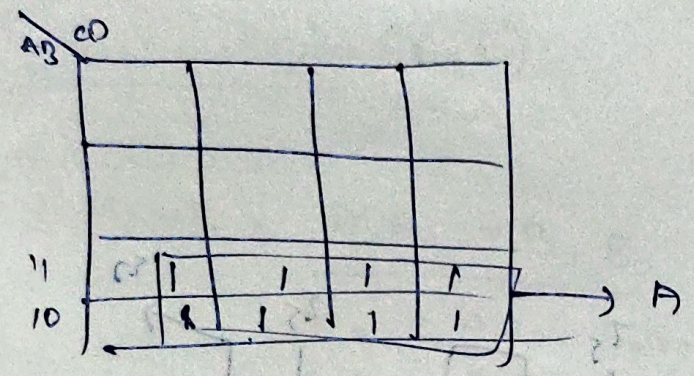
$X = \Sigma m(4, 5, 6, 7, 8, 9, 10, 11)$

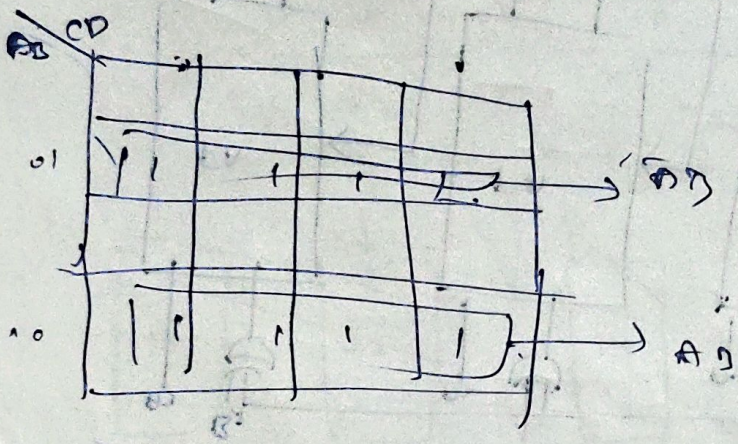
$Y = \Sigma m(2, 3, 4, 5, 10, 11, 12, 13)$

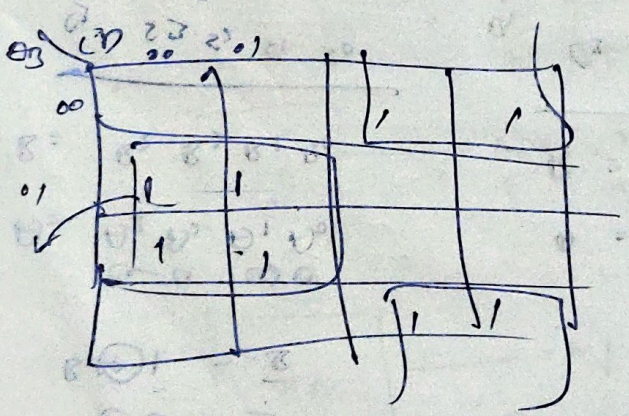
$Z = \Sigma m(1, 2, 5, 6, 9, 10, 13, 14)$

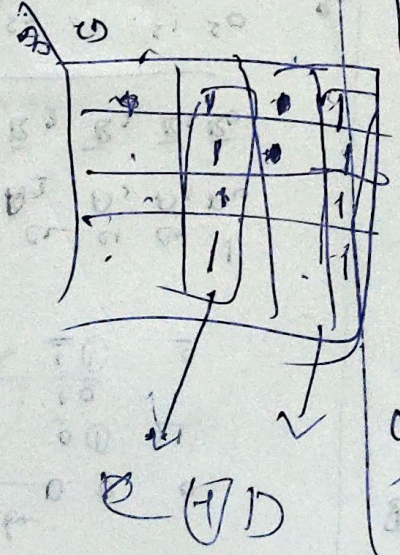
00 = 0
11 = 0
01 = 1
10 = 1

T
00 — 0
11 — 0
01 — 1
10 — 1

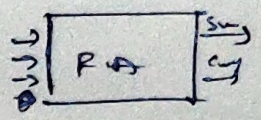








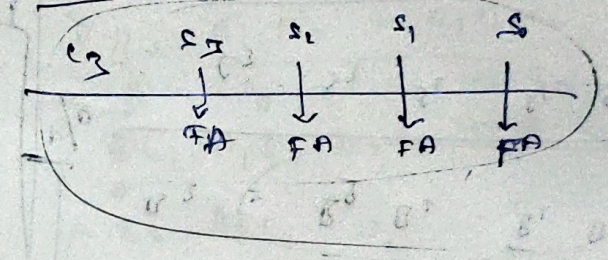
4 bit binary adder

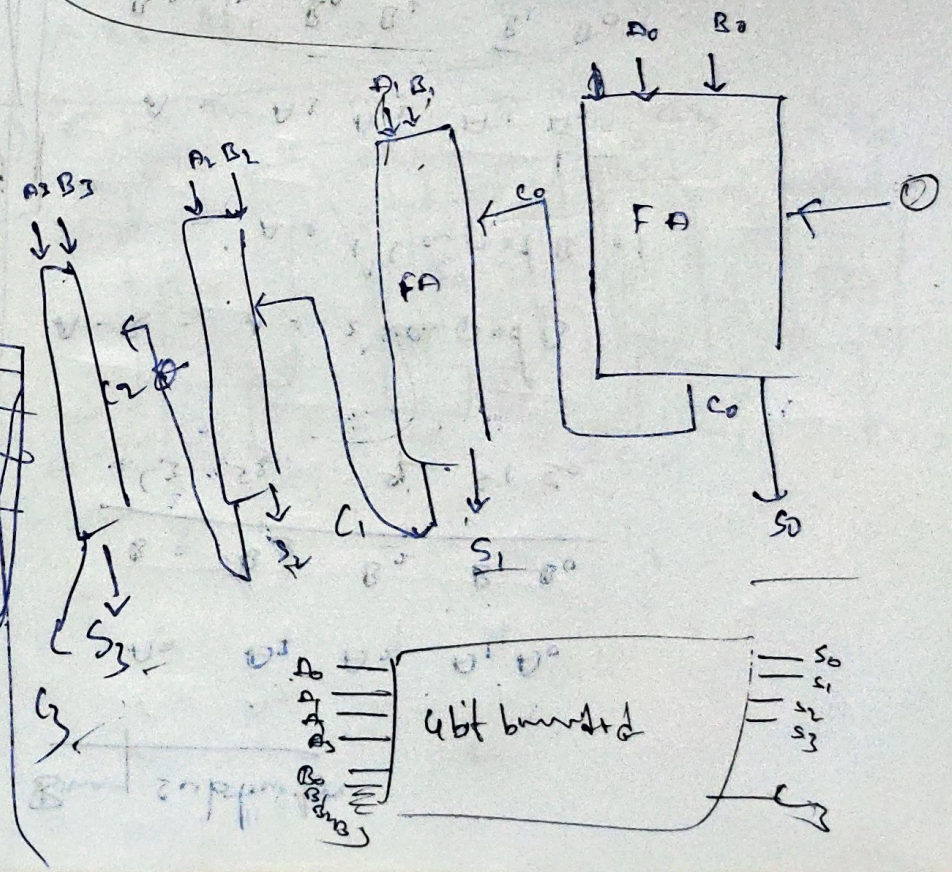


$C_4 \quad C_3 \quad C_2 \quad C_1 \quad C_0 \quad 0$

$A = A_3 \quad A_2 \quad A_1 \quad A_0$

$B = B_3 \quad B_2 \quad B_1 \quad B_0$





Design 4 bit binary adder & subtractor

$B \oplus 0 = B$

$B \oplus 1 = \bar{B}$

0	0	0
0	1	1
1	0	1
1	1	0

$A = A_3\ A_2\ A_1\ A_0$

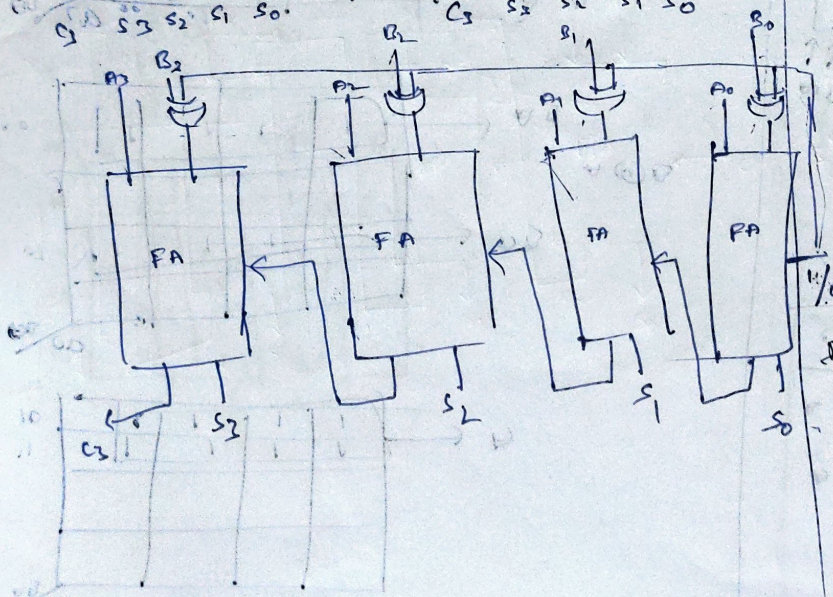
$B = B_3\ B_2\ B_1\ B_0$

$C_3\ S_3\ S_2\ S_1\ S_0$

$A = A_3\ A_2\ A_1\ A_0$

$B = \bar{B}_3\ \bar{B}_2\ \bar{B}_1\ \bar{B}_0$

$C_3\ S_3\ S_2\ S_1\ S_0$



Binary subtractor

$A = A_3\ A_2\ A_1\ A_0$

$B = B_3\ B_2\ B_1\ B_0$

$C_3\ S_3\ S_2\ S_1\ S_0$

$A - B = A$ + 2's comp of B

$= A$ + 1's comp of B + 1

$A = A_3\ A_2\ A_1\ A_0$

$B_3 = \bar{B}_3\ \bar{B}_2\ \bar{B}_1\ \bar{B}_0$

$A - B = C_3\ S_3\ S_2\ S_1\ S_0$

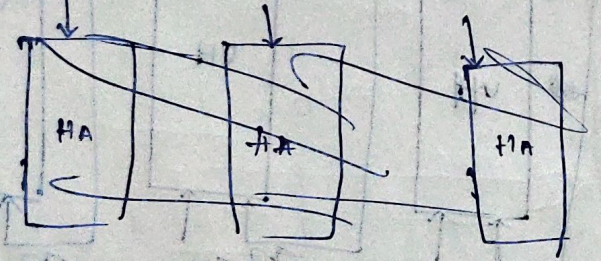
Binary multiplier (2 x 2)

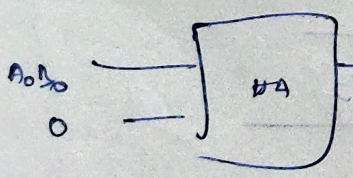
$A \times B = A_1A_0 \times B_1B_0$

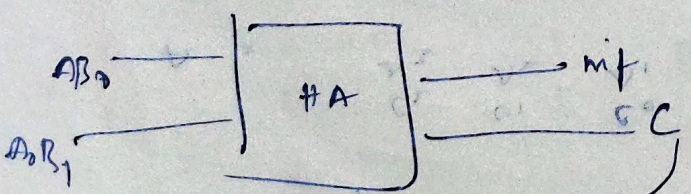
$C_0 \quad A_1B_0 \quad A_0B_0$

$A_1B_1 \quad A_0B_1 \quad 0$

$C_1 \quad m_2 \quad m_1 \quad m_0$







2 x 3 multiplier

$A = A_1A_0$

$B = B_2B_1B_0$

~~$B_2B_1B_0 \times A_1A_0$~~

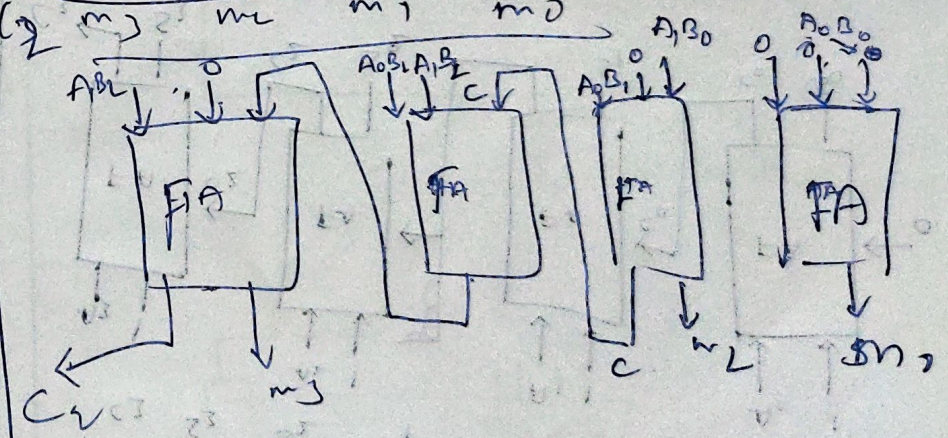
$A_1A_0 \times B_2B_1B_0$

$C_0 \quad A_1B_0 \quad A_0B_0$

$C_1 \quad A_1B_1 \quad A_0B_1 \quad 0$

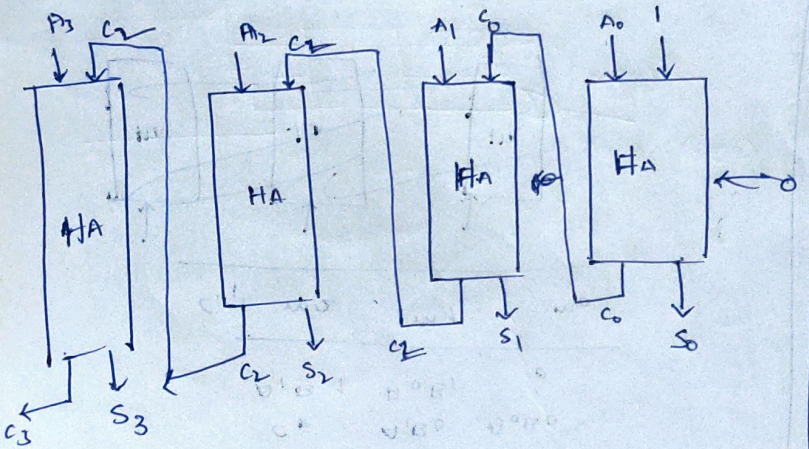
$A_1B_2 \quad A_0B_2 \quad 0 \quad 0$

$C_2 \quad m_3 \quad m_2 \quad m_1 \quad m_0$



4-bit binary incrementor:

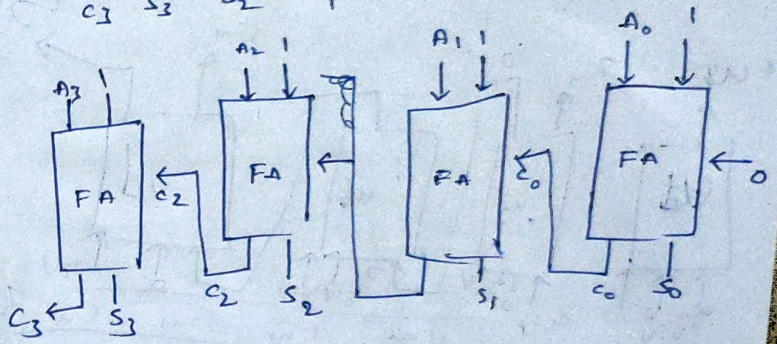
	C_2	C_1	C_0	
A =	A_3	A_2	A_1	A_0
	0	0	0	1
C_3	S_3	S_2	S_1	S_0



4 bit binary decrementor.

0001

	C_2	C_1	C_0	0
A	A_3	A_2	A_1	A_0
+	1	1	1	1 → 2's com
C_3	S_3	S_2	S_1	S_0

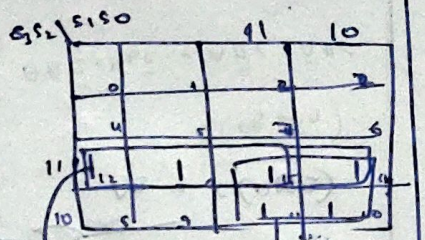


BCD Add^n / Decimal Add^n

	S_3	S_2	S_1	S_0	Validity ($S_3S_2 + S_3S_1$)
0	0	0	0	0	0
1	0	0	0	1	0
2	0	0	1	0	0
3	0	0	1	1	0
4	0	1	0	0	0
5	0	1	0	1	0
6	0	1	1	0	0
7	0	1	1	1	0
8	1	0	0	0	0
9	1	0	0	1	0
10	1	0	1	0	1
11	1	0	1	1	1
12	1	1	0	0	1
13	1	1	0	1	1
14	1	1	1	0	1
15	1	1	1	1	1

Σ Invalid (S_3, S_2, S_1, S_0)

$= \Sigma(10, 11, 12, 13, 14, 15)$

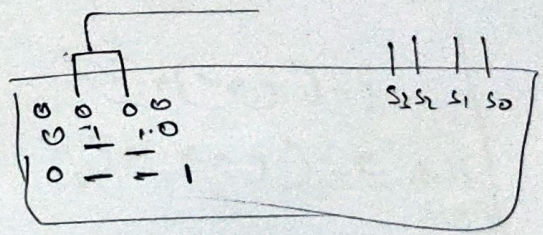


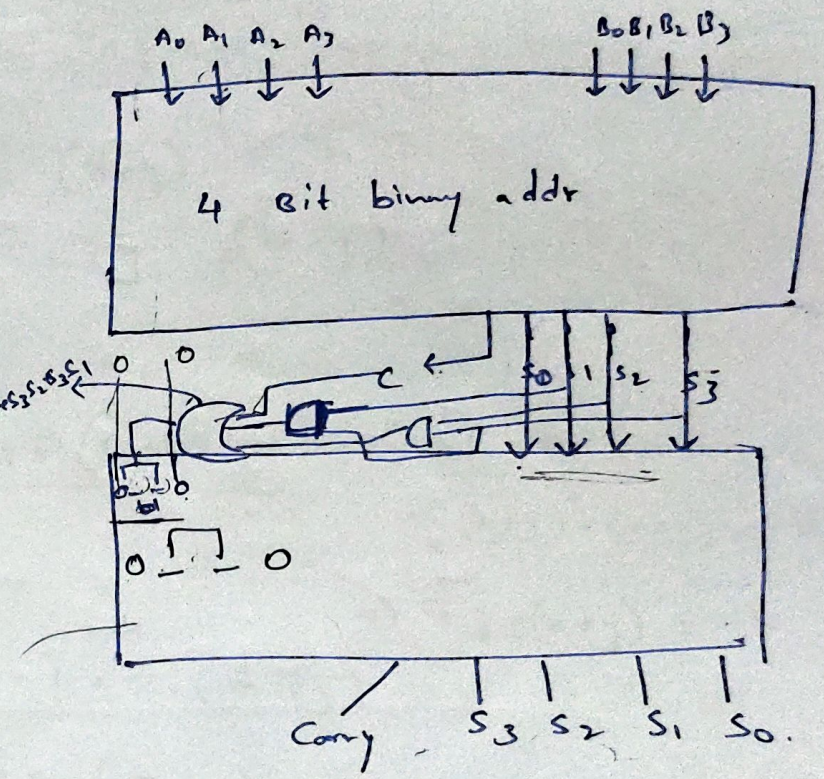
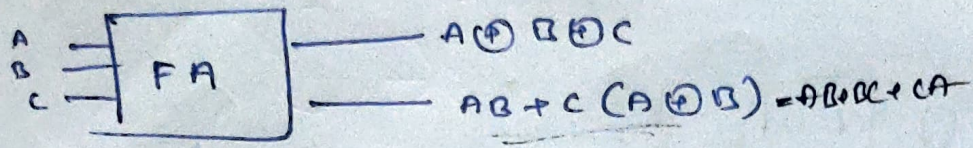
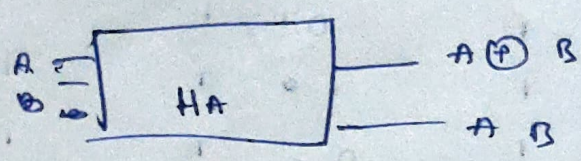
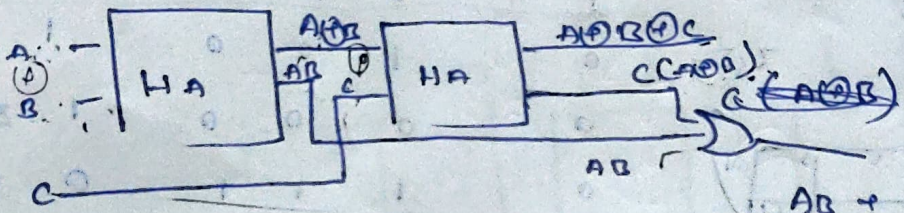
S_3S_2

S_3S_1

$S_3S_2 + S_3S_1 = 0$

$= 1$

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