Code No: R1622054 **R16** SET - 1

II B. Tech II Semester Model Examinations, March 2018
Computer Organization

Time: 3 hours Max. Marks: 70

Note: 1. Question Paper consists of two parts (**Part-A** and **Part-B**)
2. Answer **ALL** the question in **Part-A**
3. Answer any **THREE** Questions from **Part-B**

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PART –A

1. a) Perform the following subtractions in the binary number system, using 2's complements : (i) 1111 – 110 (ii) 1110 – 1100 (4M)
   b) Differentiate between Micro operation and Macro Operation with an example (4M)
   c) "Instruction Set Architecture has impact on the processors micro architecture" – support this statement with proper reasoning. (3M)
   d) Differentiate Micro programmed control and Hardwired control. (4M)
   e) What is the impact of the cache on overall performance of the computer? (3M)
   f) What do you understand by the term peripheral? Explain with some examples (4M)

PART -B

2. a) Explain different functional units of a digital computer with neat sketch. (8M)
   b) Discuss the advantages, disadvantages, and applications of (8M)
   i) Excess – 3 code ii) Gray Code
   (Illustrate with one example each)

3. a) Explain memory reference instructions with an example each. (8M)
   b) Write short note on i) BUN ii) BSA iii) ISZ (8M)

4. a) What do you mean by addressing mode? Explain the following addressing modes with examples. (8M)
   i) Index addressing mode ii) Relative addressing mode
   b) Explain clearly the three types of CPU organizations with examples (8M)

5. a) Perform floating point addition using the numbers 0.5 and 0.4375 use the floating point addition algorithm. (8M)
   b) Explain the multiplication of positive numbers using array multiplier with a neat sketch. (8M)

6. a) What is virtual memory? With the help of neat sketch explain the method of virtual to physical address translation. (8M)
   b) Explain the READ and WRITE operations in Associative Memory (8M)

7. a) Draw the block diagram of a DMA controller and explain its functioning? (10M)
   b) Discuss any five key differences between subroutine and interrupt service routines (6M)
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Code No: R1622054 **R16** SET - 2

II B. Tech II Semester Model Examinations, March 2018

Computer Organization

Time: 3 hours Max. Marks: 70

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2. Answer **ALL** the question in **Part-A**
3. Answer any **THREE** Questions from **Part-B**

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PART –A

1. a) "2's complement approach is preferable than sign magnitude for representing the fixed point numbers" – Justify this statement (3M)
   b) What are the functionalities of program counter, instruction register and data register? (3M)
   c) Explain the need of some bits of current microinstruction to generate address of the next microinstruction with an example. (4M)
   d) Perform the arithmetic operations below with binary numbers and with negative numbers in signed 2's complement. Use seven bit to accommodate each number together with its sign. i) -35 + -40 ii) -35 + +40 (4M)
   e) Differentiate between static RAM and dynamic RAM (4M)
   f) Distinguish between synchronous data transfer and asynchronous data transfer. (4M)

PART -B

2. a) Perform the following: (8M)
   i) $(110.101)_2 = (\ )_{10}$ ii) $(1.10101)_2 = (\ )_{10}$
   iii) $(11010.1)_2 = (\ )_{10}$ iv) 110.10 x 10.1
   b) Discuss various generations of computer with the technological features and devices that characterized each generation (8M)

3. a) Distinguish between circular shift and arithmetic shift with proper example. (8M)
   b) Explain the design of accumulator logic. (8M)

4. a) Distinguish the characteristics of RISC and CISC (8M)
   b) Explain the three basic types of data manipulation instructions. (8M)

5. a) Given signed decimal number +86 and -17. Perform (using 8 – bit representation) (8M)
   i) 2's complement Addition ii) 2's complement Subtraction
   b) Explain the steps for Floating Point Multiplication with neat diagram and suitable example. (8M)

6. a) Draw a neat block diagram of memory hierarchy in a computer system. Compare the parameters size, speed and cost per bit in the hierarchy. (8M)
   b) Explain ROM and RAM with respect to their block diagrams (8M)

7. a) Explain in detail on i) Vectored Interrupt ii) Interrupt Nesting (8M)
   b) Discuss on the following with neat sketches (8M)
   i) Time – Shared Common bus ii) Multistage Switching Network
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Code No: R1622054 **R16** SET - 3

II B. Tech II Semester Model Examinations, March 2018

Computer Organization

Time: 3 hours Max. Marks: 70

Note: 1. Question Paper consists of two parts (**Part-A** and **Part-B**)
2. Answer **ALL** the question in **Part-A**
3. Answer any **THREE** Questions from **Part-B**

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PART –A

1. a) Convert the following decimal numbers to the bases indicated (4M)
   i) 9872 to octal ii) 4689 to hexadecimal
   b) What is the use of buffers? Explain about tri-state buffers. (3M)
   c) Explain how different instruction formats influence the system. (4M)
   d) Explain the concept of partial remainder (4M)
   e) List and explain the advantages of virtual memory. (3M)
   f) Distinguish isolated and memory mapped I/O (4M)

PART -B

2. a) What is a bus? Explain single bus and multiple bus structure used to interconnect functional units in the computer system. (8M)
   b) Distinguish between error detection and error correction. Explain with an example how Hamming code is used for error detection. (8M)

3. a) Explain the following with respect to logic micro operations (8M)
   i) Selective Set ii) Selective Complement
   iii) Selective Clear iv) Mask
   b) Explain various computer instruction formats with neat sketches (8M)

4. a) Draw and explain the micro-programmed control unit. (8M)
   b) Explain various types of interrupts in detail. (8M)

5. a) Perform the restoring division for the binary numbers 1010 and 11. Draw the circuit arrangement for binary division. (8M)
   b) What are the steps involved in the addition of 2's complement notation. Explain with an example. 8M

6. a) A computer system has a MM capacity of a total of 1M 16 bits words. It also has a 4K words cache organized in the block set associative manner, with 4 blocks per set & 64 words per block. Calculate the number of bits in each of the TAG, SET & WORD fields of MM address format. (8M)
   b) Explain the following (8M)
   i) Memory management using segmentation
   ii) Memory management using paging

7. a) Explain in detail i) Interrupt ii) An exception with an example (8M)
   b) Differentiate serial arbitration logic and parallel arbitration logic with neat sketches (8M)
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Code No: R1622054 **R16** SET - 4

II B. Tech II Semester Model Examinations, March 2018

Computer Organization

Time: 3 hours Max. Marks: 70

Note: 1. Question Paper consists of two parts (**Part-A** and **Part-B**)
2. Answer **ALL** the question in **Part-A**
3. Answer any **THREE** Questions from **Part-B**

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PART –A

1. a) Convert the number $(5675)_8$ into its decimal and hexadecimal (4M)
   b) Discuss on RTL with suitable example. (4M)
   c) What do you understand by register stack and memory stack? (3M)
   d) Discuss the advantages and disadvantages of micro programmed control unit. (3M)
   e) Define i) Memory access time ii) Memory cycle time (4M)
   f) Differentiate between tightly coupled systems and loosely coupled systems. (4M)

PART -B

2. a) Describe basic operational concepts of computer in detail (8M)
   b) "Parity checking can be used for error detection" – Justify your answer with an example. (8M)

3. a) Explain the following with neat sketches (8M)
   i) 4 – bit Binary adder ii) Binary Adder - Subtractor
   b) Explain various phases of instruction cycle with an example (8M)

4. a) Explain how registers are connected to common bus in the computer with a neat diagram. (8M)
   b) What do you mean by addressing mode? Explain the following addressing modes with examples. (8M)
   i) Direct Addressing Mode ii) Immediate Addressing Mode

5. a) Explain subtraction of binary numbers in one's complement notation with examples. (8M)
   b) Perform the following: (8M)
   i) $(110.101)_2 = (\ )_{10}$ ii) $(1.10101)_2 = (\ )_{10}$
   ii) 1010.01 x 11.1 iv) 110.10 x 10.1

6. a) Explain the following mapping techniques used for cache mapping (8M)
   i) Associative mapping cache ii)Direct mapping cache
   iii) Block-set-associative mapping cache
   b) Write short note on i) Magnetic Disks ii) Magnetic tapes (8M)

7. a) Explain the role of interrupts in Computer Organization. (8M)
   b) Discuss the following interconnection structures (8M)
   i) Crossbar Switch ii) Hypercube system
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