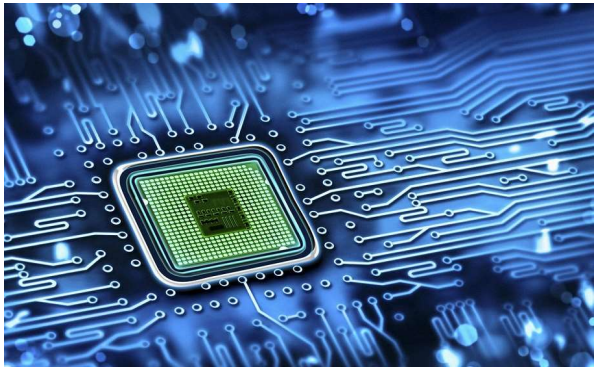
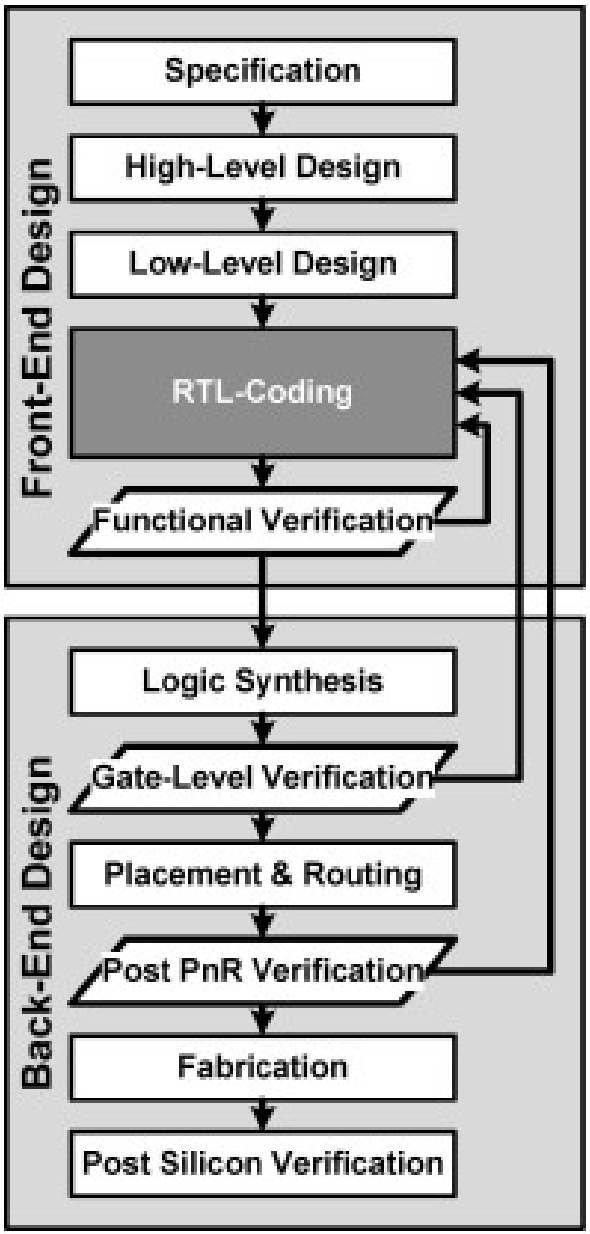
IC Design Flow





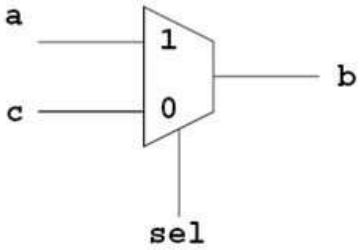
- Example:

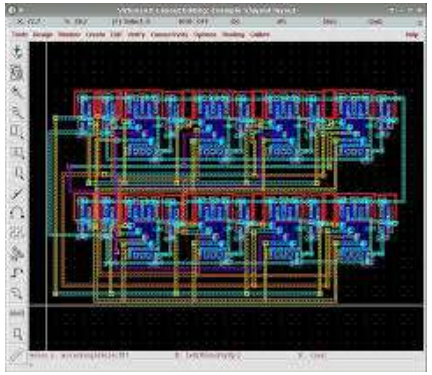
```
module mux2_1( b, a, c, sel) ;
  input     a, c, sel;
  output    b;

  wire      sel;
  wire      [3:0] a, b, c;

  assign b= (sel == 1)? a : c;

endmodule
```





Specification

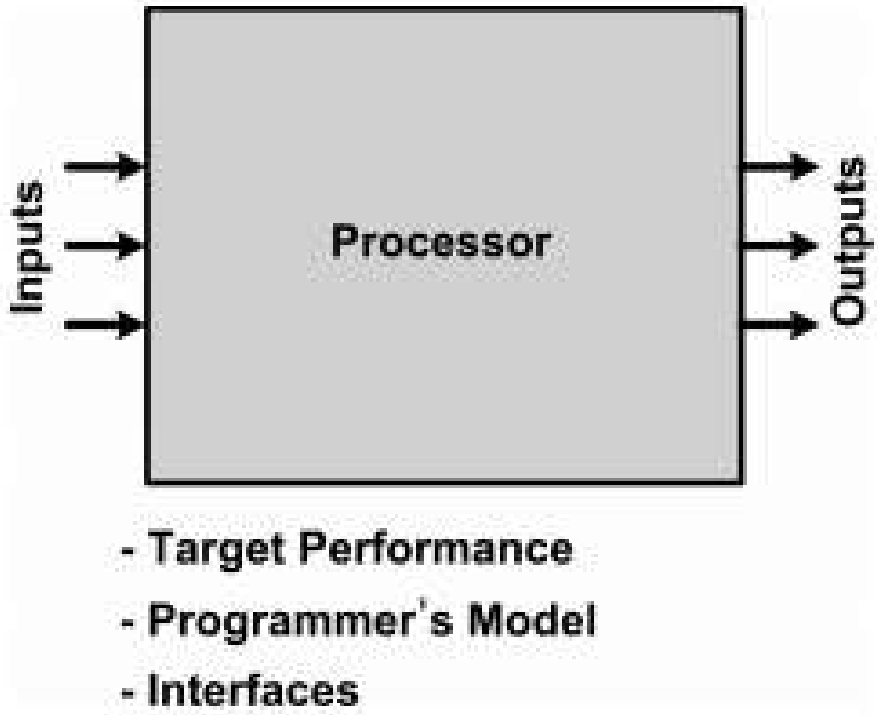


Figure A.2 Specification

High-level design

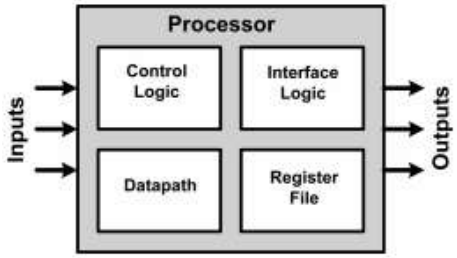


Figure A.3 High-level design

Low-level design

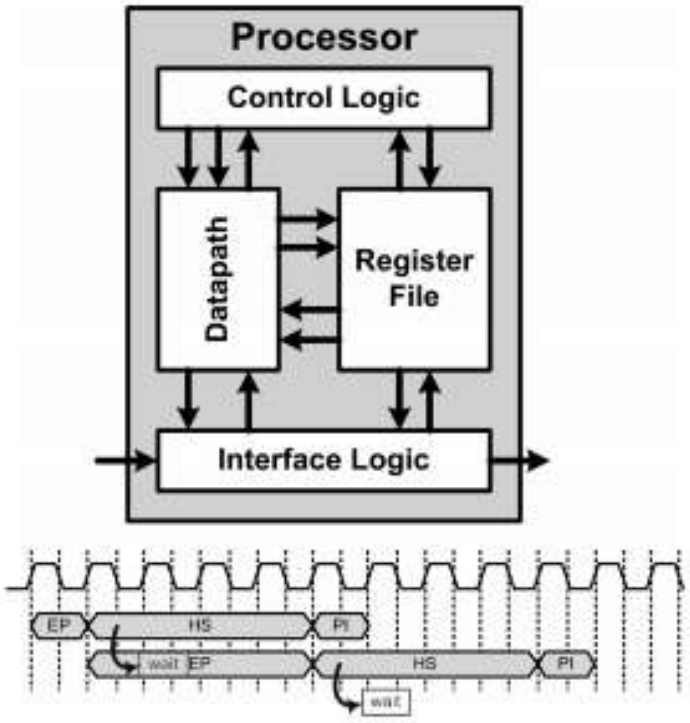


Figure A.4 Low-level design

RTL coding

```
module processor( clk,      //Clock
                  reset     //Reset
                  inputs;
                  outputs);
      input clk;
      input reset;
      input inputs;
      output      outputs

      controller        proc_ctrl(clk, reset, signals)
      datapath          proc_dp(clk, reset, signals)
      registerfile      proc_rf(clk, reset, signals)
      interfaces        proc_if(clk, reset, signals)
endmodule
```

Simulation

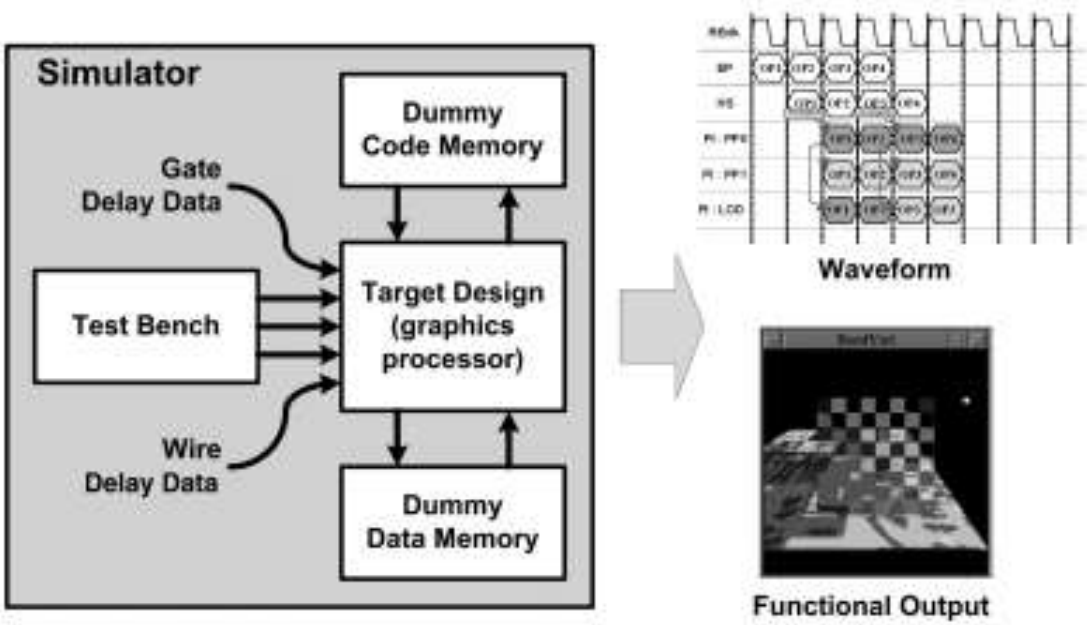


Figure A.5 Simulation

Synthesis

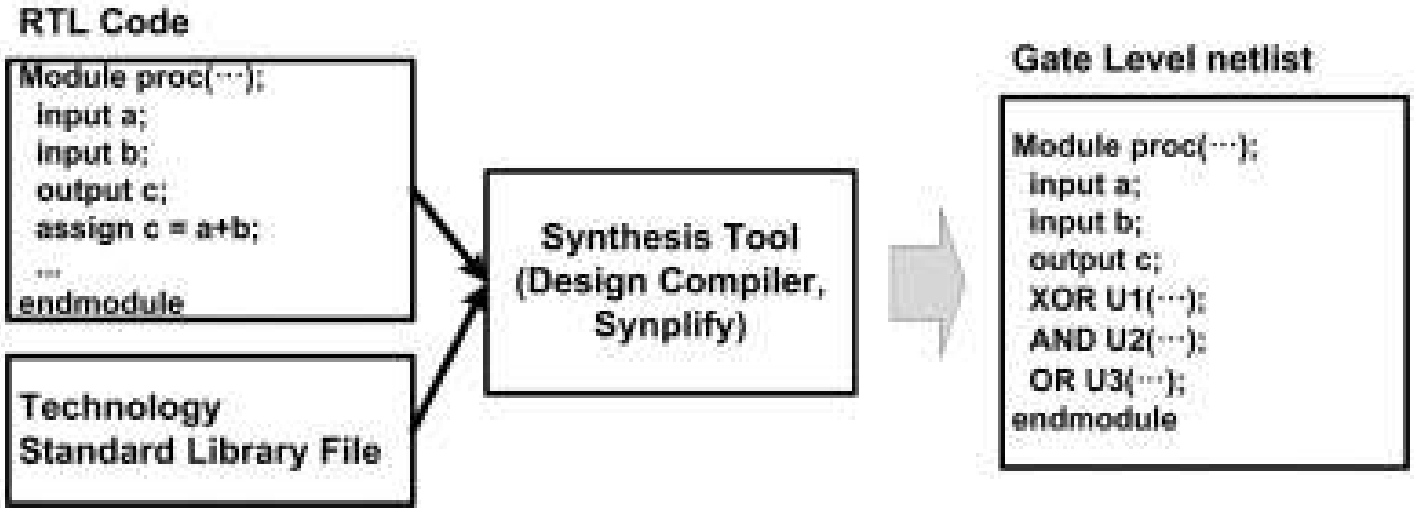


Figure A.6 Synthesis

Placement and routing

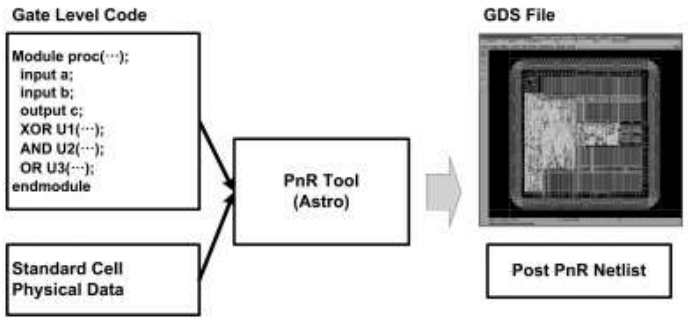


Figure A.7 Placement and routing

What is Verilog HDL ?

- Hardware description language
- Mixed level modeling
  - Behavioral
    - Algorithmic
    - Register transfer
  - Structural
    - Gate
    - Switch
- Single language for design and simulation
- Built-in primitives and logic functions
- User-defined primitives
- Built-in data types
- High-level programming constructs