Irfu
Institut de recherche sur les lois fondamentales de l'Univers

DREAM, a Front End ASIC for CLAS12 detector

User Manual

Production Version, Document 3.0, January 14, 2014.

Authors: P. Baron; E. Delagnes; C. Flouzat; F. Guilloux

Revision history

Date	Revision	Changes
25-Sept-12	1.0	Document Creation
04-March-13	2.0	Value of functionality test capacitor: 500 fF instead of 100 fF
		Register 10 & 11: these 2 registers permit to select the SCA readout of the 64 channels if put to “1”
14-January-14	3.0	DC voltage of SCA and GAIN-2 input [Vref_sca]

A number of modifications have been made on this production version compared to the previous prototype version and are reported in Annexe 3 of this document.

Contents

1. Introduction

This document describes the DREAM (**D**ead-timeless **R**ead-out **E**lectronics **A**SIC for **M**icromégas) circuit developed to read the large Micromegas chambers of the CLAS12 experiment tracker. This ASIC performs the collection, the amplification, the filtering, the discrimination and the analogue storage of the detector signal in an analogue memory which is used as a Level 1 latency and derandomizing buffer. The sampled signals which have been marked by the trigger are read-out asynchronously without stopping the analog storage process allowing a "deadtime free" operation for trigger rates up to more than 20 kHz. These samples are serialized in order to be digitized by an external ADC. The architecture reuse previous developments made for the AFTER [ref.1] and AGET chips [ref.2] with significant new features and modifications.

1.1 DREAM general description

The ***DREAM*** chip includes 64 channels (**Fig. 1**) each handling one detector channel. A channel integrates mainly: a charge sensitive preamplifier, an analogue filter (shaper), a discriminator usable for trigger building and a 512-sample analog memory.

The charge sensitive preamplifier (CSA) gain is programmable to accommodate a dynamic range up going from 50 fC to 600 fC. This gain is selectable for each channel, by selecting one of the available CSA feedback capacitors (ASIC Slow Control).

The analog filter consists in a Pole Zero Cancellation stage followed by a 2-complex pole Sallen-Key low pass filter. The peaking time of the global filter is selectable among sixteen values in the range of 50 ns to 900 ns. The filtered signal is sent to both the analog memory and the discriminator inputs.

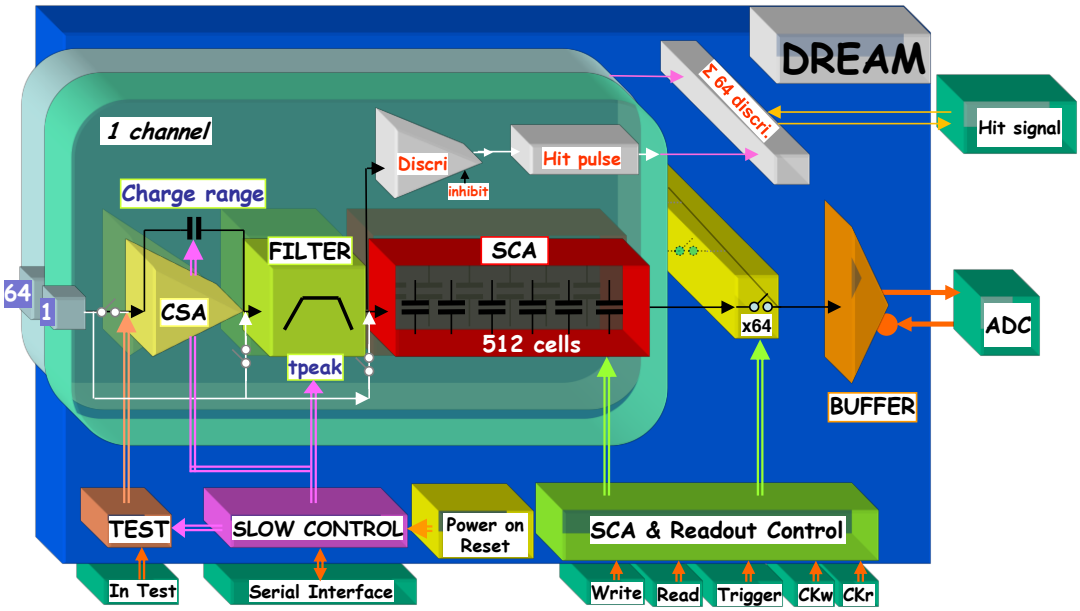


Fig. 1: Block diagram of the DREAM chip.

The analogue memory is based on a **S**witched **C**apacitor **A**rray structure (**SCA**), used as a 512 cell-depth circular buffer in which the analog signal coming out from the shaper is continuously sampled and stored. The sampling frequency is defined by ***WCk*** in the range of 1 MHz to 50 MHz. The analogue cells marked by the external trigger input signal (***Trig***) after a programmable fix latency are frozen waiting for readout, otherwise they are ready to be overwritten at the next cycle of the write pointer. Then, the oldest available frozen time slice is read on demand (initiated by the external ***Read*** signal). The analogue samples from the

enabled (by slow control) channels corresponding to the triggered time slice are successively multiplexed toward a differential driver designed to drive an external 12-bit ADC at a frequency up to 20 MHz (defined by ***RCk***). After readout, the cells from the triggered time slice are released and ready to be overwritten.

In parallel, the filtered signal is compared by a discriminator to a programmable threshold value set by a 7-bit (+1 polarity bit). This discriminator can be disabled channel by channel. A logical fast OR of the 64 channels is performed on-chip and sent using LVDS signal on ***Hitm*** & ***Hitp*** pads if the level of multiplicity is greater than a programmable value. The duration of this signal can be either an image of the time over threshold of the triggered signal either set to a fix value depending on the slow control.

A serial link, compatible with the SPI protocol, permits the configuration of the main chip parameters (e.g. gain, peaking time & test).

A chip input permits to calibrate or to test the channels.

For testability purposes, a “spy” mode is available to control some internal test points (CSA & PZC outputs; SCA & discriminator inputs) of the first analogue channel or to output the HIT signal and several debug modes are allowing the user to control some critical digital signals of the chip.

To cope with the various detector configurations, this ASIC can operate with the both signal polarities according to the adjustment of DC voltages inside the ASIC. It is also possible to bypass the internal CSA of the channel and to inject directly the input signals to the filter or SCA inputs.

1.2 DREAM requirements

The main requirements for the DREAM chip are summarized in the Table 1.

Parameter	Value
Polarity of detector signal	Negative or Positive
Number of channels	64
External Preamplifier option	Yes; access to the filter or SCA inputs
Charge measurement	
Input dynamic range/gain	50 fC; 100 fC; 200 fC; 600 fC, selectable per channel
Output dynamic range	2V p-p
I.N.L	< 2%
Charge Resolution	> 8 bits
Sampling	
Peaking time value	50 ns to 900 ns (16 values)
Number of SCA Time bins	512
Sampling Frequency (*WCk*)	1 MHz to 50 MHz
Triggering	
Discriminator solution	Leading edge
HIT signal	OR of the 64 discriminator outputs in LVDS level
Threshold Range	5% or 17.5% of the input dynamic range
I.N.L	< 5%
Threshold value	(7-bit + polarity bit) DAC common to all channels
Minimum threshold value	≥ noise
Readout	
Readout frequency	Up to 20 MHz
Channel Readout mode	all channels excepted those disabled (statically)
SCA cell Readout mode	Triggered columns only
Test	
Calibration (current input mode)	1 channel among 64; external test capacitor
Test (voltage input mode)	1 channel among 64; internal test capacitor (1/charge range)
Functional (voltage input mode)	1, few or 64 channels; internal test capacitor/channel
Trigger rate	Up to 20kHz (4 samples read/trigger).
Counting rate	< 50 kHz / channel
Power consumption	< 10 mW / channel

Table 1: Summary of the DREAM requirements.

2. Architecture of the front-end part of the channel

The architecture of the front-end part has been designed to match the noise requirements for the large Micromegas detectors foreseen for the CLAS12 tracker. It has been optimized to minimize the noise for relatively fast peaking times compatible with high particle rate. It takes into account the power consumption, occupancy and silicon area constraints and can also fit various configurations of detector parameters (gain, capacitor…), and can deal with the both detector signal (positive or negative) polarities.

2.1 General description

The front-end channel (**Fig. 2**) is made up of four stages:

- C.S.A: Charge Sensitive Amplifier,
- PZC: the pole-zero cancellation stage,
- R.C^2 filter: Sallen & Key filter,
- An inverting x2 Gain.

The parameters of the different stages are controlled by slow control, locally (at the channel level) or globally (at the ASIC level).

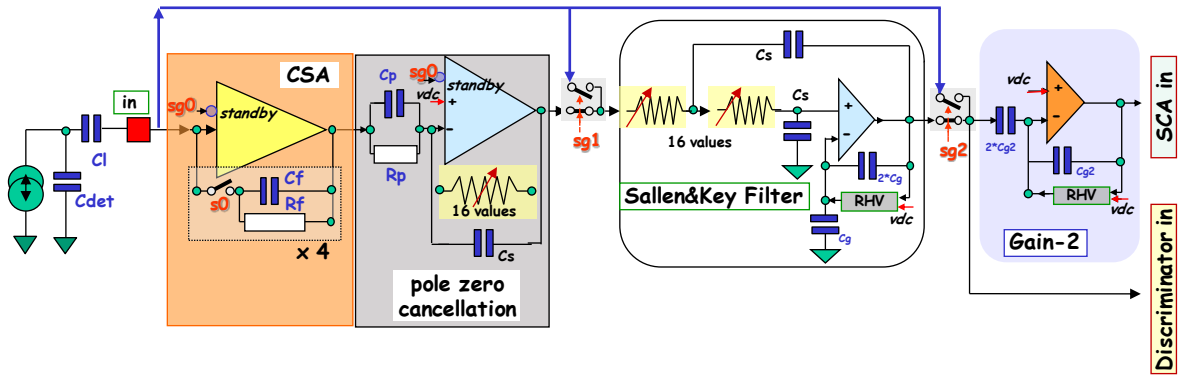


Fig. 2**:** Schematic of the front-end part of the analog channel.

The power supply, DC voltage and current references of the different stages are independent at the channel level and also at the ASIC level excepted for the inverting 2x Gain and the discriminator.

2.1.1 Channel input

In the nominal mode, the input signal goes through the input of the CSA (Charge Sensitive Amplifier). But by slow control, it is possible to switch the signal to the input of the SK filter or the inverting 2x Gain (state1<29:28>). In this case, the internal supply of the CSA and PZC filter will be cut off.

2.1.2 The Charge Sensitive Amplifier (CSA)

This amplifier is based on the single-ended folded cascode architecture. The input stage is formed by two complementary CMOS transistors (NMOS & PMOS) with gates connected together to the channel input. The input branch current is defined by an internal regulator common to 32 channels (2 regulators in chip), and controlled via slow control (state1<1:0>). This bias current choice (400

µA to 1.2mA) will be the result of a trade-off between the noise and power consumption performances that will depend on the application. The pads **101** & **124** (vreg_csad & vreg_csag) allow to filter the internal regulator voltages.

The CSA DC output voltage is defined internally and must be filtered externally through the pad **115** (vdc_csa). This DC value must be adapted, by slow control (state1<11>), to the polarity of the input signal. For the anode polarity (negative input current) 1.8V and 2.8 V for the other input polarity. The charge to voltage conversion (input charge range: 50 fC, 100 fC, 200 fC or 600 fC) is achieved by one of the feedback capacitors (CF) selected by Slow Control. This gain control is done channel by channel with two 64-bit slow control registers state6<63:0> & state7<63:0> (2 bits per channel).

The DC feedback (**Fig. 3**) of the CSA is achieved by an attenuating current conveyor (*AICON*). This current conveyor attenuates by a factor A the current flowing through the Ra resistor connected between the CSA output and the *AICON* input, so that it is equivalent to a resistor of high value Rf = A . (Ra + Rin), where Rin is the *AICON* input impedance. The Rf.Cf time constant can be set to 5µs, compatible with high rate operation, or 50 µs independently of the Gain (and therefore of Cf) value selected. The choice of the value is done by the bit state1<31>.

The maximum DC current that the CSA DC-feedback can source or sink to the detector is - 90 nA to + 30 nA (50 fC input charge range).

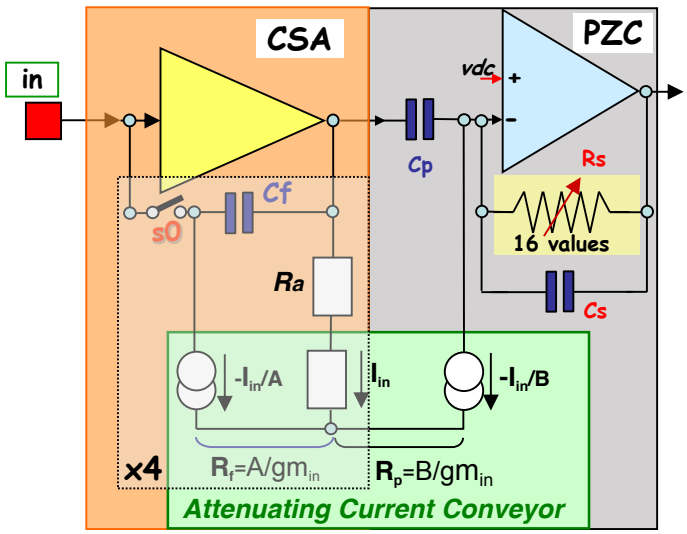


Fig. 3**:** Principle of the CSA DC feedback.

2.1.3 The Pole-Zero cancellation stage (PZC)

The PZC stage permits to avoid long duration undershoot at the shaped output due to the CSA main pole. It introduces a zero to cancel the low frequency pole of the CSA and replaces it by a higher frequency pole with a value selectable, via Slow Control (state1<7:4>), between sixteen possible values (25 ns to 0.45 µs).

The second branch of the CSA *AICON* (**Fig. 3**) is used to emulate the high value resistor (Rp) placed in parallel with the Cp to create a transmission zero cancelling the CSA pole. It is replaced by a new pole Rs.Cs defined by the feedback network of the stage that participates to the shaping.

The DC output voltage of this block is defined internally and must be filtered externally through the pad **114 (Vdc_c)**. This DC value must be adapted, by slow control (state1<11>), to the polarity of the input signal. For the anode polarity (negative input current) 2.2 V and 0.7 V for the other input polarity.

In the normal mode, the shaping time of the PZC and SK filter is the same and is controlled by the state1<7:4> bits. But it is possible to dissociate them by setting the state1<10> bit to “1”. In this condition, the shaping time of the PZC is fixed to **450 ns** independently of the 16 possible shaping time values of the SK filter, so that the channel behaves as an **integrator with 450ns decay time constant**.

2.1.4 The RC^2 filter (SK filter)

Associated with the previous PZC stage, this 2-complex pole Sallen-Key low pass filter provides a semi-Gaussian shaping of the analog channel. The filter damping factor is ξ = 0.75, so that the global filter response exhibits a 1% only undershoot.

The peaking time of the global filter is defined by switching different combinations of resistors on both the PZC and SK filter stages. The available range of peaking time extends from **50 ns** to **900 ns** (**sixteen values**). The DC output voltage of the filter is defined internally as for the PZC (pad **114**).

2.1.5 The inverting x2 Gain (G-2)

This stage provides an extra x2 inverting voltage gain and the necessary buffering for the signal sampling in the SCA. Its total dynamic (full range) is 1.5V, mainly limited by slew rate effects.

The DC output voltage of this block is defined internally and must be filtered externally through the pad **110** (**Vdc_g2**). This DC value must be adapted, by slow control (state1<11>), to the polarity of the input signal. For the anode polarity (negative input current) 0.7 V and 2.2 V for the other input polarity.

Its input common-mode voltage is defined internally and must be filtered externally through the pad **111** (**Vref_sca**). This pin is also used to supply the reference voltage of the SCA at a fixed value of 0.7V.

3. Discrimination channel

The discrimination channel is not useful for the CLAS12 experiment. Nevertheless, as it was existing in the AGET design, we have decided to keep it in a simplify version, considering it could be useful for detector testing or other experiments. But it has been considered that this channel is a “secondary functionality” and therefore all its specifications are considered also to be of secondary importance.

The event detection is performed by comparing the amplitude of the shaped signal (**Fig. 4**) to a programmable threshold value. The duration of the discriminator output signal as other parameters of the discriminator are defined by slow control.

The output signal of the shaping filter is first amplified and converted into a differential signal using amplifier (differential gain of 28 or 9) before the comparator in order to increase the discrimination sensitivity. It means that the dynamic range of the discriminator channel is only equal to **5 %** or **17.5 %** (state1<30>) of the input dynamic range of the main analog channel.

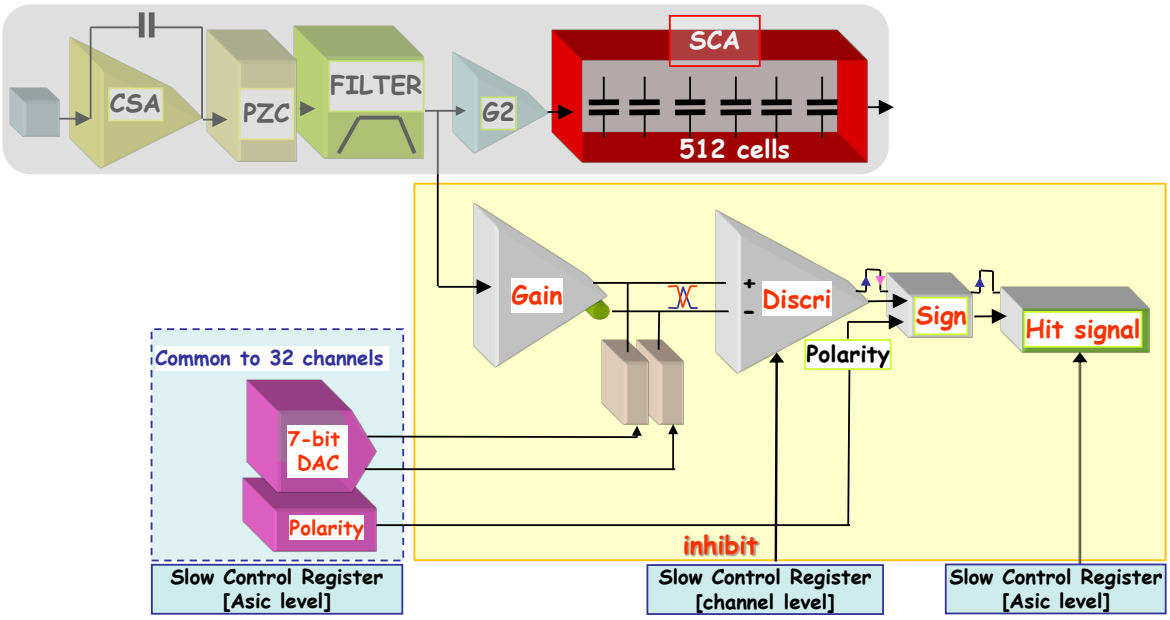


Fig. 4**:** block schematic of the analog channel.

The threshold value of the discriminator is controlled and adjusted using a 8-bit DAC (7-bit state1<20:14> plus 1 polarity bit state1<21>) common to all the channels. Actually for layout reasons, two DACS, each connected to 32 channels, but controlled by the same slow control bits are used. If the signal cross the threshold, the discriminator output signal is used to form with the 63 others discriminator signals the ***HIT*** signal (pads 60 & 61 **Hitp** & **Hitm**). The polarity bit is necessary to control the threshold and the logical output edge according to the polarity of the detector signal.

3.1 HIT signal

In each channel **i**, the ***HIT(i)*** signal provided by the discriminator is conditioned by several slow control parameters and signals as explained in this section. This signal is used to switch on or off a current source (**Fig. 5**) which is summed with the 63 others current sources to form the internal global ***HIT*** signal.

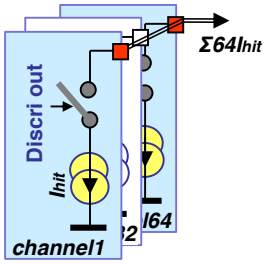


Fig. 5**:** block schematic of the channel HIT data.

3.1.1 Inhibition

The discriminator can be disabled (standby mode) channel by channel. The inhibition bits are gathered in two 32-bit registers (address 8 or 9 depending to the channel number) (see 7.6.I & 7.6.J).

3.1.2 Veto condition

It is also possible to inhibit multiple triggering of the comparator outputs (Hit(i)) during a time window of around **4 μs** [set by an analog ramp generator & comparator]. This veto condition is controlled by the state1<22> bit.

3.1.3 Duration of the Hit signal

The duration of the signal can be:

- The same of the one of discriminator output signal (Time over Threshold). This mode is controlled by the state1<23> bit.
- Chosen between two possible values: 100ns or 200ns. The choice is made by the state1<24> bit and enabled by setting the previous state1<23> bit to"0".

These durations are obtained using monostables, and therefore are subject to technology process variations. The 2 slow control bits state1<26:25> allow the control of these process variations (**Table 2**).

State1<26> Msb_HIT_width	State1<25> Lsb_HIT_width	Range_HIT_width="0"			Range_HIT_width="1"		
		wp	tm	ws	Wp	tm	ws
0	0	*61 ns*	*94 ns*	*128 ns*	*142 ns*	*218 ns*	*297 ns*
0	1	*50 ns*	*77 ns*	*106 ns*	*110 ns*	*170 ns*	*232 ns*
1	0	*72 ns*	*110 ns*	*150 ns*	*153 ns*	*235 ns*	*319 ns*
1	1	*83 ns*	*127 ns*	*171 ns*	*194 ns*	*298 ns*	*404 ns*

Table 2: the adjustment of the HIT signal width.
[wp for worst power case; tm for typical mean case; ws for worst speed case].

3.2 Global HIT signal

The summed current of the **HIT(i)** channel signals is converted into voltage signal (**Fig. 6**). This signal is compared to the threshold value controlled by 3-bit of slow control state2<27:25>.

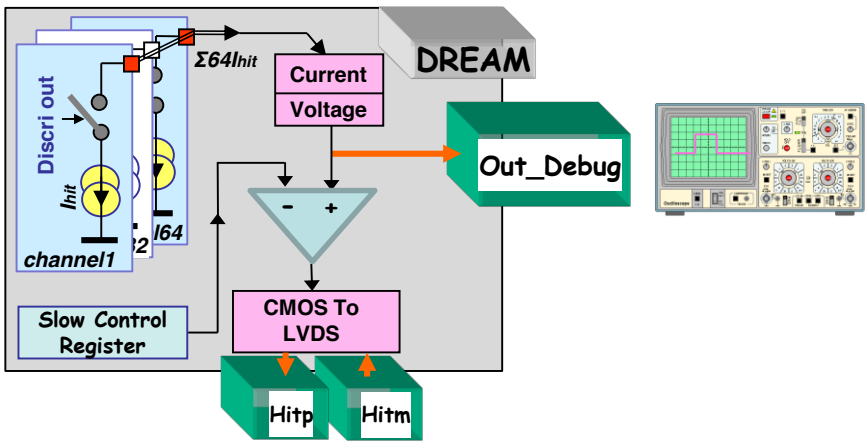


Fig. 6**:** block schematic of the HIT signal generation.

According to the multiplicity number (**Table 3**), the output of discriminator is translated into the LVDS signals available on the chip pins (Hitp & Hitm).

State2<27>	State2<26>	State2<25>	Multiplicity Level
0	0	0	*1*
0	0	1	*2*
0	1	0	*4*
0	1	1	*8*
1	0	0	*4*
1	0	1	*11*
1	1	0	*26*
1	1	1	*55*

Table 3: Selection of multiplicity level.

3.2.1 Enable of the HIT output signal

The ***HIT*** signal is available on pads 60&61 (**Hitp** & **Hitm**) by using the bit state1<27>.

3.2.2 Other way to read the HIT signal

For test purpose, it is possible to see the signal using the "spy" mode. The selection of the signal (1 among 6) is made using the 3 slow control bits state2<2:0>. The spy signal is available on the pin ***Out_debug*** (pad 38).

State2<2> Debug2	State2<1> Debug1	State2<0> Debug0	Out_debug (canal1)
0	0	0	*Standby*
0	0	1	*CSA*
0	1	0	*CR*
0	1	1	*Gain-2*
1	0	0	*Positive input of the discriminator*
1	0	1	*negative input of the discriminator*
1	1	0	*HIT*
1	1	1	*None*

Table 4: Selection of the output in the "spy" mode.

4. Principle of operation of the SCA

4.1 Simplified Operation

The analogue memory of Dream requires 5 digital signals to operate:

* Two clocks sequencing respectively the write and read operations:

- ***WCk***: the write clock, max frequency specified: 20MHz (operation up to 40-50 MHz probably possible if the event rate and then the buffer occupation is not too high).
- ***RCk***: the read clock with a maximum frequency of 20 MHz.

For SCA operation, these clocks are active on their rising edges, and can be interrupted when they are not used. In principle they can be at a different frequency and even asynchronous.

* Three control signals:

- ***Write***: signal defining the write operation and initializing the system.
- ***Trig***: "trigger" signal marking the acceptance of an event after a fixed latency **TRIGLAT**. It is taken into account on the rising edge of ***WCk***.
- ***Read***: signal commanding the read operation.

All these signals, excepted ***Write*** which is using a TTL compatible signal, are using differential LVDS compatible signals.

The analogue memory (**Fig. 7**) is composed of 64 lines of 512-cell switched capacitor array, each connected to the output of a Very Front End channel. The operations are done in parallel on the 64 lines of the SCA.

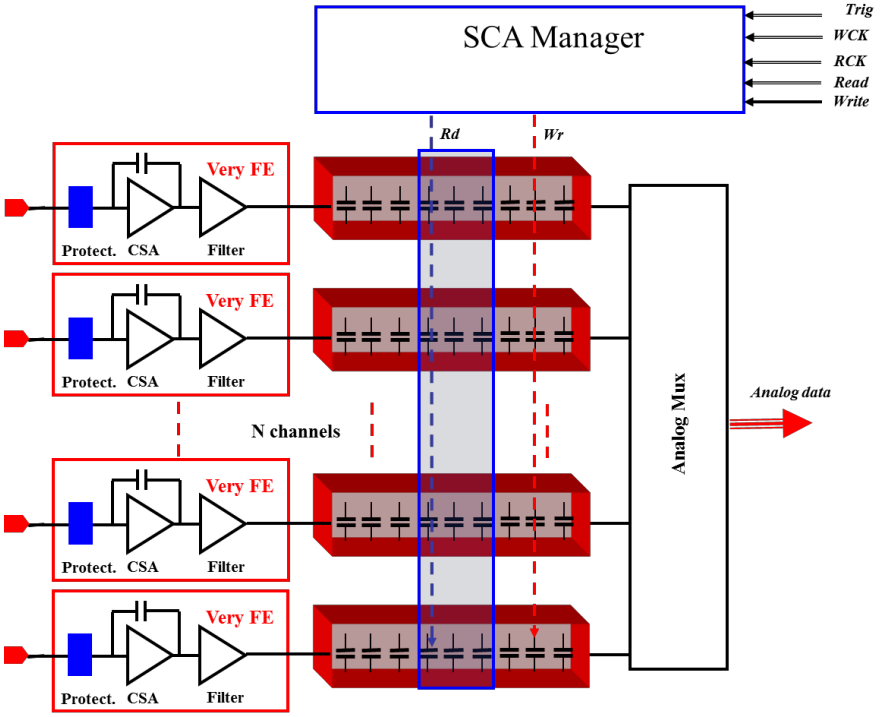


Fig. 7: Interconnection of the SCA with the very front-end part of the chip.

The SCA works as a L1 latency circular buffer. The analogue data is continuously sampled and memorized in it. Only the columns selected by an external trigger arriving with a fix ***TRIGLAT*** latency are frozen before to be read out on demand. Otherwise, during next SCA cycle, the unfrozen columns are overwritten when the write pointer of the circular buffer reach them again.

The readout is asynchronous and totally driven by external signals. It is performed in FIFO mode (the first data written is coming out first).

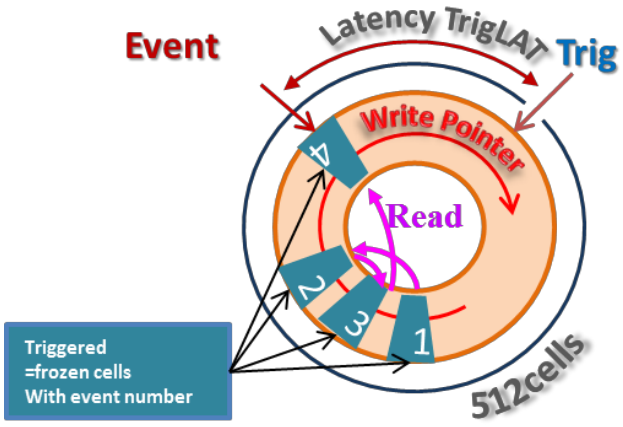


Fig. 8: SCA used as a L1 circular buffer with frozen cells.

4.2 More detailed Principle of Operation

When the Write signal takes state of '1', the analogue buffer is initialized and becomes ready for acquisition after few clock cycles (see the paragraph about initialization).

The output signal of the Front End part of the chip is sampled at the write clock frequency (rising edge) in the successive analogue memory free cells of the SCA. The SCA is used as a circular buffer: when the last cell is reached, the write pointer restarts on the first cell (or on the first free cell if the first is frozen).

When the Trig signal is high on the rising edge of ***WCk***, the column on which the signal was sampled ***TRIGLAT*** clock periods before is frozen in and is marked with an **Event Number**.

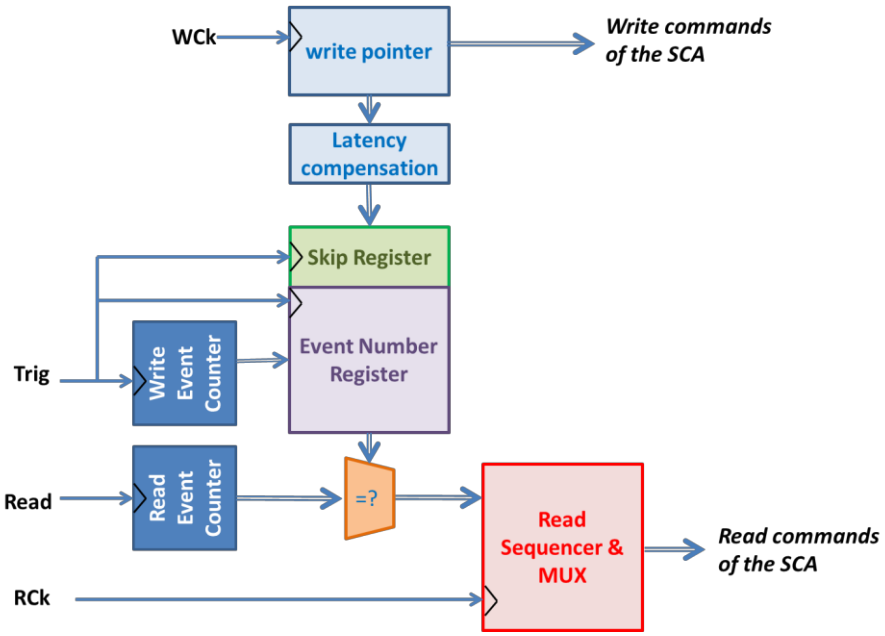


Fig. 9: Architecture of the Dream SCA Manager.

The Event Number (9 bits in **Gray code**) is incremented in the **Write Event Counter** at each new trigger. One "Event" corresponds to only one cell. To keep several (**Nc**) cells for a "physics" trigger, the ***Trig*** pulse must last **Nc** ***WCk*** period. Actually, it will be considered by the chip as **Nc** events. The only practical limitation for **Nc** is the SCA depth (and the already frozen columns)

The frozen columns are skipped by the write pointer as long as they are not released.

The sampling and triggering operations are of course not interrupted during the readout operation.

The readout of the event stored in the SCA with number equal to the **Read Event Counter** value is started on the rising edge of the ***Read*** signal. Actually, this is the oldest event stored in the SCA.

Analogue data are successively multiplexed on the ***RCk*** rising edge on the differential output of the chip:

The 3 first analogue data are coding the **Event Number**.

The samples of all the "enabled" channels are successively multiplexed starting from the channel with the lower index. If the ***Read*** signal is still high when the last channel is reached, the multiplexing restarts at the first channel.

The readout of some channels may be skipped using the Slow Control registers 9 and 10.

The readout is stopped when ***Read*** returns to 0. Starting at the next ***RCk*** rising edge, the 3 last analogue data, coding the index of the column on which the event was stored, are multiplexed. The **Read Event Counter** is then incremented.

The column is not released immediately at the trailing edge of Read but after a variable delay which can be as long as 512 ***WCk*** periods.

Theoretically, the write and the read operation can be totally asynchronous at the unique exception of the trailing edge of the Read signal which should be sent with a controlled phase in respect to the rising edge of ***WCk*** to avoid any metastability problem that could bring out desynchronisation between DREAM chips.

At least 4 ***RCk*** periods are required between the trailing edge of ***Read*** and the beginning of the next read operation (next rising edge of the ***Read*** signal).

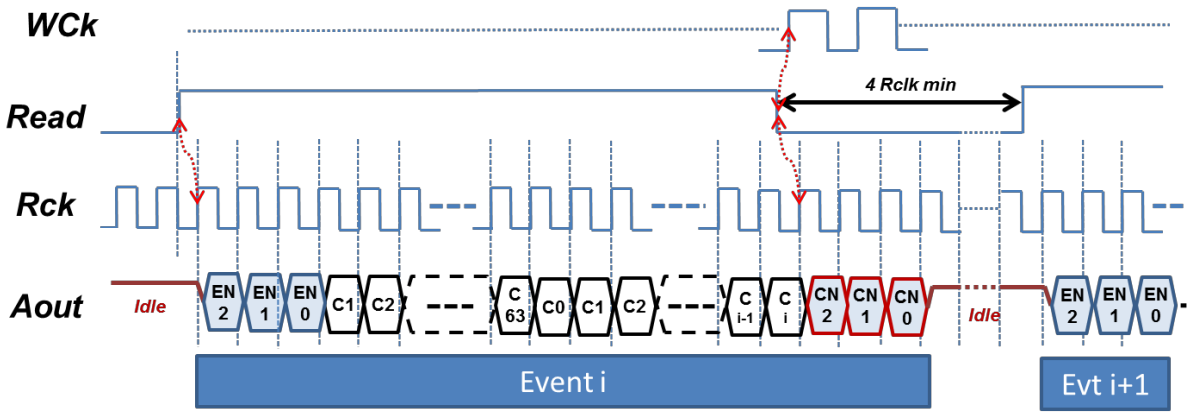


Fig. 10: Chronogram of the SCA Readout Operation.

4.3 SCA initialization

When the Write signal is at low level, the writing operation is inhibited in the SCA. The rising edge of ***Write*** initiates the synchronous resets of the **Write Pointer**, the **Write Event Counter** and the ***Read Event Counter***. It also releases all the cells (reset the markers freezing the columns) and initializes the trigger pointer (an internal pointer allowing to deal with the latency). For debugging reason, these initialization operations can be individually disabled by slow control using the bits 28-31 (DisInitWev, DisInitRev, DisInitPtW, DisInitPtS) of the register number 2. The user must wait (***TRIGLAT***+1) ***WCk*** periods after the rising edge of ***Write*** before sending a trigger.

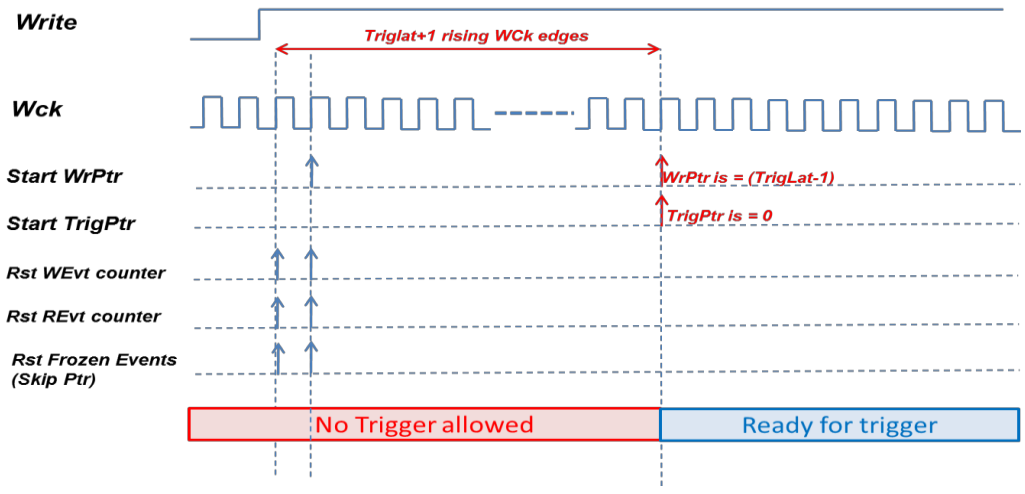


Fig. 11: Chronogram of the initialization phase of the SCA.

4.4 The SCA "idle" phase

Outside the read operation the DREAM chip output is in *idle* state. The chip behavior in this state is set by the value of the bits 6 and 7 of the SlowControl register 2 (*EnMkerRst* and *DisCompEvt*).

When ***EnMkerRst*** is set to **0**, the chip output voltage is at the standard baseline value of the chip.

When ***EnMkerRst*** is set to **1**, a "binary" data, depending on the state of the bit 7 of register 2 (***DisCompEvt***) is sent to the analogue output. A binary "0" corresponds to a low analogue level corresponding to a negative saturation of the ADC, whereas a binary "1" is a high analogue level corresponding to a positive saturation of the ADC.

If ***DisCompEvt*** is set to **0**: the output digital level sent on the analogue output during the idle phase is a digital 0.

If ***DisCompEvt*** is set to **1**: the output digital level is 1 if at least one triggered event is stored in the DREAM chip (waiting for readout); otherwise it is set to 0.

4.5 Analogue encoding of digital data during SCA readout

During the 3 first and 3 last clock periods of the readout of an event, 3 analogue data, coding each a 3-bit digital words, are sent to the analogue output. Two 9 bits digital data are thus sent. For each word, the first analogue data is coding the 3 most significant bits, the second the 3 intermediate bits and the last analogue data for the less significant bit of the digital data.

Each analogue data can take 8 levels (corresponding to a 3-bit digital data), starting typically from ***- 570mV*** (code 0) by step of ***163 mV***.

There is major exception to this: if a ***Read*** signal is sent by the controller while there is no event stored in the chip, the 3 last data of the analogue frame corresponding normally to the column index are forced to a special low level of ***- 740mV*** which can be interpreted as an error code.

5. The differential output buffer

This buffer is designed to drive differentially an external 12-bit ADC at up to 20MHz readout frequency (with a typical input capacitance up to 7pF, PCB parasitics included). Its input, connected to the SCA multiplexer output, is single-ended while its output is differential. As shown on **Fig. 12**, the single-ended to differential conversion is achieved using a full differential amplifier with its negative input connected to a reference voltage **Vicm.** This buffer also provides a gain of 1.328 between the differential output ($\mathbf{V_{op}}$-$\mathbf{V_{on}}$) and its input ($\mathbf{V_{ip}}$) to fit with the differential ADC input range (**+/-1 V**).

Thanks an internal common mode feedback, the common mode output voltage of the amplifier (($\mathbf{V_{op}}$+$\mathbf{V_{on}}$)/2) is equal to the voltage applied on the ***vocm*** (Pad 55) input. Its value can be fixed between 0.7V to 1.7V (1V for CLAS12 ADC).

The input common mode voltage (**Vicm**) is defined internally and must be filtered externally through the pad 56. The value of this voltage is controlled by the 2-bit state1<13:12>, to take into account the signal polarity and the offset voltage.

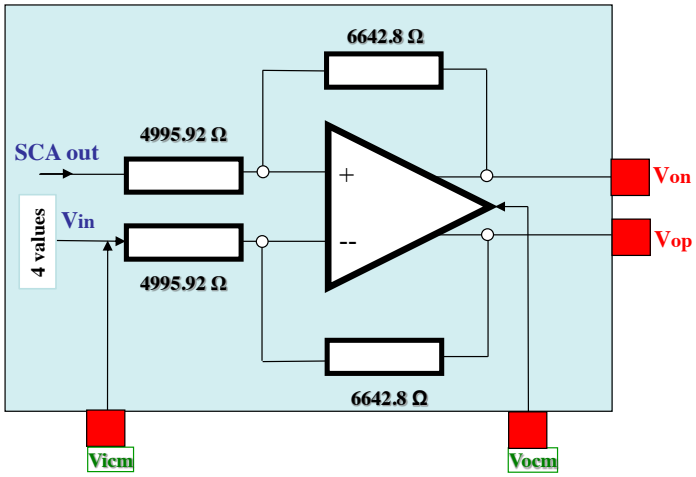


Fig. 12**:** Schematic of the readout buffer.

6. Architecture of the test & analog and digital "spy" modes systems

The DREAM chip includes a test system useful for the electrical calibration, the production test of the chips, and the control of the functionality of the overall electronics (ASIC to acquisition) when connected to detector. The chip also offers the possibility to spy internal nets inside the ASIC through 2 modes: analog and digital. The analog mode concerns the front end part of the channel 1 (CSA, PZC, Gain-2 outputs and discriminator inputs) and the HIT signal in CMOS level. The digital mode is dedicated to logical signals used for the SCA sampling and reading.

6.1 General description of the test system

The DREAM ASIC (**Fig. 13**) offers 3 different modes of test: calibration, test and functionality.

The Calibration operation consists in generating the same knew charge on the inputs of all the channels of the ASIC. Therefore, the charge pulse is generated outside of the chip, directly on the PCB. The charge injection is generated by applying a voltage step to a precision capacitor connected to the input of the selected channel via the ***In_Test*** input (pad 35).

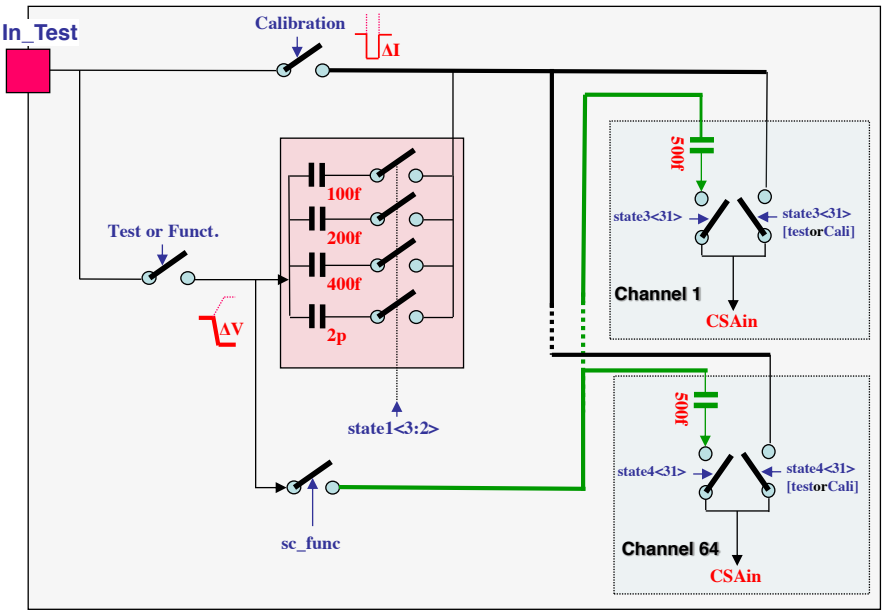


Fig. 13**:** Schematic of the test system

For the two other modes, the charge injection is generated through internal capacitors driven by an externally generated voltage applied on the pad ***In_Test***.

In the test mode, four different values of injection capacitor can be used. This permits working with the same test voltage pulse level for the 4 ranges. The selection of the injection capacitor is done with the 2-bit state1<3:2>.

In the functionality test mode, a single capacitor (500 fF) per channel is used.

For the 3 injection modes, the channel selection is made by switches inside the chip configured by slow control (state3<31:0> or state4<31:0>). For the two first modes, only one tested channel must be selected whereas up to the 64 channels can be selected when the functionality mode is used.

6.2 General description of the analog "spy" mode system

This mode permits to visualize on an oscilloscope (**Fig. 14**) the outputs of the CSA, PZC block and Gain-2 and the discriminator inputs of the channel number 1. It also gives the possibility to view the HIT signal.

This feature is useful to compare experimental and simulation results. By the state2<2:0> bits, one of these signals can be multiplexed, through an internal test buffer, to the pad ***Out_debug*** (pad 38).

If the "spy" mode is not selected, the internal buffer is put in a standby mode.

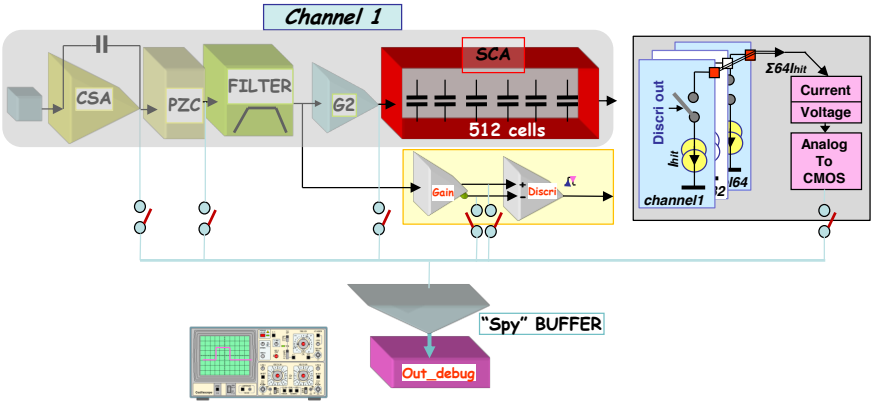


Fig. 14**:** Schematic of the analog "spy" system

6.3 General description of the digital "spy" mode system

This mode permits to visualize on an oscilloscope (**Fig. 15**) some critical signals used for the SCA management. Two signals among 16 possible (8 issued from column 0 and 8 from column 511) can be multiplexed simultaneously on pads ***Hitp*** and ***Hitm***, in LVDS level and pad **Out_debug** in CMOS level. This selection is made using the 9 Slow Control bits state2<24:16>.

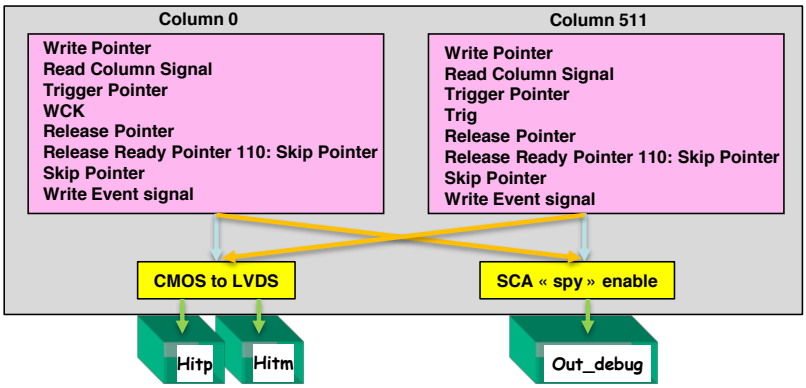


Fig. 15**:** Principle of the digital "spy" system.

7. The DREAM slow control

The slow control permits to program various chip parameters (gain, shaping time, test mode …) and to access to specific modes of operation. It is a serial protocol, used in several ASICs designed in IRFU laboratory. It gives access in write or read mode to the thirteen internal registers of the chip.

7.1 Power on Reset

When the chip is powered on, an internal "power on reset" device delivers a reset pulse (about 1ms of duration) resetting all the registers (all bits to 0), excepted for the register 5 which has only a read access.

7.2 Description of the slow control serial link

The link uses **4** signals [They use **CMOS** [0V; 3.3V] levels; except for the clock using **LVDS** levels]:

- ***Sc_din*** *[pin n°39]*: input data of the serial link.
- ***RCkm&RCkp*** *[pins n°44&45]*: readout clock also used to clock of the serial link. It is named ***RCk*** in the following section.
- ***Sc_en*** *[pin n°40]*: enable of the serial link.
- ***Sc_dout*** *[pin n°41]*: output data of the serial link.

IMPORTANT WARNINGS:

RCk is disabled in the slow control block during acquisition (if WRITE = 1).
⇨ **Slow control is only possible if WRITE = 0**

As RCk is used both for readout and slow control, it is forbidden to make a slow control access during readout and vice versa
⇨ **The Read signal must be equal to 0 when Sc_en is set to 1.**

The data are latched on the input lines, decoded and operations of reading/writing are carried out, by the ASIC, on the falling edge of ***RCk***. The data at the output of ***Sc_dout*** are also normally synchronous with this edge. A safe way to generate ***Sc_din*** & ***Sc_en*** signals consists in changing their state on the rising edge of ***RCk.***

On ***Sc_din,*** the data frame is defined as:

[r/wb] [Ad6… Ad0] [DNBD-1…D0]

[**r/wb**]: This first bit defines the type of operation. **r/wb** = 1 : readout; 0: write.
[**Ad6… Ad0**]: These 7 bits give the address of the target register.
[**DNBD-1…D0**]: This is the **NBD** bits of data to transmit.

The most significant bit of the address and the data is always sent (or read) first.

The ***Sc_en*** signal frames the data sent on ***Sc_din***. It must rise simultaneously with the positioning of [**r/wb**] and must go down one cycle of ***RCk*** after the positioning of the last bit of data (***D0***) on ***Sc_din***. Thus, the data packet defined by the setting of the ***Sc_en*** signal to 1 must frame [***8+ NBD*** falling edges**]** of ***RCk***.

The ***RCk*** clock must be present immediately after the beginning of the data frame and must continue at least during four clocks (falling edge) after the falling edge of ***Sc_en***.

Between the slow-control frames, the ***Sc_dout*** output is in idle state. If the ***force_eout*** bit of the register 2 is high, this output keeps its last valid value. If it is low (default mode), the output is in high impedance state.

7.3 Resynchronization of Sc_dout

All the data on the ***Sc_dout*** line are, by default, locally synchronized at each register level on the ***RCk*** falling edge. But this synchronizing is partially lost due to the different transit times in the chip. It is also possible, by slow control, to synchronize the signal on ***Sc_dout***. This is done by the bit 9 (***out_resync***) of the register 2, and the choice of active edge by the bit 10 (***synchro_inv***). If the state is "1", the synchronization is made on the falling edge of ***RCk***; "0" on the rising edge. All the chronograms on the next figures are in the case where the slow control bit ***out_resync*** is "0".

7.4 Writing mode (address other that 0) in a register of NBD bits

The write mode (**Fig. 16**) is defined by the first bit **r/wb = 0** on ***Sc_din***. The falling edge of ***Sc_en*** starts the writing of the **NBD** last bits on ***Sc_din*** in the target register. After the eighth falling edge of ***RCk***, ***Sc_dout*** leaves its idle state. During **NBD** clocks, ***Sc_dout*** takes the **Q0<n:1>** states, according to the history on the **Sc_din** line. Then, it will take the states present **NBD** clocks before (A<0>, D<NBD-1>, D<NBD-2> and D<NBD-3>).

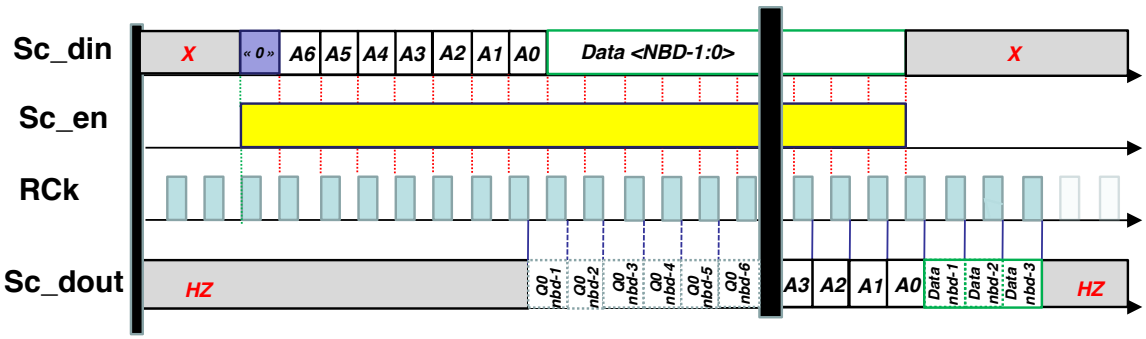


Fig. 16**:** The write mode.

Sc_dout will come back to its idle state 4 falling edges of the clock after the falling of ***Sc_en.*** The number of **NBD** bits present in the data part of ***Sc_din*** can be greater than the size of the register (**C** bits). In this case, only the **C** last bits will be written in the register. The **NBD-C-3** first bits of the data will go out on the ***Sc_dout*** after A0, DNBD-1, DNBD-2 & DNBD-3. This feature can be used to test the serial link.

7.5 Read operation on a NBD bits register

In the readout mode (**Fig. 17**), ***Sc_en*** must cover more than **8+NBD-2** falling edges of ***RCk***. A minimum of 4 falling edges of ***RCk*** after the falling of ***Sc_en*** is necessary to finish the reading phase.

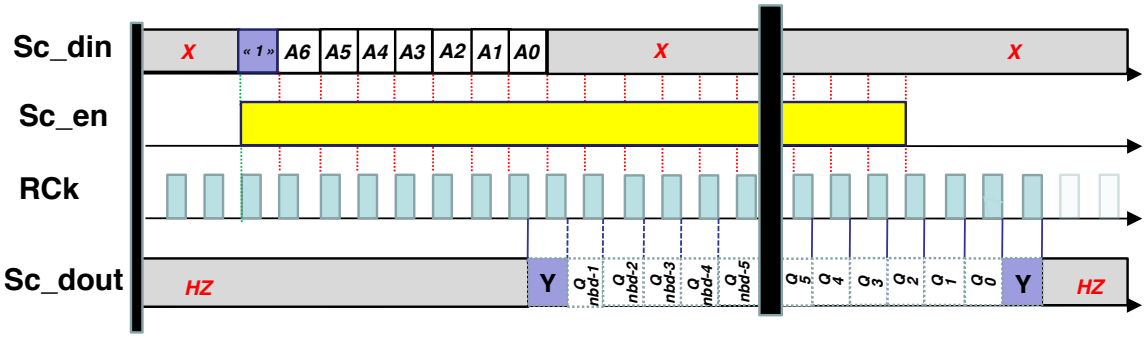


Fig. 17**:** The read mode.

The first bit on ***Sc_din*** must be to "1" (**r/wb**)**.** Thus the 7 other bits define the address of the register. The next bits can be indefinite.

At the eighth falling edge of ***RCk***, the address is decoded and ***Sc_dout*** leaves the idle state. During 1 clock cycle, its state **Y** depends on history of the serial link.

At the ninth falling edge of ***RCk***, the data of the register is serialized toward ***Sc_dout*** during **NBD-1** clock cycles. After these **NBD** clock cycles, the data coming out from the ***Sc_dout*** are no more valid.

As for the writing phase, ***Sc_dout*** go back to the idle state, **4** clock cycles after the falling edge of ***Sc_en.***

7.6 Description of the slow control registers

The DREAM chip includes 12 internal registers for the ASIC configuration (table 5) with different wide (16 to 64 bits).

address	name	Width	access	action
0	**dummy**		W	serial link test purpose
1	**ASIC configuration 1**	32 bits	R/W	chip configuration
2	**ASIC configuration 2**	32 bits	R/W	Special modes and test configuration.
3	**First group test selection**	32 bits	R/W	selection of tested channels (1 to 32)
4	**Second group test selection**	32 bits	R/W	selection of tested channels (33 to 64)
5	**ASIC version number**	16 bits	R	Contains the version number of the chip
6	**Gain 1 to 32**	64 bits	R/W	Input charge range of the channel 1 to 32
7	**Gain 33 to 64**	64 bits	R/W	Input charge range of the channel 33 to 64
8	**Trigger Inhibition 1 to 32**	32 bits	R/W	inhibition of the channel trigger 1 to 32
9	**Trigger inhibition 33 to 64**	32 bits	R/W	inhibition of the channel trigger 33 to 64
10	**SCA Readout 1 to 32**	32 bits	R/W	enabling of the SCA readout channel 1 to 32
11	**SCA Readout 35 to 64**	32 bits	R/W	enabling of the SCA readout of channels 33 to 64
12	**Trigger Latency**	16 bits	R/W	Value of the Trigger Latency

Table 5: Mapping of the DREAM slow control registers.

7.6. A The register 0

The register **0** doesn't physically exist. But, when it is addressed in write mode, ***Sc_dout*** recopy the data on ***Sc_din*** (after the eighth falling edge of ***RCk***). ***Sc_dout*** comes back to the idle state (4 falling edges after the falling edge of ***Sc_en***).

7.6. B The register 1

This 32-bit register is located at address number 1 (table 6). This register controls the main configuration parameters of the chip front-end part.

bit	name	action
0	**Icsa0**	LSB for the CSA input current value
1	**Icsa1**	MSB for the CSA input current value
2	**TestGain0**	LSB of the internal test capacitor in Test mode
3	**TestGain1**	MSB of the internal test capacitor in Test mode
4	**Time0**	LSB of the filter peaking time
5	**Time1**	bit 1 of the filter peaking time
6	**Time2**	bit 2 of the filter peaking time
7	**Time3**	MSB of the filter peaking time
8	**Test0**	LSB of the test mode register
9	**Test1**	MSB of the test mode register
10	**Integrator mode**	If 1, set the PZC shaping time value to 500 ns
11	**Polarity**	Specify the polarity of the input detector signal
12	**Vicm0**	LSB of the input common mode voltage of the data buffer
13	**Vicm1**	MSB of the input common mode voltage of the data buffer
14	**ThDAC 0**	LSB of the global threshold DAC
15	**ThDAC 1**	Bit 1 of the global threshold DAC
16	**ThDAC 2**	Bit 2 of the global threshold DAC
17	**ThDAC 3**	Bit 3 of the global threshold DAC
18	**ThDAC 4**	Bit 4 of the global threshold DAC
19	**ThDAC 5**	Bit 5 of the global threshold DAC
20	**ThDAC 6**	MSB of the global threshold DAC
21	**ThDAC sign**	Sign bit for the global threshold DAC
22	**HIT veto**	Select the HIT logic veto
23	**TOT**	if 1, width HIT = output discri (Time over Threshold)
24	**Range_HIT_width**	Select the width range of the HIT signal (100ns/200ns)
25	**Lsb_HIT_width**	LSB of the HIT width
26	**Msb_HIT_width**	MSB of the HIT width
27	**HIT_enable**	If 1, enables the HIT on channels & LVDS outputs
28	**External 0**	LSB of the external input selection
29	**External 1**	MSB of the external input selection
30	**Discri_range**	If 1, the discriminator input range is fixed to 5% (17.5% for 0)
31	**Int_time_constant**	If 1, the CSA integration time constant is set to 50 µs (5 µs for 0)

Table 6: Register 1 Mapping.

The purposes of the register 1 bit are described hereafter:

state1<0:1>: Bits Icsa0 & Icsa1.

These 2 bits configure the current value of the CSA input stage (table 7). This feature permits to adapt the power consumption versus the noise resolution.

Icsa1	Icsa0	Current value
0	**0**	***400 µA***
0	**1**	***500 µA***
1	**0**	***800 µA***
1	**1**	***1.2 mA***

Table 7: Definition of the CSA input current.

state1<2:3>: Bits TestGain0 &TestGain1.

These 2 bits are need to select one internal test capacitor among 4 (table 8) in the test mode.

TestGain1	TestGain0	Test Capacitor value
0	**0**	***100 fF***
0	**1**	***200 fF***
1	**0**	***400 fF***
1	**1**	***2 pF***

Table 8: Choice of the internal test capacitor.

state1<4:7>: Bits Time0 to Time3.

These 4 bits are setting the peaking time of the shaper (table 9), by switching resistors on the PZC & SK filters.

Time3	Time2	Time1	Time0	Peaking Time [5%_100%] (ns)
0	0	0	0	*76*
0	0	0	1	*123*
0	0	1	0	*180*
0	0	1	1	*228*
0	1	0	0	*283*
0	1	0	1	*328*
0	1	1	0	*388*
0	1	1	1	*433*
1	0	0	0	*578*
1	0	0	1	*618*
1	0	1	0	*675*
1	0	1	1	*717*
1	1	0	0	*781*
1	1	0	1	*818*
1	1	1	0	*880*
1	1	1	1	*919*

Table 9: Definition of the peaking time.

state1<8:9>: Bits Test0 & Test1.

These bits are defining the test mode (table 10).

Test1	Test0	Test mode
0	0	*nothing*
0	1	*calibration*
1	0	*test*
1	1	*functionality*

Table 10: Definition of the test mode.

The calibration, test & functionality tests require the choice of one or several channels. This is done by the registers 3 & 4. For the test mode, it is also necessary to select the internal capacitor (Gain 0 & 1 of the register 1).

state1<10>: Bit integrator mode.

This bit fixes the shaping time of the PZC stage to 450 ns value independently of the 16 possible shaping time values of the Sallen-Key filter.

state1<11>: Bit polarity.

This bit controls the value of the dc voltage level (2 values) of the CSA, CR and Gain -2 according to the input signal polarity (table 11).

CSA	CR&SK	G2	Bit polarity	Detector signal
1.8V	2.2V	*0.7V*	*0*	*Neg. (CSA current out)*
2.8V	0.7V	*2.2V*	*1*	*Pos. (CSA current in)*

Table 11: CSA, CR, SK & Gain2 dc voltage value versus bit polarity.

state1<12:13>: Bits vicm0 & vicm1.

These 2 bits adapt the input common mode voltage of the analog output buffer, according to the polarity of the signal and additional offset (table 12).

Vicm 1	Vicm 0	VICM value	Polarity
0	0	*1.25V*	*negative*
0	1	*1.35V*	
1	0	*1.55V*	*positive*
1	1	*1.65V*	

Table 12: Definition of the Buffer Vicm.

state1<14:21>: Bits ThDAC0 to ThDAC sign.

The first 7 bits are defining the value of the global threshold and the last bit (DAC sign) the polarity of the input signal (“0” for negative polarity).

state1<22>: Bit HIT veto.

This bit controls the veto on the HIT building (table 13).

Bit HIT veto	veto
0	*none*
1	*4 µs*

Table 13: Definition of the HIT veto.

state1<23>: Bit TOT.

This bit permits ("1") or not ("0") to have a **HIT** signal with the same duration as the one of the discriminator output signal (Time Over Threshold).

state1<24>: Bit Range_HIT_width.

This bit defines the width range of the HIT signal (table 14).

Range_HIT_width	Width range (ns)
0	*100 ns*
1	*200 ns*

Table 14: Definition of the HIT width range.

state1<25:26>: Bits lsb_HIT_width & msb_HIT_width.

These 2 bits adjust the value of the HIT according to the technology process variations (table 15 & 16) and to the value of the ***Range_HIT_width*** value.

For Range_HIT_width = "0".

Msb_HIT_width	Lsb_HIT_width	wp	tm	ws
0	0	*60.86 ns*	*93.88 ns*	*127.91 ns*
0	1	*49.8 ns*	*77.4 ns*	*106.25 ns*
1	0	*71.95 ns*	*110.36 ns*	*149.8 ns*
1	1	*82.86 ns*	*126.9 ns*	*171.6 ns*

Table 15: adjustment of the HIT width in the 100 ns range.

For Range_HIT_width = "1".

Msb_HIT_width	Lsb_HIT_width	wp	tm	ws
0	0	*142 ns*	*218 ns*	*297 ns*
0	1	*110 ns*	*170 ns*	*232 ns*
1	0	*153 ns*	*235 ns*	*319 ns*
1	1	*194 ns*	*298 ns*	*404 ns*

Table 16: adjustment of the HIT width in the 200 ns range.

state1<27>: Bit HIT enable.

This bit enables the HIT data output at the channel level and LVDS outputs.

state1<28:29>: Bits External 0 & External 1.

These 2 bits specify the access point in the external input mode (table 17).

External 1	External 0	Access point
0	0	*none*
0	1	*SK Filter input*
1	0	*Gain-2 input*
1	1	*CSA standby*

Table 17: Definition of the access point.

state1<30>: Bit discri-range.

This bit permits to select the value of input dynamic range of the discriminator between two values: 5 or 17.5 % of the channel input dynamic range.

State1<30>	Input dynamic range of the discriminator
0	*17.5 %*
1	*5 %*

Table 18: Definition of the input dynamic range of the discriminator.

state1<31>: Bit Int_time_constant.

By slow control, it is possible to select the value of integration time constant between two values for all the 4 gains: 5 µs or 50 µs (table 19).

State1<31>	CSA Integration time constant
0	*5 µs*
1	*50 µs*

Table 19: Definition of the integration time constant value.

7.6. C The register 2

This 32-bit register is used to configure the test modes and to control the SCA readout (table 20).

bit	name	Action
0	**debug0**	These 3 bits select the internal signal to be visualized on scope.
1	**debug1**	
2	**debug2**	
3	**forceDAC<0>**	If different of 0, force the Event Number to a fix value.
4	**forceDAC<1>**	
5	**SC_lowBLSCARes**	This bit controls or not the CSA read amplifier current
6	**EnMkerRst**	If 1, a "digital" marker (level defined by DiscompEvt)) is sent at the Output during the idle phase of the SCA readout instead of the SCA base line (0.7 V).
7	**DiscompEvt**	Set the level of the “digital” level (if EnMkerRst is set to “1”).
8	**boost_pw**	If 1, the output current of the analog block Gain-2 is increased (+20%)
9	**out_resync**	If 1, the SC output data is resynchronized by a clock edge (selected by synchro_inv).
10	**synchro_inv**	Select the edge for the synchronizing of the SC output data: 0= rising,1=falling.
11	**force_eout**	If 1, inhibit the 3rd state of the SC output buffer during SC idle state.
12	**Cur_RA<0>**	These 2 bits are programing the current of the SCA readout amplifiers.
13	**Cur_RA<1>**	
14	**Cur_BUF<0>**	These 2 bits are programing the current of the SCA output buffers.
15	**Cur_BUF<1>**	
16	**SCASpy<0>**	These 9 bits are programing the spy Output of the SCA.
17	**SCASpy<1>**	
18	**SCASpy<2>**	
19	**SCASpy<3>**	
20	**SCASpy<4>**	
21	**SCASpy<5>**	
22	**SCASpy<6>**	
23	**SCASpy<7>**	
24	**SCASpy<8>**	
25	**HIT_multi<0>**	These 3 bits select the multiplicity threshold value for the HIT signal
26	**HIT_multi<1>**	
27	**HIT_multi<2>**	
28	**DisInitWev**	If 1 disable the reset of the Write Event Counter.
29	**DisInitRev**	If 1 disable the reset of the Read Event Counter.
30	**DisInitPtW**	If 1 disable the reset of the Write and Trigger Pointers.
31	**DisInitPtSK**	If 1 disable the reset of the Skip Pointers.

Table 20: Register 2.

state2<0:2>: Bits Debug 0 & Debug 2.

These 3 bits permits to multiplex toward the ***Out_debug*** pad the output of the CSA, PZC filter and Gain-2 or of the 2 inputs of the discriminators from the channel number 1. It is also possible to view directly the trigger signal. Depending on these bits (table 21), one among these outputs is selected.

Debug2	Debug1	Debug0	Out_debug (canal1)
0	0	0	*Standby*
0	0	1	*CSA*
0	1	0	*CR*
0	1	1	*Gain-2*
1	0	0	*Positive input of the discriminator*
1	0	1	*negative input of the discriminator*
1	1	0	*HIT*
1	1	1	*none*

Table 21: Selection of the output in the analog “spy” mode.

state2<3:4>: Bits forceDAC<0:1>

Mask the 9 bit word coded in analogue levels corresponding to the **EventNumber** at the beginning of the readout phase (table 22).

ForceDAC	Effect on the EventNumber data
0	*no masking*
1	*Forced to 0*
2	*Forced to 90 (001011010 in binary)*
3	*Forced to 511*

Table 22: Event Number masking.

This can be used for testing or to calibrate the levels of the DAC coding the digital information during the beginning and the end of the Readout.

state2<5>: Sc_LowBLSCARes.

If “1”, the SCA read amplifier is put in standby outside the read phase.

state2<6>: en_mker_rst.

If “1”, a "digital" marker (level defined by the bit state2<7>) is sent at the Output during the idle phase of the SCA readout. If “0”, the output voltage is fixed to 0.7 V.

state2<7>: DisCompEvt.

This bit set the level of the “digital” marker. If “0” the digital level sent on the analogue output during the idle phase is a digital “0”. If “1” the digital level is “1” if at least one triggered event is stored in the DREAM chip, otherwise a 0 is sent.

state2<8>: boost_pw.

If 1, the output current of the GAIN-2 amplifier is increased by +20%. It can be used for very fast sampling frequencies and in case of chip fabricated in a “slow” corner process.

state2<9>: out_resync.

If 1, the ***Sc_dout*** output data is resynchronized by a clock edge ***RCk***, selected by ***synchro_inv***.

state2<10>: synchro_inv.

It selects the edge for the synchronizing of the ***Sc_dout*** output data. "0" select the rising edge, "1" the falling.

state2<11>: force_eout.

"1" inhibits the 3rd state functionality of the Slow Control output buffer.

state2<12:13>: Bits CUR_RA <0:1>.

These 2 bits are controlling the bias current of the 64 SCA line readout amplifiers. The table 23 gives the different values of the current consumed by a single readout buffer.

CUR_RA<1>	CUR_RA<0>	*value*
0	0	***352uA***
0	1	***450uA***
1	0	***637uA***
1	1	***1150uA***

Table 23: Control of the SCA line readout amplifier.

The nominal configuration is: « **10** » (637 µA).

state2<14:15>: Bits CUR_BUF <0:1>.

These 2 bits are controlling the bias current of the SCA amplifiers used in the output analogue multiplexer. The table 24 shows the different values of the current consumed by these 3 amplifiers.

CUR_BUF<1>	CUR_BUF<0>	I power
0	0	***1.503 mA***
0	1	***1.914 mA***
1	0	***2.700 mA***
1	1	***4.870 mA***

Table 24: Control of the SCA mux amplifiers current.

The nominal configuration is: « **10** » (2.7 mA).

state2<16> to state2<24>: Bits SCASpy<0:8>.

These 9 bits are programing the Spy Output of the SCA.

state2<16:18>: Bits SCASpyCh0<0:2>.

These 3 bits select the test signal, 1 among 8 (table 25), sent on the ***Hitp*** & ***Hitm*** outputs.

SCASpyCh0<2>	SCASpyCh0<1>	SCASpyCh0<0>	Test signal on Hitp&Hitm
0	0	0	***Write Pointer***
0	0	1	***Read Column Signal***
0	1	0	***Trigger Pointer***
0	1	1	***WCk (for col. 0) or Trig (for col. 511)***
1	0	0	***Release Pointer***
1	0	1	***Release Ready Pointer 110: Skip Pointer***
1	1	0	***Skip Pointer***
1	1	1	***Write Event signal***

Table 25: Selection of the test signal on ***Hitp & Hitm*** outputs.

state2<19>: Bits SCASpyCh0<3>.

This bit defines the source column of the test signal (table 26), sent on the ***Hitp*** & ***Hitm*** outputs.

SCASpyCh0<3>	Source column of theTest signal on Hitp&Hitm outputs
0	***Column 0***
1	***Column 511***

Table 26: Selection of the source column of the test signal on ***Hitp & Hitm*** outputs.

state2<20:22>: Bits SCASpyCh1<0:2>.

These 3 bits select the test signal, 1 among 8 (table 27), sent on the ***Out_debug*** output.

SCASpyCh1<2>	SCASpyCh1<1>	SCASpyCh1<0>	Test signal on Out_debug
0	0	0	***Write Pointer***
0	0	1	***Read Column Signal***
0	1	0	***Trigger Pointer***
0	1	1	***WCk (for col. 0) or Trig (for col. 511)***
1	0	0	***Release Pointer***
1	0	1	***Release Ready Pointer 110: Skip Pointer***
1	1	0	***Skip Pointer***
1	1	1	***Write Event signal***

Table 27: Selection of the test signal on ***Out_debug*** output.

state2<23>: Bit SCASpyCh1<3>.

This bit defines the source column of the test signal (table 28), sent on the ***Out_debug*** output.

SCASpyCh1<3>	Source column of the test signal on Out_debug output
0	***Column 0***
1	***Column 511***

Table 28: Selection of the source column of the test signal on ***Out_debug*** output.

state2<24>: Bit EnSCASpy

This bit enables the spy mode of the SCA digital signals. In this mode, 2 spy signal selected among 16 possible are send on the chip pads: ***Hitp***&***Hitm*** (through a CMOS to LVDS converter) and ***Out_debug***.

state2<25:27>: Bits Hit_multi<0:2>.

These 3 bits select the multiplicity level value (table 29) necessary to validate a HIT signal.

Hit_multi<2>	Hit_multi<1>	Hit_multi<0>	Multiplicity level
0	0	0	*1*
0	0	1	*2*
0	1	0	*4*
0	1	1	*8*
1	0	0	*4*
1	0	1	*11*
1	1	0	*26*
1	1	1	*55*

Table 29: Selection of the multiplicity level need to validate a HIT signal.

state2<28:31>: Bits ***DisInitWev***, ***DisInitRev***, ***DisInitPtW***, ***DisInitPtSK***.

These bits permit to inhibit reset or initialization performed respectively on the Write Event Counter, the Read Event Counter, the Write and Trigger Pointers, and the Skip Pointer when the Write signal rises to 1.

7.6. D The register 3

This 32-bit register is located at address number 3. It is used to select the channel for the test (table 30). The channel number goes from 1 to 32.

bit	name	action
0	**select_c32**	Selection of the channel 32 for the test
1	**select_c31**	Selection of the channel 31 for the test
2	**select_c30**	Selection of the channel 30 for the test
3	**select_c29**	Selection of the channel 29 for the test
4	**select_c28**	Selection of the channel 28 for the test
5	**select_c27**	Selection of the channel 27 for the test
6	**select_c26**	Selection of the channel 26 for the test
7	**select_c25**	Selection of the channel 25 for the test
8	**select_c24**	Selection of the channel 24 for the test
9	**select_c23**	Selection of the channel 23 for the test
10	**select_c22**	Selection of the channel 22 for the test
11	**select_c21**	Selection of the channel 21 for the test
12	**select_c20**	Selection of the channel 20 for the test
13	**select_c19**	Selection of the channel 19 for the test
14	**select_c18**	Selection of the channel 18 for the test
15	**select_c17**	Selection of the channel 17 for the test
16	**select_c16**	Selection of the channel 16 for the test
17	**select_c15**	Selection of the channel 15 for the test
18	**select_c14**	Selection of the channel 14 for the test
19	**select_c13**	Selection of the channel 13 for the test
20	**select_c12**	Selection of the channel 12 for the test
21	**select_c11**	Selection of the channel 11 for the test
22	**select_c10**	Selection of the channel 10 for the test
23	**select_c9**	Selection of the channel 9 for the test
24	**select_c8**	Selection of the channel 8 for the test
25	**select_c7**	Selection of the channel 7 for the test
26	**select_c6**	Selection of the channel 6 for the test
27	**select_c5**	Selection of the channel 5 for the test
28	**select_c4**	Selection of the channel 4 for the test
29	**select_c3**	Selection of the channel 3 for the test
30	**select_c2**	Selection of the channel 2 for the test
31	**select_c1**	Selection of the channel 1 for the test

Table 30: Description of the register 3.

7.6. E The register 4

This 32-bit register is located at address number 4. It is used to select the channel for the test (table 31). The channel number goes from 33 to 64.

bit	name	action
0	**select_c33**	Selection of the channel 33 for the test
1	**select_c34**	Selection of the channel 34 for the test
2	**select_c35**	Selection of the channel 35 for the test
3	**select_c36**	Selection of the channel 36 for the test
4	**select_c37**	Selection of the channel 37 for the test
5	**select_c38**	Selection of the channel 38 for the test
6	**select_c39**	Selection of the channel 39 for the test
7	**select_c40**	Selection of the channel 40 for the test
8	**select_c41**	Selection of the channel 41 for the test
9	**select_c42**	Selection of the channel 42 for the test
10	**select_c43**	Selection of the channel 43 for the test
11	**select_c44**	Selection of the channel 44 for the test
12	**select_c45**	Selection of the channel 45 for the test
13	**select_c46**	Selection of the channel 46 for the test
14	**select_c47**	Selection of the channel 47 for the test
15	**select_c48**	Selection of the channel 48 for the test
16	**select_c49**	Selection of the channel 49 for the test
17	**select_c50**	Selection of the channel 50 for the test
18	**select_c51**	Selection of the channel 51 for the test
19	**select_c52**	Selection of the channel 52 for the test
20	**select_c53**	Selection of the channel 53 for the test
21	**select_c54**	Selection of the channel 54 for the test
22	**select_c55**	Selection of the channel 55 for the test
23	**select_c56**	Selection of the channel 56 for the test
24	**select_c57**	Selection of the channel 57 for the test
25	**select_c58**	Selection of the channel 58 for the test
26	**select_c59**	Selection of the channel 59 for the test
27	**select_c60**	Selection of the channel 60 for the test
28	**select_c61**	Selection of the channel 61 for the test
29	**select_c62**	Selection of the channel 62 for the test
30	**select_c63**	Selection of the channel 63 for the test
31	**select_c64**	Selection of the channel 64 for the test

Table 31: Description of the register 4.

7.6. F The register 5

This 16- bit register is located at address number 5. It contains the version number of the circuit. The version number is: 0x0302 (0x0301 for DREAM prototype version).

7.6. G The register 6

This 64-bit register defines the gain of the 32 first channels. For each channel, there are 2 bits to select its CSA charge capacitor among 4 possible. The mapping is given in the table 32.

bit	name	action	bit	name	action
0	**Lsb Gain c32**		32	**Lsb Gain c16**	
1	**Msb Gain c32**	Gain selection channel 32	33	**Msb Gain c16**	Gain selection channel 16
2	**Lsb Gain c**31		34	**Lsb Gain c**15	
3	**Msb Gain c**31	Gain selection channel 31	35	**Msb Gain c**15	Gain selection channel 15
4	**Lsb Gain c30**		36	**Lsb Gain c14**	
5	**Msb Gain c30**	Gain selection channel 30	37	**Msb Gain c14**	Gain selection channel 14
6	**Lsb Gain c29**		38	**Lsb Gain c13**	
7	**Msb Gain c29**	Gain selection channel 29	39	**Msb Gain c13**	Gain selection channel 13
8	**Lsb Gain c28**		40	**Lsb Gain c12**	
9	**Msb Gain c28**	Gain selection channel 28	41	**Msb Gain c12**	Gain selection channel 12
10	**Lsb Gain c27**		42	**Lsb Gain c11**	
11	**Msb Gain c27**	Gain selection channel 27	43	**Msb Gain c11**	Gain selection channel 11
12	**Lsb Gain c26**		44	**Lsb Gain c10**	
13	**Msb Gain c26**	Gain selection channel 26	45	**Msb Gain c10**	Gain selection channel 10
14	**Lsb Gain c25**		46	**Lsb Gain c09**	
15	**Msb Gain c25**	Gain selection channel 25	47	**Msb Gain c09**	Gain selection channel 9
16	**Lsb Gain c24**		48	**Lsb Gain c08**	
17	**Msb Gain c24**	Gain selection channel 24	49	**Msb Gain c08**	Gain selection channel 8
18	**Lsb Gain c23**		50	**Lsb Gain c07**	
19	**Msb Gain c23**	Gain selection channel 23	51	**Msb Gain c07**	Gain selection channel 7
20	**Lsb Gain c22**		52	**Lsb Gain c06**	
21	**Msb Gain c22**	Gain selection channel 22	53	**Msb Gain c06**	Gain selection channel 6
22	**Lsb Gain c21**		54	**Lsb Gain c05**	
23	**Msb Gain c21**	Gain selection channel 21	55	**Msb Gain c05**	Gain selection channel 5
24	**Lsb Gain c20**		56	**Lsb Gain c04**	
25	**Msb Gain c20**	Gain selection channel 20	57	**Msb Gain c04**	Gain selection channel 4
26	**Lsb Gain c19**		58	**Lsb Gain c03**	
27	**Msb Gain c19**	Gain selection channel 19	59	**Msb Gain c03**	Gain selection channel 3
28	**Lsb Gain c18**		60	**Lsb Gain c02**	
29	**Msb Gain c18**	Gain selection channel 18	61	**Msb Gain c02**	Gain selection channel 2
30	**Lsb Gain c17**		62	**Lsb Gain c01**	
31	**Msb Gain c17**	Gain selection channel 17	63	**Msb Gain c01**	Gain selection channel 1

Table 32: Description of the register 6.

At the channel level, the gain is defined as follows:

MSB	LSB	Input dynamic range
0	**0**	***50 fC (0,5 pF)***
0	**1**	***100 fC (1 pF)***
1	**0**	***200 fC (2 pF)***
1	**1**	***600 fC (1,2 pF)***

7.6. H The register 7

This 64-bit register defines the gain of the 32 last channels. For each channel, there are 2 bits to select its CSA charge capacitor among 4 possible. The mapping is given in the table 33.

bit	name	action	bit	name	action
0	**Lsb Gain c33**		32	**Lsb Gain c49**	
1	**Msb Gain c33**	Gain selection channel 33	33	**Msb Gain c49**	Gain selection channel 49
2	**Lsb Gain c**34		34	**Lsb Gain c**50	
3	**Msb Gain c**34	Gain selection channel 34	35	**Msb Gain c**50	Gain selection channel 50
4	**Lsb Gain c35**		36	**Lsb Gain c51**	
5	**Msb Gain c35**	Gain selection channel 35	37	**Msb Gain c51**	Gain selection channel 51
6	**Lsb Gain c36**		38	**Lsb Gain c52**	
7	**Msb Gain c36**	Gain selection channel 36	39	**Msb Gain c52**	Gain selection channel 52
8	**Lsb Gain c37**		40	**Lsb Gain c53**	
9	**Msb Gain c37**	Gain selection channel 37	41	**Msb Gain c53**	Gain selection channel 53
10	**Lsb Gain c38**		42	**Lsb Gain c54**	
11	**Msb Gain c38**	Gain selection channel 38	43	**Msb Gain c54**	Gain selection channel 54
12	**Lsb Gain c39**		44	**Lsb Gain c55**	
13	**Msb Gain c39**	Gain selection channel 39	45	**Msb Gain c55**	Gain selection channel 55
14	**Lsb Gain c40**		46	**Lsb Gain c56**	
15	**Msb Gain c40**	Gain selection channel 40	47	**Msb Gain c56**	Gain selection channel 56
16	**Lsb Gain c41**		48	**Lsb Gain c57**	
17	**Msb Gain c41**	Gain selection channel 41	49	**Msb Gain c57**	Gain selection channel 57
18	**Lsb Gain c42**		50	**Lsb Gain c58**	
19	**Msb Gain c42**	Gain selection channel 42	51	**Msb Gain c58**	Gain selection channel 58
20	**Lsb Gain c43**		52	**Lsb Gain c59**	
21	**Msb Gain c43**	Gain selection channel 43	53	**Msb Gain c59**	Gain selection channel 59
22	**Lsb Gain c44**		54	**Lsb Gain c60**	
23	**Msb Gain c44**	Gain selection channel 44	55	**Msb Gain c60**	Gain selection channel 60
24	**Lsb Gain c45**		56	**Lsb Gain c61**	
25	**Msb Gain c45**	Gain selection channel 45	57	**Msb Gain c61**	Gain selection channel 61
26	**Lsb Gain c46**		58	**Lsb Gain c62**	
27	**Msb Gain c46**	Gain selection channel 46	59	**Msb Gain c62**	Gain selection channel 62
28	**Lsb Gain c47**		60	**Lsb Gain c63**	
29	**Msb Gain c47**	Gain selection channel 47	61	**Msb Gain c63**	Gain selection channel 63
30	**Lsb Gain c48**		62	**Lsb Gain c64**	
31	**Msb Gain c48**	Gain selection channel 48	63	**Msb Gain c64**	Gain selection channel 64

Table 33: Description of the register 7.

At the channel level, the gain is defined as follows:

MSB	LSB	Input dynamic range
0	**0**	***50 fC (0,5 pF)***
0	**1**	***100 fC (1 pF)***
1	**0**	***200 fC (2 pF)***
1	**1**	***600 fC (1,2 pF)***

7.6. I The register 8

This 32-bit register permits to inhibit the discriminator of specific channel. The mapping for the channel 1 to 32 is given in the table 34.

bit	name	action
0	**Trig_inhi_c32**	inhibition of the channel 32
1	**Trig_inhi _c31**	inhibition of the channel 31
2	**Trig_inhi _c30**	inhibition of the channel 30
3	**Trig_inhi _c29**	inhibition of the channel 29
4	**Trig_inhi _c28**	inhibition of the channel 28
5	**Trig_inhi _c27**	inhibition of the channel 27
6	**Trig_inhi _c26**	inhibition of the channel 26
7	**Trig_inhi _c25**	inhibition of the channel 25
8	**Trig_inhi _c24**	inhibition of the channel 24
9	**Trig_inhi _c23**	inhibition of the channel 23
10	**Trig_inhi _c22**	inhibition of the channel 22
11	**Trig_inhi _c21**	inhibition of the channel 21
12	**Trig_inhi _c20**	inhibition of the channel 20
13	**Trig_inhi _c19**	inhibition of the channel 19
14	**Trig_inhi _c18**	inhibition of the channel 18
15	**Trig_inhi _c17**	inhibition of the channel 17
16	**Trig_inhi _c16**	inhibition of the channel 16
17	**Trig_inhi _c15**	inhibition of the channel 15
18	**Trig_inhi _c14**	inhibition of the channel 14
19	**Trig_inhi _c13**	inhibition of the channel 13
20	**Trig_inhi _c12**	inhibition of the channel 12
21	**Trig_inhi _c11**	inhibition of the channel 11
22	**Trig_inhi _c10**	inhibition of the channel 10
23	**Trig_inhi _c9**	inhibition of the channel 9
24	**Trig_inhi _c8**	inhibition of the channel 8
25	**Trig_inhi _c7**	inhibition of the channel 7
26	**Trig_inhi _c6**	inhibition of the channel 6
27	**Trig_inhi _c5**	inhibition of the channel 5
28	**Trig_inhi _c4**	inhibition of the channel 4
29	**Trig_inhi _c3**	inhibition of the channel 3
30	**Trig_inhi _c2**	inhibition of the channel 2
31	**Trig_inhi _c1**	inhibition of the channel 1

Table 34: Description of the register 8.

7.6. J The register 9

This 32-bit register permits to inhibit the discriminator of specific channel. The mapping for the channel 33 to 64 is given in the table 35.

bit	name	action
0	**Trig_inhi_c33**	inhibition of the channel 33
1	**Trig_inhi _c34**	inhibition of the channel 34
2	**Trig_inhi _c35**	inhibition of the channel 35
3	**Trig_inhi _c36**	inhibition of the channel 36
4	**Trig_inhi _c37**	inhibition of the channel 37
5	**Trig_inhi _c38**	inhibition of the channel 38
6	**Trig_inhi _c39**	inhibition of the channel 39
7	**Trig_inhi _c40**	inhibition of the channel 40
8	**Trig_inhi _c41**	inhibition of the channel 41
9	**Trig_inhi _c42**	inhibition of the channel 42
10	**Trig_inhi _c43**	inhibition of the channel 43
11	**Trig_inhi _c44**	inhibition of the channel 44
12	**Trig_inhi _c45**	inhibition of the channel 45
13	**Trig_inhi _c46**	inhibition of the channel 46
14	**Trig_inhi _c47**	inhibition of the channel 47
15	**Trig_inhi _c48**	inhibition of the channel 48
16	**Trig_inhi _c49**	inhibition of the channel 49
17	**Trig_inhi _c50**	inhibition of the channel 50
18	**Trig_inhi _c51**	inhibition of the channel 51
19	**Trig_inhi _c52**	inhibition of the channel 52
20	**Trig_inhi _c53**	inhibition of the channel 53
21	**Trig_inhi _c54**	inhibition of the channel 54
22	**Trig_inhi _c55**	inhibition of the channel 55
23	**Trig_inhi _c56**	inhibition of the channel 56
24	**Trig_inhi _c57**	inhibition of the channel 57
25	**Trig_inhi _c58**	inhibition of the channel 58
26	**Trig_inhi _c59**	inhibition of the channel 59
27	**Trig_inhi _c60**	inhibition of the channel 60
28	**Trig_inhi _c61**	inhibition of the channel 61
29	**Trig_inhi _c62**	inhibition of the channel 62
30	**Trig_inhi _c63**	inhibition of the channel 63
31	**Trig_inhi _c64**	inhibition of the channel 64

Table 35: Description of the register 9.

7.6. K The register 10

This 32-bit register permits to enable the SCA readout for the specified channels (1 to 32). The mapping for the channel 1 to 32 is given in the table 36.

bit	name	action
0	**Sca_inhi_c32**	SCA read enable of the channel 32
1	**Sca_inhi_c31**	SCA read enable of the channel 31
2	**Sca_inhi_c30**	SCA read enable of the channel 30
3	**Sca_inhi_c29**	SCA read enable of the channel 29
4	**Sca_inhi_c28**	SCA read enable of the channel 28
5	**Sca_inhi_c27**	SCA read enable of the channel 27
6	**Sca_inhi_c26**	SCA read enable of the channel 26
7	**Sca_inhi_c25**	SCA read enable of the channel 25
8	**Sca_inhi_c24**	SCA read enable of the channel 24
9	**Sca_inhi_c23**	SCA read enable of the channel 23
10	**Sca_inhi_c22**	SCA read enable of the channel 22
11	**Sca_inhi_c21**	SCA read enable of the channel 21
12	**Sca_inhi_c20**	SCA read enable of the channel 20
13	**Sca_inhi_c19**	SCA read enable of the channel 19
14	**Sca_inhi_c18**	SCA read enable of the channel 18
15	**Sca_inhi_c17**	SCA read enable of the channel 17
16	**Sca_inhi_c16**	SCA read enable of the channel 16
17	**Sca_inhi_c15**	SCA read enable of the channel 15
18	**Sca_inhi_c14**	SCA read enable of the channel 14
19	**Sca_inhi_c13**	SCA read enable of the channel 13
20	**Sca_inhi_c12**	SCA read enable of the channel 12
21	**Sca_inhi_c11**	SCA read enable of the channel 11
22	**Sca_inhi_c10**	SCA read enable of the channel 10
23	**Sca_inhi_c9**	SCA read enable of the channel 9
24	**Sca_inhi_c8**	SCA read enable of the channel 8
25	**Sca_inhi_c7**	SCA read enable of the channel 7
26	**Sca_inhi_c6**	SCA read enable of the channel 6
27	**Sca_inhi_c5**	SCA read enable of the channel 5
28	**Sca_inhi_c4**	SCA read enable of the channel 4
29	**Sca_inhi_c3**	SCA read enable of the channel 3
30	**Sca_inhi_c2**	SCA read enable of the channel 2
31	**Sca_inhi_c1**	SCA read enable of the channel 1

Table 36: Description of the register 10.

7.6. L The register 11

This 32-bit register permits to enable the SCA readout for the specified channels (33 to 64). The mapping for the channel 33 to 64 is given in the table 37.

bit	name	action
0	**Sca_inhi_c33**	SCA read enable of the channel 33
1	**Sca_inhi_c34**	SCA read enable of the channel 34
2	**Sca_inhi_c35**	SCA read enable of the channel 35
3	**Sca_inhi_c36**	SCA read enable of the channel 36
4	**Sca_inhi_c37**	SCA read enable of the channel 37
5	**Sca_inhi_c38**	SCA read enable of the channel 38
6	**Sca_inhi_c39**	SCA read enable of the channel 39
7	**Sca_inhi_c40**	SCA read enable of the channel 40
8	**Sca_inhi_c41**	SCA read enable of the channel 41
9	**Sca_inhi_c42**	SCA read enable of the channel 42
10	**Sca_inhi_c43**	SCA read enable of the channel 43
11	**Sca_inhi_c44**	SCA read enable of the channel 44
12	**Sca_inhi_c45**	SCA read enable of the channel 45
13	**Sca_inhi_c46**	SCA read enable of the channel 46
14	**Sca_inhi_c47**	SCA read enable of the channel 47
15	**Sca_inhi_c48**	SCA read enable of the channel 48
16	**Sca_inhi_c49**	SCA read enable of the channel 49
17	**Sca_inhi_c50**	SCA read enable of the channel 50
18	**Sca_inhi_c51**	SCA read enable of the channel 51
19	**Sca_inhi_c52**	SCA read enable of the channel 52
20	**Sca_inhi_c53**	SCA read enable of the channel 53
21	**Sca_inhi_c54**	SCA read enable of the channel 54
22	**Sca_inhi_c55**	SCA read enable of the channel 55
23	**Sca_inhi_c56**	SCA read enable of the channel 56
24	**Sca_inhi_c57**	SCA read enable of the channel 57
25	**Sca_inhi_c58**	SCA read enable of the channel 58
26	**Sca_inhi_c59**	SCA read enable of the channel 59
27	**Sca_inhi_c60**	SCA read enable of the channel 60
28	**Sca_inhi_c61**	SCA read enable of the channel 61
29	**Sca_inhi_c62**	SCA read enable of the channel 62
30	**Sca_inhi_c63**	SCA read enable of the channel 63
31	**Sca_inhi_c64**	SCA read enable of the channel 64

Table 37: Description of the register 11.

7.6. M The register 12

This 16-bit register permits to define the Trigger Latency. Only the first 9 bits are currently used (table 38).

bit	name	action
0	**TrigLat<0>**	Lsb of the Trigger Latency value
1	**TrigLat<1>**	
2	**TrigLat<2>**	
3	**TrigLat<3>**	
4	**TrigLat<4>**	
5	**TrigLat<5>**	
6	**TrigLat<6>**	
7	**TrigLat<7>**	
8	**TrigLat<8>**	Msb of the Trigger Latency value

Table 38: Description of the register 12.

8. The power supply connections

A significant number of pins of the DREAM chip (19 Vdd; 19 Gnd) are dedicated to power supplies. The analog channels of DREAM are split into 2 groups of 32, for matching a square package. The height of these 2 groups (8 mm) and the sensitivity of each block (CSA, CR, SK, G-2, Discriminator & Dac threshold) imply to supply these blocks independently. This is also true for the SCA powering.

All the Vdd (Gnd) pads can be connected to the same PCB Vdd (Gnd) plan. A decoupling ceramic capacitor of 100 nF must be put very shortly to each Vdd connection point. An additional capacitor of 10 µF must be added for the pads: 36, 63, 98, 99, 115 & 127.

8.1 The cavity connection

The substrat (P type) of the chip must be connected to the ground. This is done by connecting the bottom of the package cavity with 3 pins in each corner (**Fig. 18**).

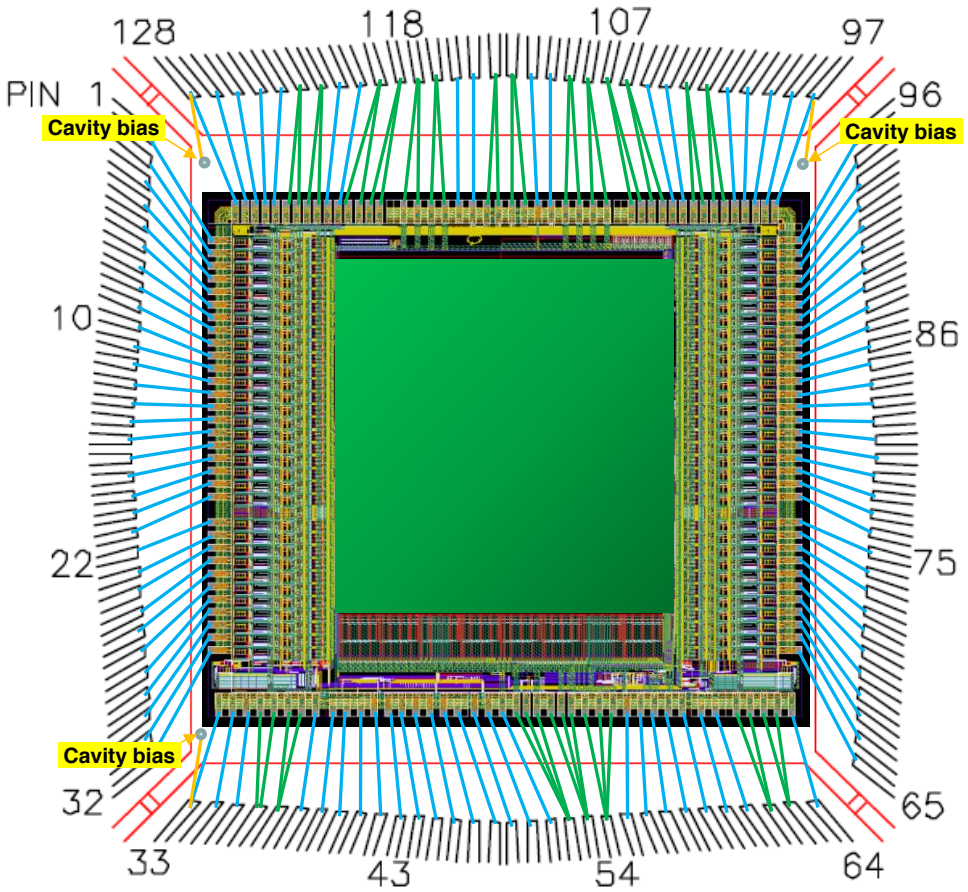


Fig. 18**:** Bonding diagram of the DREAM chip.

N° pin	Name	Current value	Description
33	**Gnd_Substrat**	*0 A*	*Cavity; Protection diodes [33 to 64]; SCA digital guard ring; Slow Control + left part (1to32).*
97	**Gnd_Substrat**	*0 A*	*Cavity; Protection diodes [65 to 96].*
128	**Gnd_Substrat**	*0 A*	*Cavity; Protection diodes [1 to 32].*

Table 39: Pins for the cavity connection.

8.2 The protection diode bias

All the pins of the chip are protected by internal diodes. The power supplies of these diodes are carried out by independent pins and are used also to supply others “quiet” parts of the chip.

N° pin	Name	I	Description
33	Gnd_Substrat	0 A	*Gnd for Cavity; Protection diodes [33 to 64]; SCA guard ring; Slow Control + left part (channel 1to32).*
34	Vdd_prob	0 A	*Vdd for Protection diodes [33 to 64]; Slow Control + left part (channel 1to32).*
97	Gnd_Substrat	0 A	*Gnd for Cavity; Protection diodes [65 to 96].*
98	Vdd_proind	0 A	*Vdd for Protection diodes [65 to 96].*
112	Vdd_proh	0 A	*Vdd for HIT & Slow control right; Protection diodes [99 to 126].*
113	Gnd_proh	0 A	*Gnd for HIT & Slow control right; Protection diodes [99 to 126].*
127	Vdd_proing	0 A	*Vdd for Protection diodes [1 to 32].*
128	Gnd_Substrat	0 A	*Gnd for Cavity; Protection diodes [1 to 32].*

Table 40: Pins for the protection diodes bias.

8.3 The front-end bias

The front-end is made of 5 blocks: CSA, PZC, SK, Gain-2 & HIT (Gain & Discriminator). Each of them uses dedicated pins for power supplies, excepted for the Trigger block. The analog & digital aspect of this functionality and the lake of free pins have push to use the bias of other blocks.

8.3.A The CSA bias

The DC power consumption current depends on the value of CSA nominal bias current set internally by 2-bit slow control state1<1:0>.

N° pin	Name	Idc (mA)	Description
36	Vdd_csag	*10.9/12.3/17.36/24.15 (4.65 in standby mode)*	*Vdd & Gnd:* • *CSA (1 to 32)* • *$DAC_{threshold}$ (1 to 32)*
37	Gnd_csag	*10.9/12.3/17.36/24.15 (4.65 in standby mode)*	
125	Gnd_csag	*10.9/12.3/17.36/24.15 (4.65 in standby mode)*	
126	Vdd_csag	*10.9/12.3/17.36/24.15 (4.65 in standby mode)*	
62	Gnd_csad	*10.9/12.3/17.36/24.15 (4.65 in standby mode)*	*Vdd & Gnd:* • *CSA (33 to 64)* • *$DAC_{threshold}$ (33 to 64)*
63	Vdd_csad	*10.9/12.3/17.36/24.15 (4.65 in standby mode)*	
99	Vdd_csad	*10.9/12.3/17.36/24.15 (4.65 in standby mode)*	
100	Gnd_csad	*10.9/12.3/17.36/24.15 (4.65 in standby mode)*	

Table 41: Pins for the CSA bias.

8.3.B The Pole-Zero-Cancellation stage bias

N° pin	Name	Idc (mA)	Description
102	Vdd_crd	*10.6 (2.2 in standby mode)*	*Vdd & Gnd for PZC channel 33 to 64.*
103	Gnd_crd	*10.6 (2.2 in standby mode)*	
122	Gnd_crg	*10.6 (2.2 in standby mode)*	*Vdd & Gnd for PZC channel 1 to 32.*
123	Vdd_crg	*10.6 (2.2 in standby mode)*	

Table 42: Pins for the PZC bias.

8.3.C The SK filter stage bias

N° pin	Name	Idc (mA)	Description
104	Gnd_skd	*3.53 (1.5 in standby mode)*	*Vdd & Gnd for SK filter channel 33 to 64.*
105	Vdd_skd	*3.53 (1.5 in standby mode)*	
120	Gnd_skg	*3.53 (1.5 in standby mode)*	*Vdd & Gnd for SK filter channel 1 to 32.*
121	Vdd_skg	*3.53 (1.5 in standby mode)*	

Table 43: Pins for the SK filter bias.

8.3.D The inverting Gain-2 stage bias

N° pin	Name	Idc (mA)	Description
106	Vdd_g2d	23.43	Vdd & Gnd: • $Gain_{-2}$ (33 to 64) • $Gain_{threshold}$ (33 to 64) • $Discri_{input}$ (33 to 64)
107	Gnd_g2d	23.43	
122	Gnd_g2g	23.43	Vdd & Gnd: • $Gain_{-2}$ (1 to 32) • $Gain_{threshold}$ (1 to 32) • $Discri_{input}$ (1 to 32)
123	Vdd_g2g	23.43	

Table 44: Pins for the Gain-2 bias.

8.4 The SCA power supplies

The SCA is divided into 4 parts: The matrix (512 x 64 analog cells), the input stage “return buffers” (1 per line), the SCA read amplifier (1 per line) and the digital part (clock, address …).

8.4.A The analog memory cell matrix

The supply of the matrix is made by a metal grid on its entire surface. This grid is connected to the power bus supply of the return and output buffers. The DC power consumption of this part is zero.

8.4.B The “return buffer” amplifiers

This stage buffers the Vreturn voltage (Vref_sca [pin n° 111]) to provide it as a reference to the memory cells.

N° pin	Name	Idc (mA)	Description
116	Vdd	3.4	Vdd & Gnd: Return buffer & Matrix
117	Gnd	3.4	

Table 45: Pins for the “return buffer” amplifiers.

8.4.C The SCA read amplifiers

This amplifier is used to read back the analog data stored in the memory cells. It is active only during the read phase. Its power consumption value is adjustable by slow control (2-bit state2<13:12>).

N° pin	Name	Idc (mA)	Description
108	Vdd	15/19/27.5/50	Vdd & Gnd: SCA readout amplifiers & Matrix
109	Gnd	15/19/27.5/50	

Table 46: Pins for the SCA read amplifiers.

8.4.D The SCA digital part

This part generates and distributes the signals required for the writing and reading operations in the SCA.

N° pin	Name	Idc (mA)	Description
53	Gnd	0.509	Vdd & Gnd for SCA logic& LVDS receivers
54	Vdd	0.509	

Table 47: Pins for the SCA digital part.

8.4.E The SCA guard ring

An important point concerns the parasitic injection charge through the substrat between the SCA (the noise source) and the front-end (CSA input). So, particularity care has been taken into account by putting guard ring around the SCA. The supply of these 2 rings (pplus&nplus diffusion) is done by 2 specific pads.

N° pin	Name	Idc (mA)	Description
51	**Vdd**	*0*	*Vdd & Gnd for SCA guard ring*
52	**Gnd**	*0*	

Table 48: Pins for the SCA guard ring.

8.5 The readout output buffers

This section of the chip includes the analog output multiplexer, the several intermediate buffers and the differential output buffer. The bias current of the intermediate buffers is controlling by the state2<15:14>.

N° pin	Name	Idc (mA)	Description
57	**Vdd_out**	*17.3*	*Vdd & Gnd for the readout output & SCA buffers*
64	**Gnd**	*17.3*	

Table 49: Pins for the readout output buffers.

8.6 The channel power consumption

The chip power consumption depends of the CSA bias current value and also of the one chooses to optimize the readout of the analog data (bias of the output buffers). For a CSA bias nominal value of ***400 µA***, the power consumption per channel will be around ***8.7 mW***; ***11.34 mW*** for CSA bias value of ***1.2 mA.***

9. The DC voltage references

The DREAM chip needs DC reference voltages to bias the inputs or outputs of its functional blocks. All these voltages are defined internally (except for ***Vocm*** (pad 55)) and are accessible through some pads (table 50). For the DC voltage ***Vref_sca***, it is necessary to decrease the input impedance by putting external resistor bridge (511 Ω to Vdd and 147 Ω to the ground for DC voltage of 0.736 V).

For high frequency noise reduction, all these pads must be bypassed to ground by a 100 nF ceramic capacitor.

N° pin	Name	Description
55	**Vocm**	*Common mode output voltage of the SCA readout buffer*
56	**Vicm**	*Common mode input voltage of the SCA readout buffer*
101	**Vreg_csad**	*Regulator voltage of the CSA input transistors (channel 33 to 64)*
110	**Vdc_g2**	*DC output level voltage of Gain-2*
111	**Vref_sca**	*DC reference level voltage of SCA and Gain-2 input*
114	**Vdc_c**	*DC output level voltage of the PZC & SK filters*
115	**Vdc_csa**	*DC output level voltage of the CSA*
124	**Vreg_csag**	*Regulator voltage of the CSA input transistors (channel 1 to 32)*

Table 50: Pins for the DC voltage references.

10. Specifications for digital signals

The DREAM chip uses two types of digital inputs:
- LVDS differential inputs. These inputs are not internally terminated (differential input resistance > 10 Mohm).
- CMOS inputs (high level = VDD, low level = 0).

Two types of digital outputs are available:
- CMOS outputs (high level = VDD, low level = 0).
- LVDS compatible outputs as shown on **Fig 19**.

Considering LVDS outputs:

An external terminating resistor Rout must be connected between the positive and negative outputs of the signal at the receiver level. The high level is defined by a 3mA current circulating from the positive output to the negative input through the external terminating resistor. This current is inverted in case of a low LVDS level.

Name	Description	Min	Typ.	Max
VDD	Power supply voltage	3.2V	3.3V	3.4V
PVDD	Total power			
Vcmm LVDSin	Common mode for LVDS inputs	0.6V	1.2 V	3V
Vswing LVDSin	LVDS input swing	0.2V	0.4 V	
VCMOSin_l	Low level for CMOS input	-0.2V	0	VSS+0.6V
VCMOSin_h	High level for CMOS input	2	3.3	3.5V
Rin_dig	Input resistance for the digital inputs (CMOS or LVDS)	10 MOhm		
Cin_ding	Input capacitance for the digital inputs		4pF	
Iout	Current for LVDS outputs		3mA	
Rout	External load resistance required for LVDS outputs		100 Ohm	
Vcout	Common mode voltage for LVDS outputs		1.25V	
Vswing out	LVDS differential output swing (3mA setting, 100 Ohm load)		600mV	
VCMOSout_l	Low CMOS output level	0V	0V	0.4V
VCMOSout_h	High CMOS output	2.9V	3.3V	3.3V
ICMOSout	Maximum current for CMOS outputs			4 mA

Table 51: specifications for digital signals.

The common mode output voltage (Voutp+Voutm)/2 is internally set to **1.25V**. In the standard mode of operation, Rout=100 Ohm (to properly terminate a 100 Ohm impedance differential line), as Iout =3mA, the voltage levels on the 2 outputs are 1.5V and 0.9V, giving a differential voltage swing compatible with standard LVDS receiver.

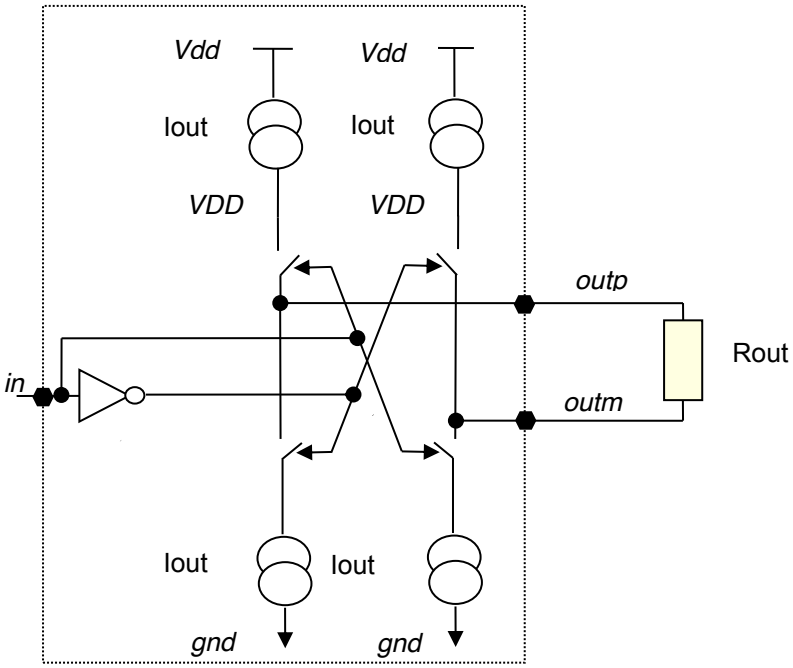


Fig 19: Principle of a LVDS compatible output.

11. Timing Specifications.

The table 52 summarizes the main timing requirements for the DREAM chip. The setup, hold and delay times standard definitions are shown on Fig 20.

Type	Signal	Signal edge	Clock	Clock edge	Min	Typ	Max	Unit
Frequency			***RCk*** (Slow Control)				20	*MHz*
Duty Cycle			***RCk*** (Slow Control)		0.4	0.5	0.6	
Setup	***sc_en***	**both**	***RCk***	**-**	10			*ns*
Hold	***sc_en***	**both**	***RCk***	**-**	10			*ns*
Setup	***sc_din***	**both**	***RCk***	**-**	10			*ns*
Hold	***sc_din***	**both**	***RCk***	**-**	10			*ns*
Propagation	***Sc_dout***		***RCk***				30	*ns*
Frequency			***RCk*** (Readout)				20	*MHz*
Duty Cycle			***RCk*** (Readout)		0.4	0.5	0.6	*ns*
Frequency			***WCk***	**+**		20	50	*MHz*
Duty Cycle			***WCk***	**+**	0.4	0.5	0.6	
Setup	***Write***	**both**	***WCk***	**+**	5			*ns*
Hold	***Write***	**both**	***WCk***	**+**	5			*ns*
Setup	***Trig***	**both**	***WCk***	**+**	5			*ns*
Hold	***Trig***	**both**	***WCk***	**+**	5			*ns*
Setup	***Read***	**+**	***RCk***	**+**	5			*ns*
Setup	***Read***	**-**	***WCk***	**+**	5			*ns*
Hold	***Read***	**-**	***WCk***	**+**	4			*WCK periods*
Aperture	***Analog Sampling***		***WCK***	**+**		TBD		*ns*
Delay	***Analog Out***		***RCK***	**+**		10		*ns*

Table 52: Timing Requirements.

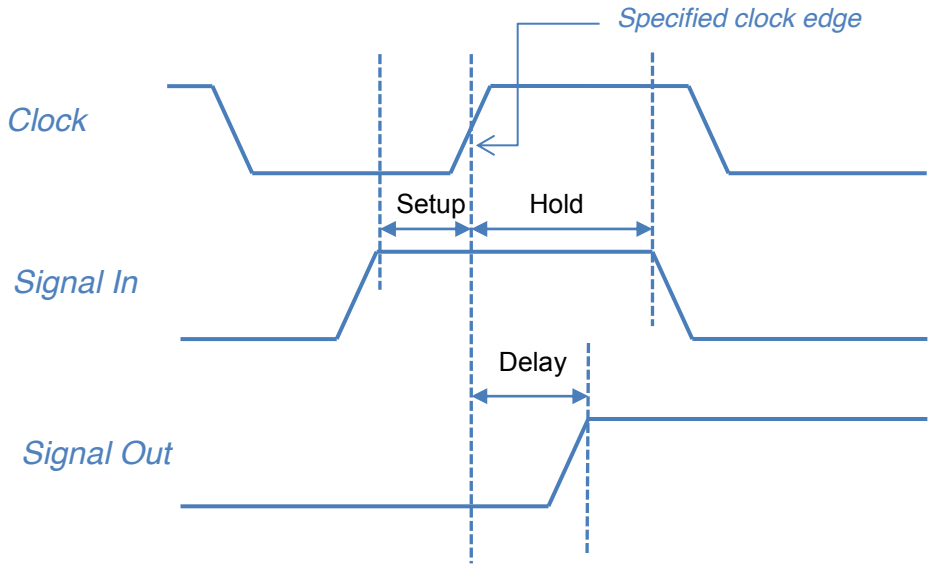


Fig 20: Definition of the timing parameters.

12. Pinout of the DREAM chip.

The DREAM chip is housed in a 128-pin Low Quad Flat Pack (LQFP-128). The package body dimensions are 14 x 14 x 1.4 mm. Its pitch is 0.4 mm with 2 mm footprint. The pin configuration is given in the **Fig. 21**.

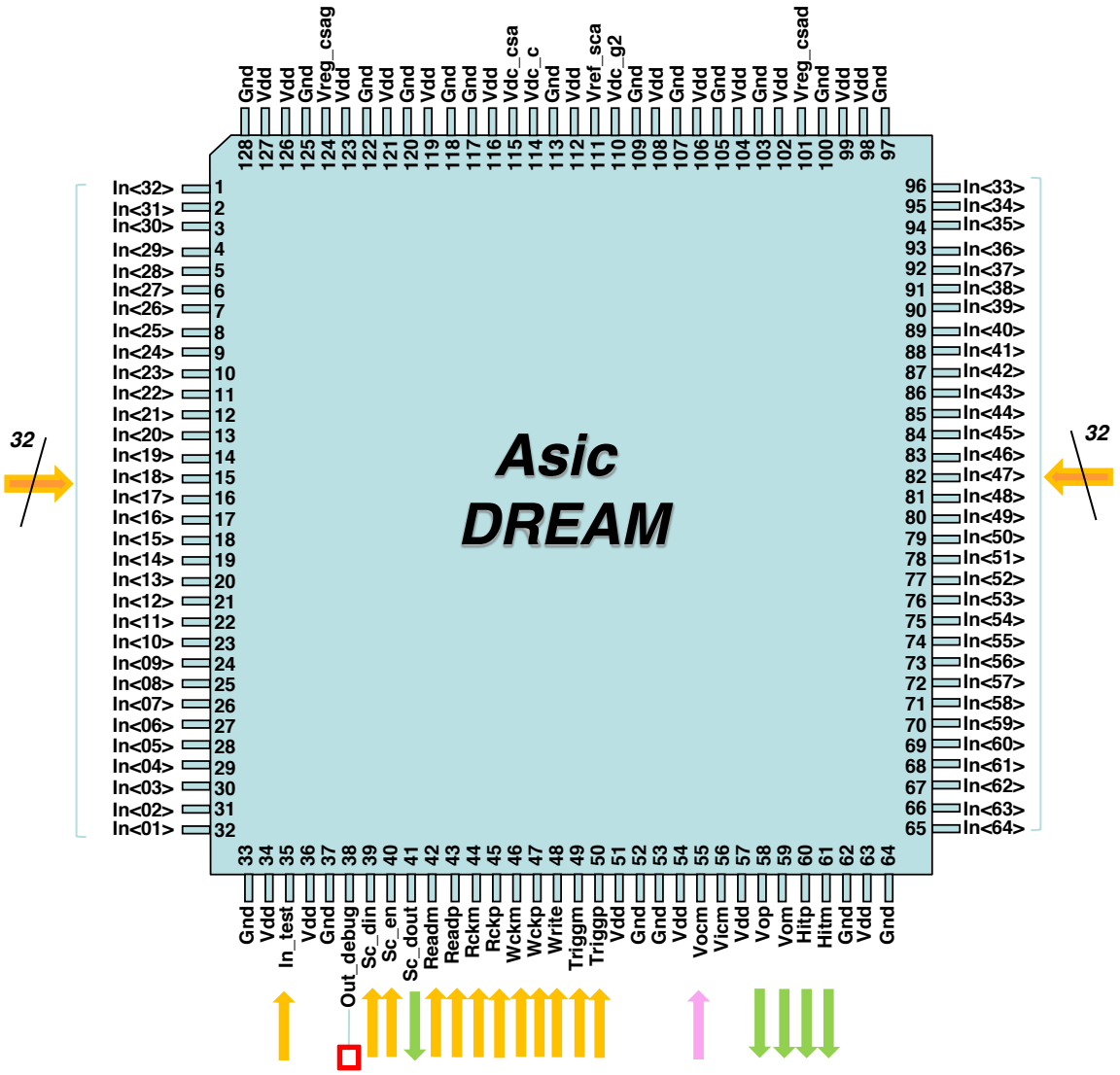


Fig. 21**:** Pinout of the DREAM chip.

The pin function descriptions of the chip are reported in the table 53.

N° Pin	*Name*	*Dir.*	*Level*	*Description*
1 to 32	**In<32> to In<01>**	In	Analog	Inputs of channels 32 to 1
33	**gnd**	In	0V	Gnd for protection diode [33 to 64], cavity, Slow Control
34	**Vdd_prob**	In	3.3V	Vdd for protection diode [33 to 64], Slow Control
35	**In_test**	In	Analog	Input for the test, functionality or calibration
36	**Vdd_csag**	In	3.3V	Vdd for the csa of the channels 32 to 1 & Threshold DAC
37	**gnd**	In	0V	Gnd for the csa of the channels 32 to 1 & Threshold DAC
38	**Out_debug**	Out	Analog	Output of the “spy” mode: “analog” or “SCA”
39	**Sc_din**	In	CMOS 3.3V	Serial data input of Slow Control
40	**Sc_en**	In	CMOS 3.3V	Chip Select input of Slow Control
41	**Sc_dout**	Out	CMOS 3.3V	Serial data output of Slow Control
42	**Readm**	In	LVDS	SCA negative read mode
43	**Readp**	In	LVDS	SCA positive read mode
44	***RCk*m**	In	LVDS	SCA or Slow Control Negative read clock

45	***RCkp***	In	LVDS	SCA or Slow Control Positive read clock
46	***WCkm***	In	LVDS	SCA Negative write clock
47	***WCkp***	In	LVDS	SCA Positive write clock
48	**Write**	In	CMOS 3.3V	SCA write init mode
49	**Triggerm**	In	LVDS	Trigger Negative input signal
50	**Triggerp**	In	LVDS	Trigger Positive input signal
51	**vdd**	In	3.3V	Vdd SCA guard ring
52	**gnd**	In	0V	Gnd SCA guard ring
53	**gnd**	In	0V	Gnd SCA logic
54	**vdd**	In	3.3V	Vdd SCA logic
55	**vocm**	In	ADC vicm	Common mode output voltage of the Readout buffer
56	**vicm**	In	Analog	Common mode input voltage of the Readout buffer
57	**Vdd_out**	In	3.3V	Vdd of the Readout buffer & SCA buffer
58	**vop**	Out	Analog	Positive output of the Readout buffer
59	**vom**	Out	Analog	Negative output of the Readout buffer
60	**Hitp**	Out	LVDS	Hit Positive output signal + SCA internal signals
61	**Hitm**	Out	LVDS	Hit Negative output signal + SCA internal signals
62	**gnd**	In	0V	Gnd for the CSA of the channels 33 to 64 & Threshold DAC
63	**Vdd_csad**	In	3.3V	Vdd for the CSA of the channels 33 to 64 & Threshold DAC
64	**gnd**	In	0V	Gnd buffer out, logic
65 to 96	**In<64> to In<33>**	In	Analog	Inputs of channels 64 to 33
97	**gnd**	In	0V	Gnd for protection diode [33 to 64] & cavity
98	**Vdd_proind**	In	3.3V	Vdd for protection diode [33 to 64]
99	**Vdd_csad**	In	3.3V	Vdd for the CSA of the channels 33 to 64 & Threshold DAC
100	**gnd**	In	0V	Gnd for the CSA of the channels 33 to 64 & Threshold DAC
101	**Vreg_csad**	Out	Analog	Regulator voltage of the input transistors of CSA [33 to 64]
102	**Vdd_crd**	In	3.3V	Vdd for the PZC of the channels 33 to 64
103	**gnd**	In	0V	Gnd for the PZC of the channels 33 to 64
104	**Vdd_skd**	In	3.3V	Vdd for the SK filter of the channels 33 to 64
105	**gnd**	In	0V	Gnd for the SK filter of the channels 33 to 64
106	**Vdd_g2d**	In	3.3V	Vdd for the Gain -2 of the channels 33 to 64; Threshold gain & LEAD input stage.
107	**gnd**	In	0V	Gnd for the Gain -2 of the channels 33 to 64; Threshold gain & LEAD input stage.
108	**Vdd**	In	3.3V	Vdd SCA Readout Amplifier + Matrix
109	**gnd**	In	0V	Gnd SCA Readout Amplifier + Matrix
110	**Vdc_g2**	Out	0.7V [2.2V]	DC output level voltage of the Gain-2
111	**vref_sca**	Out	0.7V	DC reference level voltage of the SCA and Gain-2 input
112	**vdd_proh**	In	3.3V	Vdd for protection diode [99 to 126], Trigger & Slow Control right
113	**gnd**	In	0V	Gnd for protection diode [99 to 126], Trigger & Slow Control right
114	**Vdc_c**	Out	2.2V [0.7V]	DC output level voltage of the PZC & SK filter
115	**Vdc_csa**	Out	1.8V [2.8V]	DC output level voltage of the CSA
116	**Vdd**	In	3.3V	Vdd return buffer + Matrix
117	**gnd**	In	0V	Gnd return buffer + Matrix
118	**gnd**	In	0V	Gnd for the Gain -2 of the channels 32 to 1; Threshold gain & LEAD input stage.
119	**Vdd_g2g**	In	3.3V	Vdd for the Gain -2 of the channels 32 to 1; Threshold gain & LEAD input stage.
120	**gnd**	In	0V	Gnd for the SK filter of the channels 32 to 1
121	**Vdd_skg**	In	3.3V	Vdd for the SK filter of the channels 32 to 1
122	**gnd**	In	0V	Gnd for the PZC of the channels 32 to 1
123	**Vdd_crg**	In	3.3V	Vdd for the PZC filter of the channels 32 to 1
124	**Vreg_csag**	Out	Analog	Regulator voltage of the input transistors of CSA [32 to 1]
125	**gnd**	In	0V	Gnd for the CSA of the channels 32 to 1 & Threshold DAC
126	**Vdd_csag**	In	3.3V	Vdd for the CSA of the channels 32 to 1 & Threshold DAC
127	**Vdd_proing**	In	3.3V	Vdd for protection diode [32 to 1]
128	**gnd**	In	0V	Gnd for protection diode [32 to 1] & cavity

Table 53: Description of the pins of the DREAM chip.

13. Layout of the DREAM chip

A picture of the DREAM chip layout is given in the **Fig. 22.** The circuit is manufactured using the AMS CMOS 0.35µm technology. The die area is 8591.5 µm (+240µm) x 7455.8 µm (+240 µm).

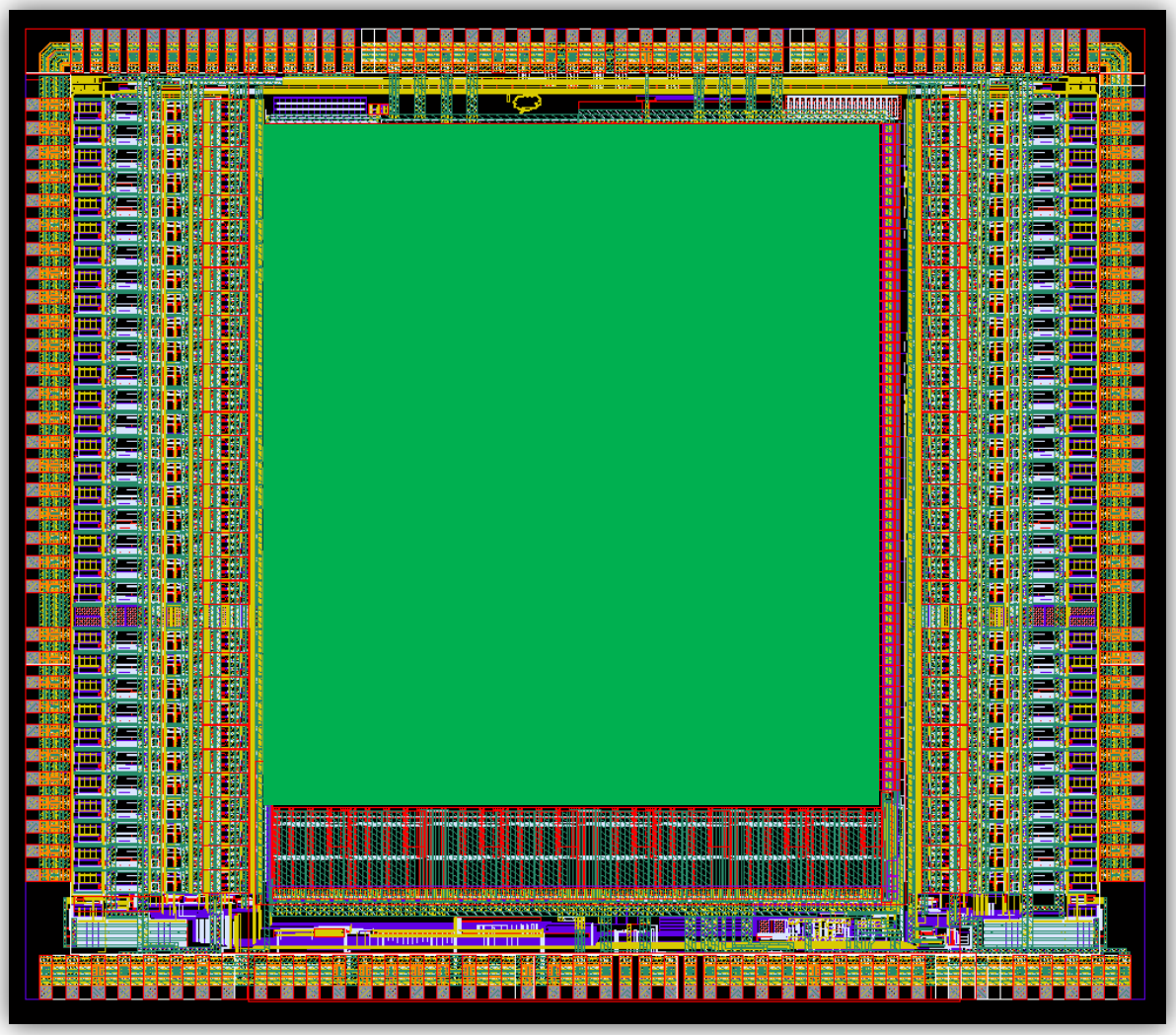


Fig. 22**:** Layout of the DREAM chip.

The DREAM chip integrates around 730 000 components (# 687 000 transistors; # 38 000 capacitors; # 5700 resistors).

Annexe 1: DREAM Package specifications

The description of the package is given in the **Fig. 23** & **Fig. 24**.

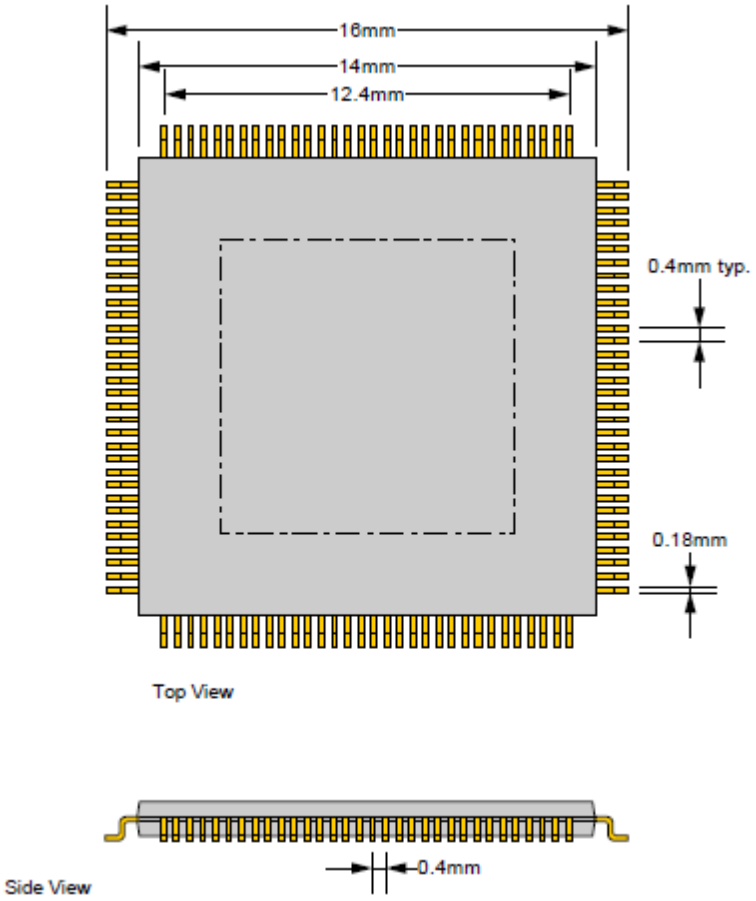
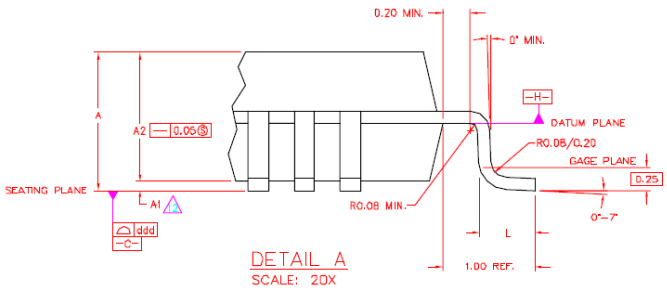


Fig. 23: Package description.



	LEAD COUNT Foot Print		
	128j 2.0 FP		
	Min	Nom	Max
A	----	----	1.6
A1	0.05	----	0.15
A2	1.35	1.40	1.45
D		16.00 BSC	
D1		14.00 BSC	
E		16.00 BSC	
E1		14.00 BSC	
L	0.45	0.6	0.75
e		0.40 BSC	
b	0.13	0.18	0.23
b1	0.13	0.16	0.19
	0.09	----	0.20
c1	0.09	----	0.16
aaa		0.2	
bbb		0.2	
ccc		0.07	
ddd		0.08	

Fig. 24: Package dimension.

Annexe 2: Bonding Diagram

The 152 pads of the chip are much greater than the available 128 pads of the package chosen (LQFP-128 pins). Therefore double or triple bonding must be necessary done to reduce the self & resistor effects of the bonding for the digital supplies (SCA) and analog supplies (CSA) of the chip. The bonding diagram of DREAM is reported in the **Fig. 25**.

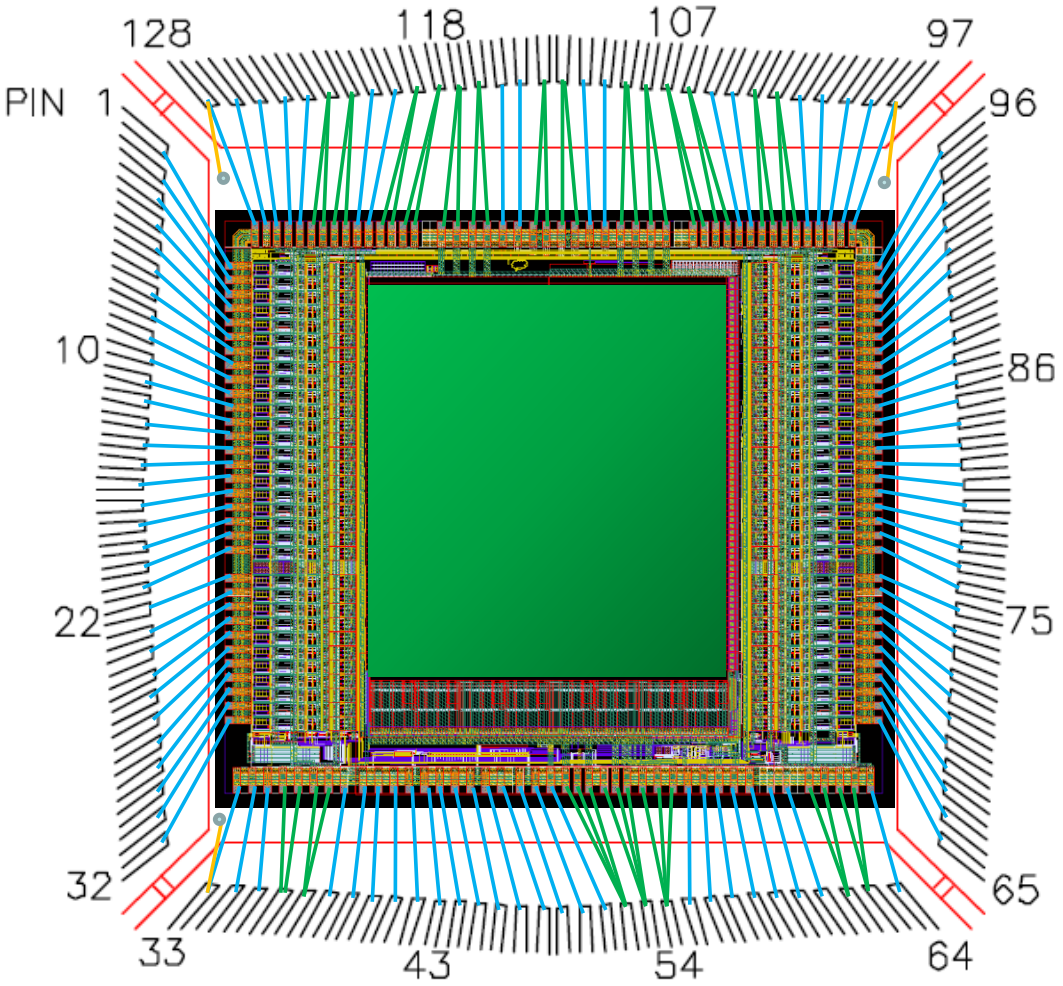


Fig. 25**:** Bonding diagram of the DREAM chip.

A double bonding is necessary for the package pin numbers: 33, 36, 37, 62, 63, 97, 102, 103, 106, 107, 108, 109, 112, 113, 116, 117, 118, 119, 122, 123 & 128.

A triple bonding for the package pin numbers: 52, 53 & 54.

The package pin numbers: 33, 97 & 128 are used to supply the cavity of the package (ASIC substrate).

Annexe 3: List of modifications

Few modifications have been made on the production version of DREAM circuit. This is the list of them.

A/ The CSA integration time constant can be now choose between 2 values: 5 µs (prototype version) or 50 µs. It implies one new slow control bit: state1<31>.

B/ The input dynamic range of 1 pC is replaced by 600 fC.

C/ The input dynamic range of the discriminator can be fixed to 5% or 17.5% of the input dynamic range of the analog channel. The new slow control bit state1<30> permits to define this gain.

D/ A new set of values for the filter is used to cover uniformly the range between 50 and 400 ns.

E/ A programmable threshold is settable on the multiplicity signal to generate the HIT signal. It requires new slow control bit state2<27:25>.

F/ The SCA read amplifier can be have or not working with a constant current. It is done by using new slow control bit state2<5>.

G/ The version number of the production version is set to: 0x0302 (0x0301 in previous version).

H/ It is now not possible to view the SCA “spy” signals independently on the two pads HITP&HITM in CMOS level. The SCA_SPY_0 is output to the pad Out_debug (pin n° 38) and the SCA_SPY_1 in LVDS level through the pads HITP&HITM (pin n° 60 & 61).

I/ The depth of the registers 8 & 9 is reduced to 32-bit (64-bit in the previous version).

Bibliography

- Ref.1: **AFTER, an ASIC for the Readout of the Large T2K Time Projection Chambers**

Baron, P. Calvet, D. Delagnes, E. de la Broise, X. Delbart, A. Druillole, F. Mazzucato, E. Monmarthe, E. Pierre, F. Zito, M. , **Nuclear Science, IEEE Transactions on**, June 2008 Volume: 55, Issue: 3, Part 3, page(s): 1744-1752.

- Ref. 2: **AGET, the GET front-end ASIC, for the readout of the Time Projection Chambers used in nuclear physic experiments**

Anvar, S; Baron, P.; Blank, B.; Chavas, J.; Delagnes, E.; Druillole, F.; Hellmuth, P.; Nalpas, L.; Pedroza, J.L.; Pibernat, J.; Pollacco, E.; Rebii,A.; Usher, N.
Nuclear Science Symposium and Medical Imaging Conference (NSS/MIC), 2011 IEEE
Digital Object Identifier: 10.1109/NSSMIC.2011.6154095
Publication Year: 2011, Page(s): 745 - 749
http://www-tpc-get.cea.fr/index.php