					_			1					
<u> 6</u>	Power/ GND	등	Push-buttons		/GA Interface	PS/2 Interface		Stereo Codec		<u> </u>	-		
XS40 Pin (J1,J3,J18)	<u>ا</u> ر	DIP Switch	nq-		lu te	쁄	"	0	2	PC Parallel Port	Oscillator		
8 ± ± ± ± ± ± ± ± ± ± ± ± ± ± ± ± ± ± ±	we	P S	ish	LEDS	Ϋ́	2/2	RAMs	e e	8051 uC	i i	, iii		
₩ <del>2</del>			٦.	Ë	>	2	ž	ž	8	2 2	ő	Function	
3	+5V			LSB0			۸٥					+5V power source Left LED segment; RAM address line	
4				LSB1			A0 A1					Left LED segment; RAM address line	
5				LSB2			A2					Left LED segment; RAM address line	
6		DIPSW4						SDOUT	P1.3			DIP switch; codec serial data output; uC I/O	
7		DIPSW1					LCEB		P1.0			DIP switch; left RAM chip-enable, uC I/O port	
8		DIPSW2					RCEB		P1.1			DIP switch; right RAM chip-enable, uC I/O port	
9		DIPSW3		D.D.o			D-7	MCLK	P1.2			DIP switch; codec master clock; uC I/O port	
10				DB8			D7		P0.7		CLK	LED; RAM data line; uC muxed address/data line  XS Board oscillator	
14									PSENB		CLK	uC program store-enable	
15									1 OLIVE			JTAG TDI; DIN	
16												JTAG TCK; CCLK	
17												JTAG TMS	
18				S5	RED1							XS Board LED segment; VGA color signal	
19				S6	HSYNCE							XS Board LED segment; VGA horiz. sync.	
20				S3	GREEN'							XS Board LED segment; VGA color signal	
23				S4	RED0							XS Board LED segment; VGA color signal	
24				S2	GREEN	)						XS Board LED segment; VGA color signal	
25 26				S0 S1	BLUE0 BLUE1							XS Board LED segment; VGA color signal XS Board LED segment; VGA color signal	
27				51	DLULI				P3.7 (R	D )		uC read line	
28				RDPB					P2.7			Right LED decimal-point; uC I/O port	
29									ALEB			uC address-latch-enable	
30												Serial EEPROM chip-enable	
32										PC_D6		PC parallel port data output	
34										PC_D7		PC parallel port data output	
35				DB5			D4		P0.4			LED; RAM data line; uC muxed address/data line	
36			DECETE						RST			uC reset	
37			RESETE	DB4			D3		XTAL1 P0.3			Pushbutton; uC clock	
39				DB3			D2		P0.3			LED; RAM data line; uC muxed address/data line LED; RAM data line; uC muxed address/data line	
40				DB2			D1		P0.1			LED; RAM data line; uC muxed address/data line	
41				DB1			D0		P0.0			LED; RAM data line; uC muxed address/data line	
44								CCLK		PC_D0		Codec control line; PC parallel port data output	
45								CDIN		PC_D1		Codec control line; PC parallel port data output	
46								CSB		PC_D2		Codec control line; PC parallel port data output	
47										PC_D3		PC parallel port data output	
48										PC_D4		PC parallel port data output	
49 50				RSB4			A12		P2.4	PC_D5		PC parallel port data output	
51				RSB2			A10		P2.4			Right LED segment; RAM address line; uC I/O port Right LED segment; RAM address line; uC I/O port	
	GND			K3b2			ATO		F Z.Z			Power supply ground	
	5.0V/3.3	RV.										5V/3.3V power supply (4000E/4000XL)	
55	0.0 170.0		PROGR	AM								XS40 configuration control	
56				RSB3			A11		P2.3			Right LED segment; RAM address line; uC I/O port	
57				RSB1			A9		P2.1			Right LED segment; RAM address line; uC I/O port	
58				RSB5			A13		P2.5			Right LED segment; RAM address line; uC I/O port	
59				RSB0			A8		P2.0			Right LED segment; RAM address line; uC I/O port	
60				RSB6			A14		P2.6			Right LED segment; RAM address line; uC I/O port	
61 62							OEB WEB		P3.6 (W	/D \		RAM output-enable RAM write-enable; uC I/O port	
65							CEB		F 3.0 (W	/K_)		XS Board RAM chip-enable	
66		DIPSW7	,				CLD	LRCK	P1.6	PC_S5		DIP switch; codec left-right channel switch; uC I/O port; PC paral	llel port status
67		J.: 0111	SPAREE	3	VSYNCE	3		Litoit	P1.7	. 0_00		Pushbutton; VGA vert. sync.; uC I/O port	port otatao
68						KB_CL	(		P3.4 (T	0)		PS/2 keyboard clock; uC I/O port	
69		DIPSW8				KB_DA	ГА		P3.1 (T)	XDC_S6		DIP switch; PS/2 keyboard serial data; uC I/O port; PC parallel p	ort status inpu
70		DIPSW6	)					SDIN	P1.5	PC_S3		DIP switch; codec serial input data; uC I/O port; PC parallel port	status input
71												JTAG TDI; DIN	
72												JTAG TDO; DOUT	
73										DC CZ		JTAG TCK; CCLK	
75		DIDOM						SCI IZ	D4 4	PC_S7		JTAG TDO; DOUT; PC parallel port status input	statue innest
77 78		DIPSW5		LSB3			A3	SCLK	P1.4	PC_S4		DIP switch; codec serial I/O clock; uC I/O port; PC parallel port s Left LED segment; RAM address line	ιαιυο ΠΙΡΟΙ
79				LSB4			A4					Left LED segment; RAM address line	
80				DB7			D6		P0.6			LED; RAM data line; uC muxed address/data line	
81				DB6			D5		P0.5			LED; RAM data line; uC muxed address/data line	
82				LSB5			A5					Left LED segment; RAM address line	
83				LSB6			A6					Left LED segment; RAM address line	
84				LDPB			A7					Left LED decimal-point; RAM address line	
								_					

