# 8 BIT TIMER

Used APB bus for this design and synchronous design (It means that all FFs must be inputted system clock.

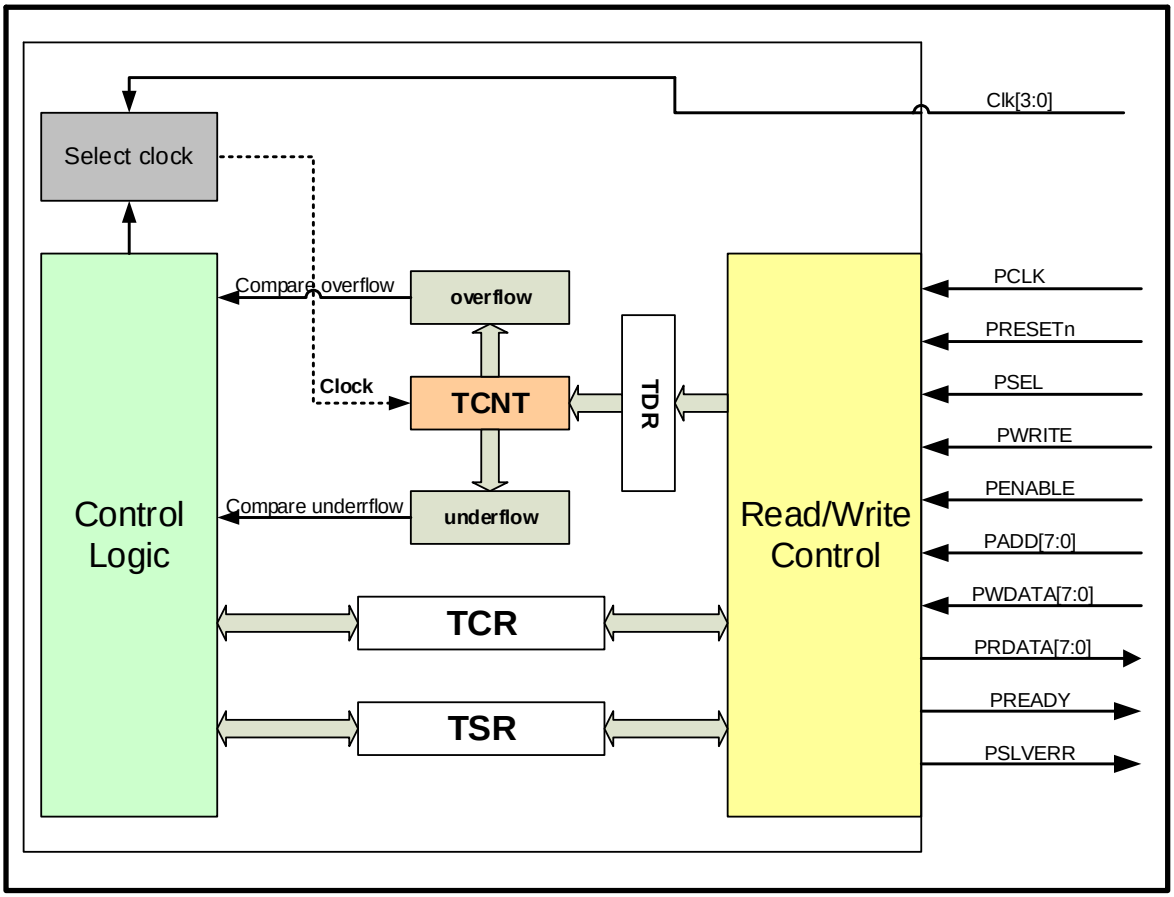



**Figure 8: Block diagram of TMR Block (Timer)**

- **Operation basic function:**

Timer Data Register (TDR): this register contains the data used for updating the value of counter when this register is updated to new value.

**Timer counter control Register (TCR):**

| Bit7 | Bit6 | Bit 5 | Bit4 | Bit3 | Bit2 | Bit1 | Bit0 |
|---|---|---|---|---|---|---|---|
| Load | Reserved | Up/Dw | En | Reserved | Reserved | cks1 | cks0 |

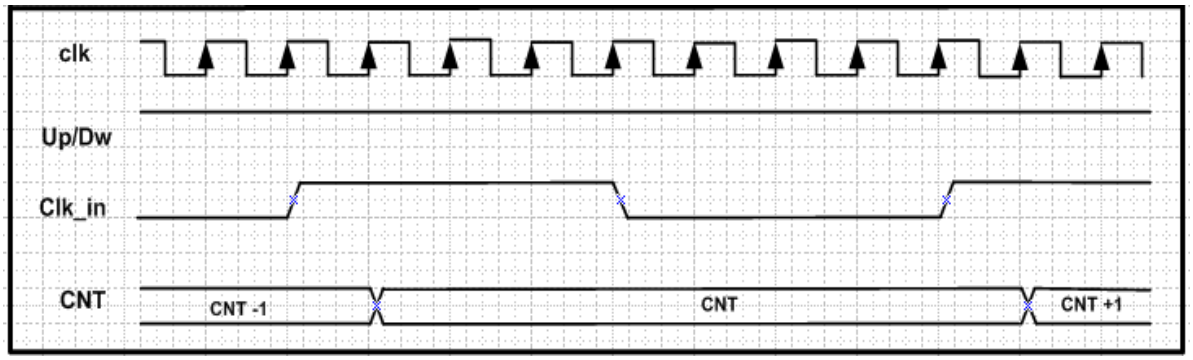
| Bit name | F/V | Description |
|---|---|---|
| Load[7] | R/W | Manual load data from TDR to TCNT when it active High.<br>1: load data to TCNT<br>0: Normal operation. |
| 6 | Reserved | Reserved |
| Up/Dw[5] | R/W | Control counter up or counter down<br>0: counter up<br>1: counter down |
| En[4] | R/W | 0 : disable<br>1: enable |
| 3:2 | Reserved | Reserved |
| cks[1:0] | R/W | Select internal clocks for circuit<br>00 : T*2<br>01 : T*4<br>10 : T*8<br>11: T*16 |

- Bit Description of TSR (Time Statue Register):

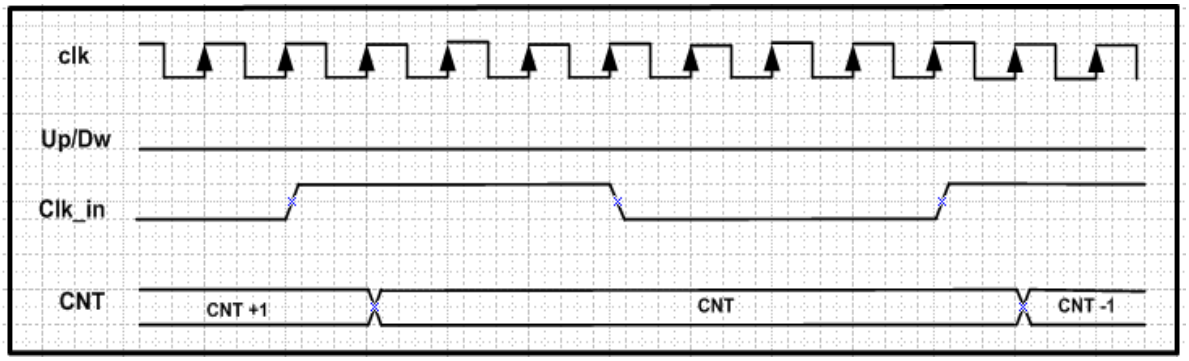
| Bit name | R/W | Description |
|---|---|---|
| 7:2 | R | Reserved |
| S_TMR_UDF[1] | R/W* | Timer counter underflow when counter 8'h00 down to 8'hff:<br>This bit is only set by hardware, clear by software |
| S_TMR_OVF[0] | R/W* | Timer counter overflow when counter 8'hFF to 8'h00:<br>This bit is only set by hardware, clear by software |

Functional Timing:

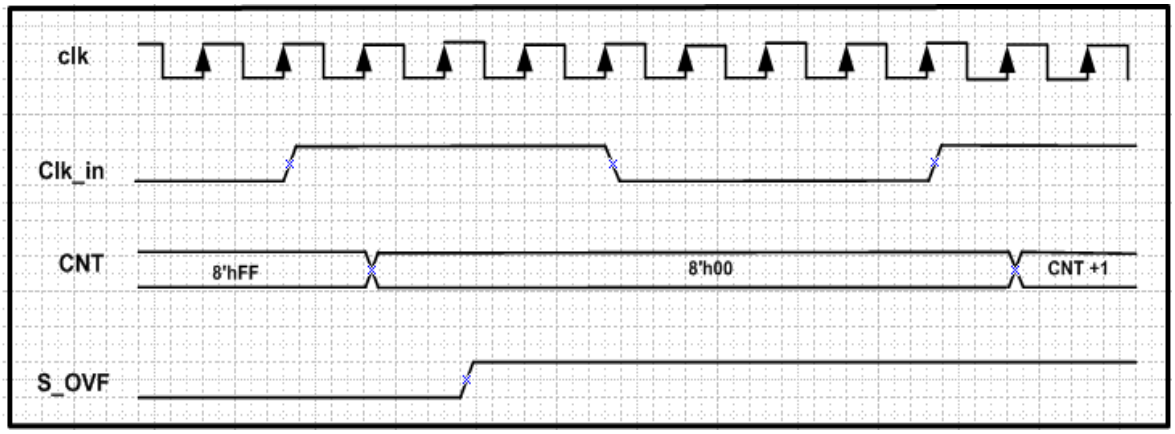
- Counter up



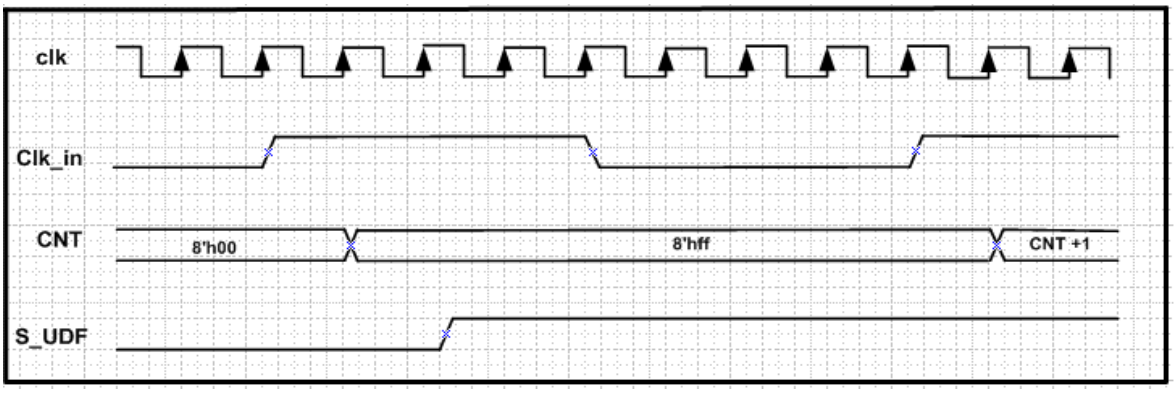

- Counter down




- Overflow



- Underflow




- **NOTES:**
  - **Design Rising Edge Circuit to apply the synchronous design for 8-bit Counter**
  - **Status bit OVF is set to 1 at the final system clock before counter changes from 8'hFF to 8'h00**
  - **Status bit UDF is set to 1 at the final system clock before counter changes from 8'h00 to 8'hFF**

- **Request with Basic function TMR**
  Analyzing the timing of signals and operation of circuit
  Building bock diagram of circuit
  Write testbench to verify 8-bit TMR.
  Debug coding.
  Do Verification
  Evaluate Code Coverage