## Report

Code starts by loading instructions and initialises their attributes, and then it checks if the current pc value instruction has been issued or not ( and that there are not branch stalls or structural hazard stalls), then it issues by finding a slot in the station, else if not set stall to true (structural hazard)

Execute checks that the instructions in the buffer were not just issued in this same cycle, and then checks if it can be executed or not (all the needed attributes are there), then starts executing.

If finished, it adds the instruction to a queue to be written

In write back, it checks if there are any instructions ready to be written to the bus, and since we implement it using FIFO, whatever instruction finishes execution first will be first in queue to be written. Then after it is written the respective station is emptied, and anything awaiting that instruction updates its values.

## Assumptions used:

Register size is 64, first half is for int and the second half for floating, we also assumed that when we branch we always branch to the beginning of the code. Also the instruction types like ADD for example is able to handle both float and int, rather than using DADD and ADD.D)

## Test cases:

Input: LD F0 2 ADDI R12 R12 99 SD R12 1 SUBI R15 R15 5 BNEZ R15 LOOP ADDI R13 R13 99

## Result:

end is 6

Instruction to be issued: LD F0 2 false

stall is now false : false Issue cycle of LD F0 2 is 1

Clock Cycle: 1 PC Value: 1

Reservation Stations:

Adder:

```
Adder position0: Tag: A1
                             Start Cycle: -1 Execute End Cycle: -1 Busy: 0 Instruction
Type: None Vj: Vk: Qj:
                              Qk:
                                    A:
                                           Duration left: -1 Ready To Write: false
                             Start Cycle: -1 Execute End Cycle: -1 Busy: 0 Instruction
Adder position1: Tag: A2
Type: None Vi:
                                           Duration left: -1 Ready To Write: false
                  Vk: Qi:
                              Qk:
                                   A:
Adder position2: Tag: A3
                             Start Cycle: -1 Execute End Cycle: -1 Busy: 0 Instruction
Type: None Vi:
                                           Duration left: -1 Ready To Write: false
                  Vk: Qi:
                              Qk:
                                    A:
Multiplier:
Multiplier position0:
Tag: M1 Start Cycle: -1 Execute End Cycle: -1 Busy: 0 Instruction Type: None Vj:
                                                                                    Vk:
                                      Ready To Write: false
Qi:
     Qk:
           A:
                  Duration left: -1
Multiplier position1:
Tag: M2 Start Cycle: -1 Execute End Cycle: -1 Busy: 0 Instruction Type: None Vi
                                                                                    Vk:
Qj:
            A:
                  Duration left: -1
                                      Ready To Write: false
Load Buffers:
Load buffer position0:
Tag: L1 Busy: 1 Effective Address: 2 Start Cycle: -1 Execute End Cycle: -1 Duration left: 1
Ready To Write: false
Load buffer position1:
Tag: L2 Busy: 0 Effective Address: -1 Start Cycle: -1 Execute End Cycle: -1 Duration left:
      Ready To Write: false
-1
Load buffer position2:
Tag: L3 Busy: 0 Effective Address: -1 Start Cycle: -1 Execute End Cycle: -1 Duration left:
      Ready To Write: false
Store Buffers:
Store buffer position0:
Tag: S1 Busy: 0 Effective Address: -1 Start Cycle: -1 Execute End Cycle: -1 Duration left:
      Ready To Write: false
-1
Store buffer position1:
Tag: S2 Busy: 0 Effective Address: -1 Start Cycle: -1 Execute End Cycle: -1 Duration left:
-1
      Ready To Write: false
Store buffer position2:
Tag: S3 Busy: 0 Effective Address: -1 Start Cycle: -1 Execute End Cycle: -1 Duration left:
-1
      Ready To Write: false
Register File:
R0: Tag: L1
              Busy: 1 Value: 0.0
R1: Tag:
             Busy: 0 Value: 0.0
             Busy: 0 Value: 3.0
R2: Tag:
R3: Tag:
             Busy: 0 Value: 0.0
             Busy: 0 Value: 1.0
R4: Tag:
R5: Tag:
             Busy: 0 Value: 0.0
             Busy: 0 Value: 0.0
R6: Tag:
R7: Tag:
             Busy: 0 Value: 0.0
             Busy: 0 Value: 0.0
R8: Tag:
R9: Tag:
             Busy: 0 Value: 0.0
R10: Tag:
             Busy: 0 Value: 0.0
R11: Tag:
             Busy: 0 Value: 0.0
R12: Tag:
             Busy: 0 Value: 0.0
```

Busy: 0 Value: 0.0

R13: Tag:

R14: Tag: Busy: 0 Value: 0.0
R15: Tag: Busy: 0 Value: 10.0
R16: Tag: Busy: 0 Value: 0.0
R17: Tag: Busy: 0 Value: 0.0
R18: Tag: Busy: 0 Value: 0.0
R19: Tag: Busy: 0 Value: 0.0

Memory: M0: 0.0 M1: 0.0 M2: 2.0 M3: 0.0 M4: 0.0 M5: 0.0

Common Data Bus:

Tag: Value:

M6: 0.0

Current Instruction in PC: ADDI R12 R12 99

Instructions To Write: Stall Branch: false

Stall: false

-----

Instruction to be issued: ADDI R12 R12 99 false

stall is now false: false

Issue cycle of ADDI R12 R12 99 is 2

Clock Cycle: 2 PC Value: 2

Reservation Stations:

Adder:

Adder position0: Tag: A1 Start Cycle: -1 Execute End Cycle: -1 Busy: 1 Instruction Type: ADDI Vj: 0.0 Vk: 99 Qj: Qk: A: Duration left: 1 Ready To Write: false Adder position1: Tag: A2 Start Cycle: -1 Execute End Cycle: -1 Busy: 0 Instruction Duration left: -1 Ready To Write: false Type: None Vj: Vk: Qj: Qk: A: Adder position2: Tag: A3 Start Cycle: -1 Execute End Cycle: -1 Busy: 0 Instruction Type: None Vi: Vk: Qj: Qk: A: Duration left: -1 Ready To Write: false Multiplier:

Multiplier position0:

Tag: M1 Start Cycle: -1 Execute End Cycle: -1 Busy: 0 Instruction Type: None Vj: Vk:

Qj: Qk: A: Duration left: -1 Ready To Write: false

Multiplier position1:

Tag: M2 Start Cycle: -1 Execute End Cycle: -1 Busy: 0 Instruction Type: None Vj: Vk:

Qj: Qk: A: Duration left: -1 Ready To Write: false

Load Buffers:

Load buffer position0:

Tag: L1 Busy: 1 Effective Address: 2 Start Cycle: 2 Execute End Cycle: 3 Duration left: 1

Ready To Write: false Load buffer position1:

Tag: L2 Busy: 0 Effective Address: -1 Start Cycle: -1 Execute End Cycle: -1 Duration left:

-1 Ready To Write: false

Load buffer position2: Tag: L3 Busy: 0 Effective Address: -1 Start Cycle: -1 Execute End Cycle: -1 Duration left: Ready To Write: false -1 Store Buffers: Store buffer position0: Tag: S1 Busy: 0 Effective Address: -1 Start Cycle: -1 Execute End Cycle: -1 Duration left: Ready To Write: false Store buffer position1: Tag: S2 Busy: 0 Effective Address: -1 Start Cycle: -1 Execute End Cycle: -1 Duration left: -1 Ready To Write: false Store buffer position2: Tag: S3 Busy: 0 Effective Address: -1 Start Cycle: -1 Execute End Cycle: -1 Duration left: -1 Ready To Write: false Register File: R0: Tag: L1 Busy: 1 Value: 0.0 R1: Tag: Busy: 0 Value: 0.0 R2: Tag: Busy: 0 Value: 3.0 R3: Tag: Busy: 0 Value: 0.0 Busy: 0 Value: 1.0 R4: Tag: Busy: 0 Value: 0.0 R5: Tag: Busy: 0 Value: 0.0 R6: Tag: R7: Tag: Busy: 0 Value: 0.0 R8: Tag: Busy: 0 Value: 0.0 R9: Tag: Busy: 0 Value: 0.0 R10: Tag: Busy: 0 Value: 0.0 R11: Tag: Busy: 0 Value: 0.0 R12: Tag: A1 Busy: 1 Value: 0.0 Busy: 0 Value: 0.0 R13: Tag: R14: Tag: Busy: 0 Value: 0.0 Busy: 0 Value: 10.0 R15: Tag: Busy: 0 Value: 0.0 R16: Tag: Busy: 0 Value: 0.0 R17: Tag: R18: Tag: Busy: 0 Value: 0.0 R19: Tag: Busy: 0 Value: 0.0 Memory: M0: 0.0 M1: 0.0 M2: 2.0 M3: 0.0 M4: 0.0 M5: 0.0 M6: 0.0

Common Data Bus:

Tag: Value:

Current Instruction in PC: SD R12 1

Instructions To Write: Stall Branch: false

Stall: false

\_\_\_\_\_

Instruction to be issued: SD R12 1 false

stall is now false: false Issue cycle of SD R12 1 is 3 Made load read to write

Clock Cycle: 3 PC Value: 3

Reservation Stations:

Adder:

Adder position0: Tag: A1 Start Cycle: 3 Execute End Cycle: 4 Busy: 1 Instruction Type: ADDI Vi: 0.0 Vk: 99 Qi: Qk: Duration left: 1 Ready To Write: false A: Start Cycle: -1 Execute End Cycle: -1 Busy: 0 Instruction Adder position1: Tag: A2 Type: None Vj: Duration left: -1 Ready To Write: false Vk: Qj: Qk: A: Adder position2: Tag: A3 Start Cycle: -1 Execute End Cycle: -1 Busy: 0 Instruction Duration left: -1 Ready To Write: false Type: None Vj: Vk: Qk: A: Qj: Multiplier:

Multiplier position0:

Tag: M1 Start Cycle: -1 Execute End Cycle: -1 Busy: 0 Instruction Type: None Vj: Vk:

Qj: Qk: A: Duration left: -1 Ready To Write: false

Multiplier position1:

Tag: M2 Start Cycle: -1 Execute End Cycle: -1 Busy: 0 Instruction Type: None Vj: Vk:

Qj: Qk: A: Duration left: -1 Ready To Write: false

Load Buffers:

Load buffer position0:

Tag: L1 Busy: 1 Effective Address: 2 Start Cycle: 2 Execute End Cycle: 3 Duration left: 1

Ready To Write: true Load buffer position1:

Tag: L2 Busy: 0 Effective Address: -1 Start Cycle: -1 Execute End Cycle: -1 Duration left:

-1 Ready To Write: false

Load buffer position2:

Tag: L3 Busy: 0 Effective Address: -1 Start Cycle: -1 Execute End Cycle: -1 Duration left:

-1 Ready To Write: false

Store Buffers:

Store buffer position0:

Tag: S1 Busy: 1 Effective Address: 1 Start Cycle: -1 Execute End Cycle: -1 Duration left:

1 Ready To Write: false

Store buffer position1:

Tag: S2 Busy: 0 Effective Address: -1 Start Cycle: -1 Execute End Cycle: -1 Duration left:

-1 Ready To Write: false

Store buffer position2:

Tag: S3 Busy: 0 Effective Address: -1 Start Cycle: -1 Execute End Cycle: -1 Duration left:

-1 Ready To Write: false

Register File:

R0: Tag: L1 Busy: 1 Value: 0.0 R1: Tag: Busy: 0 Value: 0.0 R2: Tag: Busy: 0 Value: 3.0 R3: Tag: Busy: 0 Value: 0.0 R4: Tag: Busy: 0 Value: 1.0

```
R5: Tag:
             Busy: 0 Value: 0.0
R6: Tag:
             Busy: 0 Value: 0.0
R7: Tag:
             Busy: 0 Value: 0.0
             Busy: 0 Value: 0.0
R8: Tag:
             Busy: 0 Value: 0.0
R9: Tag:
             Busy: 0 Value: 0.0
R10: Tag:
R11: Tag:
             Busy: 0 Value: 0.0
R12: Tag: A1
               Busy: 1 Value: 0.0
R13: Tag:
             Busy: 0 Value: 0.0
R14: Tag:
             Busy: 0 Value: 0.0
R15: Tag:
             Busy: 0 Value: 10.0
R16: Tag:
             Busy: 0 Value: 0.0
R17: Tag:
             Busy: 0 Value: 0.0
R18: Tag:
             Busy: 0 Value: 0.0
             Busy: 0 Value: 0.0
R19: Tag:
Memory:
M0: 0.0
M1: 0.0
M2: 2.0
M3: 0.0
M4: 0.0
M5: 0.0
M6: 0.0
Common Data Bus:
Tag: Value:
Instructions To Write:
```

Current Instruction in PC: SUBI R15 R15 5

LD F0 2

Stall Branch: false

Stall: false

Instruction to be issued: SUBI R15 R15 5 false

stall is now false: false

Issue cycle of SUBI R15 R15 5 is 4

Value of memory is: 2.0 and effective address is: 2

Instruction to be written: LD F0 2

Clock Cycle: 4 PC Value: 4

Reservation Stations:

Adder:

Adder position0: Tag: A1 Start Cycle: 3 Execute End Cycle: 4 Busy: 1 Instruction Type: ADDI Vj: 0.0 Vk: 99 Qj: Qk: A: Duration left: 1 Ready To Write: true Adder position1: Tag: A2 Start Cycle: -1 Execute End Cycle: -1 Busy: 1 Instruction Vk: 5 Qj: Type: SUBI Vj: 10.0 Qk: A: Duration left: 1 Ready To Write: false Adder position2: Tag: A3 Start Cycle: -1 Execute End Cycle: -1 Busy: 0 Instruction Type: None Vj: Vk: Duration left: -1 Ready To Write: false Qj: Qk: A: Multiplier:

Multiplier position0:

```
Tag: M1 Start Cycle: -1 Execute End Cycle: -1 Busy: 0 Instruction Type: None Vi:
                                                                                    Vk:
Qj:
     Qk:
           A:
                  Duration left: -1
                                      Ready To Write: false
Multiplier position1:
Tag: M2 Start Cycle: -1 Execute End Cycle: -1 Busy: 0 Instruction Type: None Vj:
                                                                                    Vk:
Qj:
           A:
                  Duration left: -1
                                      Ready To Write: false
     Qk:
Load Buffers:
Load buffer position0:
Tag: L1 Busy: 0 Effective Address: -1 Start Cycle: -1 Execute End Cycle: -1 Duration left:
      Ready To Write: false
Load buffer position1:
Tag: L2 Busy: 0 Effective Address: -1 Start Cycle: -1 Execute End Cycle: -1 Duration left:
      Ready To Write: false
Load buffer position2:
Tag: L3 Busy: 0 Effective Address: -1 Start Cycle: -1 Execute End Cycle: -1 Duration left:
      Ready To Write: false
Store Buffers:
Store buffer position0:
                                      Start Cycle: -1 Execute End Cycle: -1 Duration left:
Tag: S1 Busy: 1 Effective Address: 1
      Ready To Write: false
1
Store buffer position1:
Tag: S2 Busy: 0 Effective Address: -1 Start Cycle: -1 Execute End Cycle: -1 Duration left:
-1
      Ready To Write: false
Store buffer position2:
Tag: S3 Busy: 0 Effective Address: -1 Start Cycle: -1 Execute End Cycle: -1 Duration left:
-1
      Ready To Write: false
Register File:
R0: Tag:
             Busy: 0 Value: 2.0
R1: Tag:
             Busy: 0 Value: 0.0
R2: Tag:
             Busy: 0 Value: 3.0
             Busy: 0 Value: 0.0
R3: Tag:
R4: Tag:
             Busy: 0 Value: 1.0
R5: Tag:
             Busy: 0 Value: 0.0
R6: Tag:
             Busy: 0 Value: 0.0
R7: Tag:
             Busy: 0 Value: 0.0
R8: Tag:
             Busy: 0 Value: 0.0
R9: Tag:
             Busy: 0 Value: 0.0
             Busy: 0 Value: 0.0
R10: Tag:
R11: Tag:
             Busy: 0 Value: 0.0
R12: Tag: A1
               Busy: 1 Value: 0.0
R13: Tag:
             Busy: 0 Value: 0.0
R14: Tag:
             Busy: 0 Value: 0.0
R15: Tag: A2 Busy: 1 Value: 10.0
R16: Tag:
             Busy: 0 Value: 0.0
R17: Tag:
             Busy: 0 Value: 0.0
R18: Tag:
             Busy: 0 Value: 0.0
R19: Tag:
             Busy: 0 Value: 0.0
Memory:
```

M0: 0.0

```
M1: 0.0
M2: 2.0
M3: 0.0
M4: 0.0
M5: 0.0
M6: 0.0
Common Data Bus:
Tag: L1 Value: 2.0
Current Instruction in PC: BNEZ R15 LOOP
Instructions To Write:
ADDI R12 R12 99
Stall Branch: false
Stall: false
Instruction to be issued: BNEZ R15 LOOP false
stall is now false: false
-----Stall due to Branch-----
Issue cycle of BNEZ R15 LOOP is 5
Instruction to be written: ADDI R12 R12 99
Clock Cycle: 5
PC Value: 5
Reservation Stations:
Adder:
Adder position0: Tag: A1
                            Start Cycle: -1 Execute End Cycle: -1 Busy: 0 Instruction
Type: None Vj: Vk:
                             Qk: A:
                                          Duration left: -1 Ready To Write: false
                        Qj:
Adder position1: Tag: A2
                            Start Cycle: 5 Execute End Cycle: 6 Busy: 1 Instruction
Type: SUBI Vi: 10.0
                                     Qk: A: Duration left: 1 Ready To Write: false
                        Vk: 5 Qi:
                            Start Cycle: -1 Execute End Cycle: -1 Busy: 1 Instruction
Adder position2: Tag: A3
Type: BNEZ Vj: Vk: Qj: A2 Qk: A:
                                            Duration left: 1 Ready To Write: false
Multiplier:
Multiplier position0:
Tag: M1 Start Cycle: -1 Execute End Cycle: -1 Busy: 0 Instruction Type: None Vj:
                                                                                  Vk:
Qi:
     Qk:
           A:
                 Duration left: -1
                                     Ready To Write: false
Multiplier position1:
Tag: M2 Start Cycle: -1 Execute End Cycle: -1 Busy: 0 Instruction Type: None Vj:
                                                                                   Vk:
                                     Ready To Write: false
Qj:
     Qk: A:
                 Duration left: -1
Load Buffers:
Load buffer position0:
Tag: L1 Busy: 0 Effective Address: -1 Start Cycle: -1 Execute End Cycle: -1 Duration left:
      Ready To Write: false
Load buffer position1:
Tag: L2 Busy: 0 Effective Address: -1 Start Cycle: -1 Execute End Cycle: -1 Duration left:
      Ready To Write: false
Load buffer position2:
Tag: L3 Busy: 0 Effective Address: -1 Start Cycle: -1 Execute End Cycle: -1 Duration left:
```

Ready To Write: false

-1

Store Buffers:

Store buffer position0:

```
Tag: S1 Busy: 1 Effective Address: 1
                                      Start Cycle: -1 Execute End Cycle: -1 Duration left:
      Ready To Write: false
1
Store buffer position1:
Tag: S2 Busy: 0 Effective Address: -1 Start Cycle: -1 Execute End Cycle: -1 Duration left:
-1
      Ready To Write: false
Store buffer position2:
Tag: S3 Busy: 0 Effective Address: -1 Start Cycle: -1 Execute End Cycle: -1 Duration left:
-1
      Ready To Write: false
Register File:
R0: Tag:
             Busy: 0 Value: 2.0
             Busy: 0 Value: 0.0
R1: Tag:
             Busy: 0 Value: 3.0
R2: Tag:
R3: Tag:
             Busy: 0 Value: 0.0
R4: Tag:
             Busy: 0 Value: 1.0
             Busy: 0 Value: 0.0
R5: Tag:
             Busy: 0 Value: 0.0
R6: Tag:
R7: Tag:
             Busy: 0 Value: 0.0
R8: Tag:
             Busy: 0 Value: 0.0
             Busy: 0 Value: 0.0
R9: Tag:
R10: Tag:
             Busy: 0 Value: 0.0
             Busy: 0 Value: 0.0
R11: Tag:
             Busy: 0 Value: 99.0
R12: Tag:
R13: Tag:
             Busy: 0 Value: 0.0
R14: Tag:
             Busy: 0 Value: 0.0
R15: Tag: A2 Busy: 1 Value: 10.0
R16: Tag:
             Busy: 0 Value: 0.0
R17: Tag:
             Busy: 0 Value: 0.0
             Busy: 0 Value: 0.0
R18: Tag:
R19: Tag:
             Busy: 0 Value: 0.0
Memory:
M0: 0.0
M1: 0.0
M2: 2.0
M3: 0.0
M4: 0.0
M5: 0.0
M6: 0.0
Common Data Bus:
Tag: A1 Value: 99.0
Current Instruction in PC: ADDI R13 R13 99
Instructions To Write:
Stall Branch: true
Stall: false
```

PC Value: 5
Reservation Stations:

Clock Cycle: 6

Instruction to be issued: ADDI R13 R13 99 false

Adder:

Adder position0: Tag: A1 Start Cycle: -1 Execute End Cycle: -1 Busy: 0 Instruction Duration left: -1 Ready To Write: false Type: None Vj: Vk: Qj: Qk: A: Adder position1: Tag: A2 Start Cycle: 5 Execute End Cycle: 6 Busy: 1 Instruction Type: SUBI Vj: 10.0 A: Duration left: 1 Ready To Write: true Vk: 5 Qj: Qk: Adder position2: Tag: A3 Start Cycle: -1 Execute End Cycle: -1 Busy: 1 Instruction Duration left: 1 Ready To Write: false Type: BNEZ Vj: Vk: Qj: A2 Qk: A: Multiplier:

Multiplier position0:

Tag: M1 Start Cycle: -1 Execute End Cycle: -1 Busy: 0 Instruction Type: None Vj: Vk:

Qj: Qk: A: Duration left: -1 Ready To Write: false

Multiplier position1:

Tag: M2 Start Cycle: -1 Execute End Cycle: -1 Busy: 0 Instruction Type: None Vj: Vk:

Qj: Qk: A: Duration left: -1 Ready To Write: false

Load Buffers:

Load buffer position0:

Tag: L1 Busy: 0 Effective Address: -1 Start Cycle: -1 Execute End Cycle: -1 Duration left:

-1 Ready To Write: false

Load buffer position1:

Tag: L2 Busy: 0 Effective Address: -1 Start Cycle: -1 Execute End Cycle: -1 Duration left:

-1 Ready To Write: false

Load buffer position2:

Tag: L3 Busy: 0 Effective Address: -1 Start Cycle: -1 Execute End Cycle: -1 Duration left:

-1 Ready To Write: false

Store Buffers:

Store buffer position0:

Tag: S1 Busy: 1 Effective Address: 1 Start Cycle: 6 Execute End Cycle: 7 Duration left: 1

Ready To Write: false Store buffer position1:

Tag: S2 Busy: 0 Effective Address: -1 Start Cycle: -1 Execute End Cycle: -1 Duration left:

-1 Ready To Write: false

Store buffer position2:

Tag: S3 Busy: 0 Effective Address: -1 Start Cycle: -1 Execute End Cycle: -1 Duration left:

-1 Ready To Write: false

Register File:

R0: Tag: Busy: 0 Value: 2.0

R1: Tag: Busy: 0 Value: 0.0

R2: Tag: Busy: 0 Value: 3.0

R3: Tag: Busy: 0 Value: 0.0

R4: Tag: Busy: 0 Value: 1.0

R5: Tag: Busy: 0 Value: 0.0

R6: Tag: Busy: 0 Value: 0.0

R7: Tag: Busy: 0 Value: 0.0

R8: Tag: Busy: 0 Value: 0.0

R9: Tag: Busy: 0 Value: 0.0

R10: Tag: Busy: 0 Value: 0.0

R11: Tag: Busy: 0 Value: 0.0

R12: Tag: Busy: 0 Value: 99.0

```
R13: Tag:
             Busy: 0 Value: 0.0
R14: Tag:
             Busy: 0 Value: 0.0
R15: Tag: A2 Busy: 1 Value: 10.0
             Busy: 0 Value: 0.0
R16: Tag:
             Busy: 0 Value: 0.0
R17: Tag:
             Busy: 0 Value: 0.0
R18: Tag:
R19: Tag:
             Busy: 0 Value: 0.0
Memory:
M0: 0.0
M1: 0.0
M2: 2.0
M3: 0.0
M4: 0.0
M5: 0.0
M6: 0.0
Common Data Bus:
Tag: A1 Value: 99.0
Current Instruction in PC: ADDI R13 R13 99
Instructions To Write:
SUBI R15 R15 5
Stall Branch: true
Stall: false
Instruction to be issued: ADDI R13 R13 99 false
sTORE FINISHED-----
Instruction to be written: SUBI R15 R15 5
Clock Cycle: 7
PC Value: 5
Reservation Stations:
Adder:
Adder position0: Tag: A1
                            Start Cycle: -1 Execute End Cycle: -1 Busy: 0 Instruction
                                          Duration left: -1 Ready To Write: false
Type: None Vj:
                Vk:
                        Qj:
                              Qk: A:
Adder position1: Tag: A2
                            Start Cycle: -1 Execute End Cycle: -1 Busy: 0 Instruction
Type: None Vi:
                Vk:
                        Qj:
                              Qk:
                                    A:
                                          Duration left: -1 Ready To Write: false
Adder position2: Tag: A3
                            Start Cycle: -1 Execute End Cycle: -1 Busy: 1 Instruction
Type: BNEZ Vj: 5.0 Vk:
                          Qi: Qk: A:
                                            Duration left: 1 Ready To Write: false
Multiplier:
Multiplier position0:
Tag: M1 Start Cycle: -1 Execute End Cycle: -1 Busy: 0 Instruction Type: None Vi:
                                                                                   Vk:
Qi:
     Qk:
           A:
                 Duration left: -1
                                     Ready To Write: false
Multiplier position1:
Tag: M2 Start Cycle: -1 Execute End Cycle: -1 Busy: 0 Instruction Type: None Vj:
                                                                                   Vk:
           A:
                 Duration left: -1
                                     Ready To Write: false
Qj:
     Qk:
Load Buffers:
Load buffer position0:
Tag: L1 Busy: 0 Effective Address: -1 Start Cycle: -1 Execute End Cycle: -1 Duration left:
```

-1

Ready To Write: false

Load buffer position1:

```
Tag: L2 Busy: 0 Effective Address: -1 Start Cycle: -1 Execute End Cycle: -1 Duration left:
-1
      Ready To Write: false
Load buffer position2:
Tag: L3 Busy: 0 Effective Address: -1 Start Cycle: -1 Execute End Cycle: -1 Duration left:
-1
      Ready To Write: false
Store Buffers:
Store buffer position0:
Tag: S1 Busy: 0 Effective Address: -1 Start Cycle: -1 Execute End Cycle: -1 Duration left:
      Ready To Write: false
Store buffer position1:
Tag: S2 Busy: 0 Effective Address: -1 Start Cycle: -1 Execute End Cycle: -1 Duration left:
      Ready To Write: false
Store buffer position2:
Tag: S3 Busy: 0 Effective Address: -1 Start Cycle: -1 Execute End Cycle: -1 Duration left:
      Ready To Write: false
-1
Register File:
R0: Tag:
             Busy: 0 Value: 2.0
R1: Tag:
             Busy: 0 Value: 0.0
R2: Tag:
             Busy: 0 Value: 3.0
R3: Tag:
             Busy: 0 Value: 0.0
             Busy: 0 Value: 1.0
R4: Tag:
R5: Tag:
             Busy: 0 Value: 0.0
R6: Tag:
             Busy: 0 Value: 0.0
R7: Tag:
             Busy: 0 Value: 0.0
R8: Tag:
             Busy: 0 Value: 0.0
             Busy: 0 Value: 0.0
R9: Tag:
             Busy: 0 Value: 0.0
R10: Tag:
R11: Tag:
             Busy: 0 Value: 0.0
R12: Tag:
             Busy: 0 Value: 99.0
             Busy: 0 Value: 0.0
R13: Tag:
R14: Tag:
             Busy: 0 Value: 0.0
R15: Tag:
             Busy: 0 Value: 5.0
R16: Tag:
             Busy: 0 Value: 0.0
R17: Tag:
             Busy: 0 Value: 0.0
R18: Tag:
             Busy: 0 Value: 0.0
R19: Tag:
             Busy: 0 Value: 0.0
Memory:
M0: 0.0
M1: 99.0
M2: 2.0
M3: 0.0
M4: 0.0
M5: 0.0
M6: 0.0
```

Common Data Bus: Tag: A2 Value: 5.0

Current Instruction in PC: ADDI R13 R13 99

Instructions To Write:

Stall Branch: true

Stall: false

\_\_\_\_\_

Instruction to be issued: ADDI R13 R13 99 false

Clock Cycle: 8 PC Value: 5

Reservation Stations:

Adder:

Adder position0: Tag: A1 Start Cycle: -1 Execute End Cycle: -1 Busy: 0 Instruction Type: None Vj: Vk: Qk: A: Duration left: -1 Ready To Write: false Qj: Adder position1: Tag: A2 Start Cycle: -1 Execute End Cycle: -1 Busy: 0 Instruction Duration left: -1 Ready To Write: false Type: None Vj: Vk: Qj: Qk: A: Adder position2: Tag: A3 Start Cycle: 8 Execute End Cycle: 9 Busy: 1 Instruction Type: BNEZ Vj: 5.0 Vk: Qj: Qk: A: Duration left: 1 Ready To Write: false Multiplier:

Multiplier position0:

Tag: M1 Start Cycle: -1 Execute End Cycle: -1 Busy: 0 Instruction Type: None Vj: Vk:

Qj: Qk: A: Duration left: -1 Ready To Write: false

Multiplier position1:

Tag: M2 Start Cycle: -1 Execute End Cycle: -1 Busy: 0 Instruction Type: None Vj: Vk:

Qj: Qk: A: Duration left: -1 Ready To Write: false

Load Buffers:

Load buffer position0:

Tag: L1 Busy: 0 Effective Address: -1 Start Cycle: -1 Execute End Cycle: -1 Duration left:

-1 Ready To Write: false

Load buffer position1:

Tag: L2 Busy: 0 Effective Address: -1 Start Cycle: -1 Execute End Cycle: -1 Duration left:

-1 Ready To Write: false

Load buffer position2:

Tag: L3 Busy: 0 Effective Address: -1 Start Cycle: -1 Execute End Cycle: -1 Duration left:

-1 Ready To Write: false

Store Buffers:

Store buffer position0:

Tag: S1 Busy: 0 Effective Address: -1 Start Cycle: -1 Execute End Cycle: -1 Duration left:

-1 Ready To Write: false

Store buffer position1:

Tag: S2 Busy: 0 Effective Address: -1 Start Cycle: -1 Execute End Cycle: -1 Duration left:

-1 Ready To Write: false

Store buffer position2:

Tag: S3 Busy: 0 Effective Address: -1 Start Cycle: -1 Execute End Cycle: -1 Duration left:

-1 Ready To Write: false

Register File:

R0: Tag: Busy: 0 Value: 2.0 R1: Tag: Busy: 0 Value: 0.0 R2: Tag: Busy: 0 Value: 3.0 R3: Tag: Busy: 0 Value: 0.0 R4: Tag: Busy: 0 Value: 1.0 R5: Tag: Busy: 0 Value: 0.0

```
R6: Tag:
             Busy: 0 Value: 0.0
R7: Tag:
             Busy: 0 Value: 0.0
             Busy: 0 Value: 0.0
R8: Tag:
             Busy: 0 Value: 0.0
R9: Tag:
             Busy: 0 Value: 0.0
R10: Tag:
R11: Tag:
             Busy: 0 Value: 0.0
R12: Tag:
             Busy: 0 Value: 99.0
R13: Tag:
             Busy: 0 Value: 0.0
R14: Tag:
             Busy: 0 Value: 0.0
R15: Tag:
             Busy: 0 Value: 5.0
R16: Tag:
             Busy: 0 Value: 0.0
             Busy: 0 Value: 0.0
R17: Tag:
R18: Tag:
             Busy: 0 Value: 0.0
R19: Tag:
             Busy: 0 Value: 0.0
Memory:
M0: 0.0
M1: 99.0
M2: 2.0
M3: 0.0
M4: 0.0
M5: 0.0
M6: 0.0
Common Data Bus:
Tag: A2 Value: 5.0
Current Instruction in PC: ADDI R13 R13 99
Instructions To Write:
Stall Branch: true
Stall: false
Instruction to be issued: ADDI R13 R13 99 false
Clock Cycle: 9
PC Value: 5
Reservation Stations:
Adder:
Adder position0: Tag: A1
                            Start Cycle: -1 Execute End Cycle: -1 Busy: 0 Instruction
                                          Duration left: -1 Ready To Write: false
Type: None Vi:
                              Qk:
                                    A:
                 Vk:
                        Qj:
Adder position1: Tag: A2
                             Start Cycle: -1 Execute End Cycle: -1 Busy: 0 Instruction
                                          Duration left: -1 Ready To Write: false
Type: None Vj:
                Vk:
                        Qj:
                              Qk:
                                    A:
Adder position2: Tag: A3
                             Start Cycle: 8 Execute End Cycle: 9 Busy: 1 Instruction
Type: BNEZ Vj: 5.0 Vk:
                                Qk: A:
                                            Duration left: 1 Ready To Write: true
                          Qj:
Multiplier:
Multiplier position0:
Tag: M1 Start Cycle: -1 Execute End Cycle: -1 Busy: 0 Instruction Type: None Vj:
                                                                                   Vk:
                                     Ready To Write: false
           A:
                 Duration left: -1
Multiplier position1:
Tag: M2 Start Cycle: -1 Execute End Cycle: -1 Busy: 0 Instruction Type: None Vj:
                                                                                   Vk:
                                     Ready To Write: false
Qj:
     Qk:
           A:
                  Duration left: -1
Load Buffers:
```

```
Load buffer position0:
Tag: L1 Busy: 0 Effective Address: -1 Start Cycle: -1 Execute End Cycle: -1 Duration left:
      Ready To Write: false
Load buffer position1:
Tag: L2 Busy: 0 Effective Address: -1 Start Cycle: -1 Execute End Cycle: -1 Duration left:
      Ready To Write: false
Load buffer position2:
Tag: L3 Busy: 0 Effective Address: -1 Start Cycle: -1 Execute End Cycle: -1 Duration left:
      Ready To Write: false
Store Buffers:
Store buffer position0:
Tag: S1 Busy: 0 Effective Address: -1 Start Cycle: -1 Execute End Cycle: -1 Duration left:
-1
      Ready To Write: false
Store buffer position1:
Tag: S2 Busy: 0 Effective Address: -1 Start Cycle: -1 Execute End Cycle: -1 Duration left:
      Ready To Write: false
-1
Store buffer position2:
Tag: S3 Busy: 0 Effective Address: -1 Start Cycle: -1 Execute End Cycle: -1 Duration left:
-1
      Ready To Write: false
Register File:
             Busy: 0 Value: 2.0
R0: Tag:
R1: Tag:
             Busy: 0 Value: 0.0
R2: Tag:
             Busy: 0 Value: 3.0
R3: Tag:
             Busy: 0 Value: 0.0
R4: Tag:
             Busy: 0 Value: 1.0
R5: Tag:
             Busy: 0 Value: 0.0
             Busy: 0 Value: 0.0
R6: Tag:
R7: Tag:
             Busy: 0 Value: 0.0
R8: Tag:
             Busy: 0 Value: 0.0
             Busy: 0 Value: 0.0
R9: Tag:
R10: Tag:
             Busy: 0 Value: 0.0
R11: Tag:
             Busy: 0 Value: 0.0
R12: Tag:
             Busy: 0 Value: 99.0
R13: Tag:
             Busy: 0 Value: 0.0
R14: Tag:
             Busy: 0 Value: 0.0
R15: Tag:
             Busy: 0 Value: 5.0
             Busy: 0 Value: 0.0
R16: Tag:
R17: Tag:
             Busy: 0 Value: 0.0
             Busy: 0 Value: 0.0
R18: Tag:
R19: Tag:
             Busy: 0 Value: 0.0
Memory:
M0: 0.0
M1: 99.0
```

M2: 2.0 M3: 0.0 M4: 0.0 M5: 0.0 M6: 0.0 Common Data Bus: Tag: A2 Value: 5.0

Current Instruction in PC: ADDI R13 R13 99

Instructions To Write: BNEZ R15 LOOP Stall Branch: true

Stall: false

-----

Instruction to be issued: ADDI R13 R13 99 false Instruction to be written: BNEZ R15 LOOP

Clock Cycle: 10 PC Value: 0

Reservation Stations:

Adder:

Start Cycle: -1 Execute End Cycle: -1 Busy: 0 Instruction Adder position0: Tag: A1 Type: None Vi: Vk: Qi: Duration left: -1 Ready To Write: false Qk: A: Adder position1: Tag: A2 Start Cycle: -1 Execute End Cycle: -1 Busy: 0 Instruction Duration left: -1 Ready To Write: false Type: None Vj: Vk: Qj: Qk: A: Adder position2: Tag: A3 Start Cycle: -1 Execute End Cycle: -1 Busy: 0 Instruction Type: None Vj: Qk: A: Duration left: -1 Ready To Write: false Vk: Qj: Multiplier:

Multiplier position0:

Tag: M1 Start Cycle: -1 Execute End Cycle: -1 Busy: 0 Instruction Type: None Vj: Vk:

Qj: Qk: A: Duration left: -1 Ready To Write: false

Multiplier position1:

Tag: M2 Start Cycle: -1 Execute End Cycle: -1 Busy: 0 Instruction Type: None Vj: Vk:

Qj: Qk: A: Duration left: -1 Ready To Write: false

Load Buffers:

Load buffer position0:

Tag: L1 Busy: 0 Effective Address: -1 Start Cycle: -1 Execute End Cycle: -1 Duration left:

-1 Ready To Write: false

Load buffer position1:

Tag: L2 Busy: 0 Effective Address: -1 Start Cycle: -1 Execute End Cycle: -1 Duration left:

-1 Ready To Write: false

Load buffer position2:

Tag: L3 Busy: 0 Effective Address: -1 Start Cycle: -1 Execute End Cycle: -1 Duration left:

-1 Ready To Write: false

Store Buffers:

Store buffer position0:

Tag: S1 Busy: 0 Effective Address: -1 Start Cycle: -1 Execute End Cycle: -1 Duration left:

-1 Ready To Write: false

Store buffer position1:

Tag: S2 Busy: 0 Effective Address: -1 Start Cycle: -1 Execute End Cycle: -1 Duration left:

-1 Ready To Write: false

Store buffer position2:

Tag: S3 Busy: 0 Effective Address: -1 Start Cycle: -1 Execute End Cycle: -1 Duration left:

-1 Ready To Write: false

Register File:

```
R0: Tag:
             Busy: 0 Value: 2.0
R1: Tag:
             Busy: 0 Value: 0.0
             Busy: 0 Value: 3.0
R2: Tag:
R3: Tag:
             Busy: 0 Value: 0.0
             Busy: 0 Value: 1.0
R4: Tag:
R5: Tag:
             Busy: 0 Value: 0.0
R6: Tag:
             Busy: 0 Value: 0.0
R7: Tag:
             Busy: 0 Value: 0.0
             Busy: 0 Value: 0.0
R8: Tag:
             Busy: 0 Value: 0.0
R9: Tag:
             Busy: 0 Value: 0.0
R10: Tag:
             Busy: 0 Value: 0.0
R11: Tag:
R12: Tag:
             Busy: 0 Value: 99.0
R13: Tag:
             Busy: 0 Value: 0.0
             Busy: 0 Value: 0.0
R14: Tag:
             Busy: 0 Value: 5.0
R15: Tag:
R16: Tag:
             Busy: 0 Value: 0.0
R17: Tag:
             Busy: 0 Value: 0.0
             Busy: 0 Value: 0.0
R18: Tag:
             Busy: 0 Value: 0.0
R19: Tag:
Memory:
M0: 0.0
M2: 2.0
M3: 0.0
```

M1: 99.0

M4: 0.0 M5: 0.0

M6: 0.0

Common Data Bus:

Tag: A3 Value: PC value is: 0 Current Instruction in PC: LD F0 2

Instructions To Write: Stall Branch: false

Stall: false

Instruction to be issued: LD F0 2 false

stall is now false : false Issue cycle of LD F0 2 is 11

Clock Cycle: 11 PC Value: 1

Reservation Stations:

Adder:

Adder position0: Tag: A1 Start Cycle: -1 Execute End Cycle: -1 Busy: 0 Instruction Type: None Vj: Duration left: -1 Ready To Write: false Vk: Qj: Qk: A: Adder position1: Tag: A2 Start Cycle: -1 Execute End Cycle: -1 Busy: 0 Instruction Type: None Vj: Duration left: -1 Ready To Write: false Vk: Qj: Qk: A:

Adder position2: Tag: A3 Start Cycle: -1 Execute End Cycle: -1 Busy: 0 Instruction Type: None Vj: Vk: Qj: Qk: A: Duration left: -1 Ready To Write: false Multiplier:

Multiplier position0:

Tag: M1 Start Cycle: -1 Execute End Cycle: -1 Busy: 0 Instruction Type: None Vj: Vk:

Qj: Qk: A: Duration left: -1 Ready To Write: false

Multiplier position1:

Tag: M2 Start Cycle: -1 Execute End Cycle: -1 Busy: 0 Instruction Type: None Vj: Vk:

Qj: Qk: A: Duration left: -1 Ready To Write: false

Load Buffers:

Load buffer position0:

Tag: L1 Busy: 1 Effective Address: 2 Start Cycle: -1 Execute End Cycle: -1 Duration left: 1

Ready To Write: false Load buffer position1:

Tag: L2 Busy: 0 Effective Address: -1 Start Cycle: -1 Execute End Cycle: -1 Duration left:

-1 Ready To Write: false

Load buffer position2:

Tag: L3 Busy: 0 Effective Address: -1 Start Cycle: -1 Execute End Cycle: -1 Duration left:

-1 Ready To Write: false

Store Buffers:

Store buffer position0:

Tag: S1 Busy: 0 Effective Address: -1 Start Cycle: -1 Execute End Cycle: -1 Duration left:

-1 Ready To Write: false

Store buffer position1:

Tag: S2 Busy: 0 Effective Address: -1 Start Cycle: -1 Execute End Cycle: -1 Duration left:

-1 Ready To Write: false

Store buffer position2:

Tag: S3 Busy: 0 Effective Address: -1 Start Cycle: -1 Execute End Cycle: -1 Duration left:

-1 Ready To Write: false

Register File:

R0: Tag: L1 Busy: 1 Value: 2.0 Busy: 0 Value: 0.0 R1: Tag: R2: Tag: Busy: 0 Value: 3.0 R3: Tag: Busy: 0 Value: 0.0 R4: Tag: Busy: 0 Value: 1.0 Busy: 0 Value: 0.0 R5: Tag: Busy: 0 Value: 0.0 R6: Tag: R7: Tag: Busy: 0 Value: 0.0 Busy: 0 Value: 0.0 R8: Tag: R9: Tag: Busy: 0 Value: 0.0

R10: Tag: Busy: 0 Value: 0.0 R11: Tag: Busy: 0 Value: 0.0

R11: Tag: Busy: 0 Value: 0.0 R12: Tag: Busy: 0 Value: 99.0

R12: Tag: Busy: 0 Value: 99.0

R14: Tag: Busy: 0 Value: 0.0

R15: Tag: Busy: 0 Value: 5.0

R16: Tag: Busy: 0 Value: 0.0 R17: Tag: Busy: 0 Value: 0.0

R18: Tag: Busy: 0 Value: 0.0 R19: Tag: Busy: 0 Value: 0.0

Memory: M0: 0.0 M1: 99.0 M2: 2.0 M3: 0.0 M4: 0.0 M5: 0.0 M6: 0.0

Common Data Bus:

Tag: A3 Value: PC value is: 0

Current Instruction in PC: ADDI R12 R12 99

Instructions To Write: Stall Branch: false

Stall: false

\_\_\_\_\_

Instruction to be issued: ADDI R12 R12 99 false

stall is now false : false

Issue cycle of ADDI R12 R12 99 is 12

Clock Cycle: 12 PC Value: 2

**Reservation Stations:** 

Adder:

Adder position0: Tag: A1 Start Cycle: -1 Execute End Cycle: -1 Busy: 1 Instruction Type: ADDI Vj: 99.0 Vk: 99 Qj: Qk: A: Duration left: 1 Ready To Write: false Adder position1: Tag: A2 Start Cycle: -1 Execute End Cycle: -1 Busy: 0 Instruction Duration left: -1 Ready To Write: false Type: None Vj: Vk: Qj: Qk: A: Adder position2: Tag: A3 Start Cycle: -1 Execute End Cycle: -1 Busy: 0 Instruction Type: None Vj: Duration left: -1 Ready To Write: false Vk: Qj: Qk: A: Multiplier:

Multiplier position0:

Tag: M1 Start Cycle: -1 Execute End Cycle: -1 Busy: 0 Instruction Type: None Vj: Vk:

Qj: Qk: A: Duration left: -1 Ready To Write: false

Multiplier position1:

Tag: M2 Start Cycle: -1 Execute End Cycle: -1 Busy: 0 Instruction Type: None Vj: Vk:

Qj: Qk: A: Duration left: -1 Ready To Write: false

Load Buffers:

Load buffer position0:

Tag: L1 Busy: 1 Effective Address: 2 Start Cycle: 12 Execute End Cycle: 13 Duration left:

1 Ready To Write: false

Load buffer position1:

Tag: L2 Busy: 0 Effective Address: -1 Start Cycle: -1 Execute End Cycle: -1 Duration left:

-1 Ready To Write: false

Load buffer position2:

Tag: L3 Busy: 0 Effective Address: -1 Start Cycle: -1 Execute End Cycle: -1 Duration left:

-1 Ready To Write: false

Store Buffers:

Store buffer position0:

Tag: S1 Busy: 0 Effective Address: -1 Start Cycle: -1 Execute End Cycle: -1 Duration left:

Ready To Write: false

Store buffer position1:

Tag: S2 Busy: 0 Effective Address: -1 Start Cycle: -1 Execute End Cycle: -1 Duration left:

Ready To Write: false

Store buffer position2:

Tag: S3 Busy: 0 Effective Address: -1 Start Cycle: -1 Execute End Cycle: -1 Duration left:

Ready To Write: false

Register File:

R0: Tag: L1 Busy: 1 Value: 2.0 Busy: 0 Value: 0.0 R1: Tag: R2: Tag: Busy: 0 Value: 3.0 R3: Tag: Busy: 0 Value: 0.0 Busy: 0 Value: 1.0 R4: Tag: Busy: 0 Value: 0.0 R5: Tag: R6: Tag: Busy: 0 Value: 0.0 R7: Tag: Busy: 0 Value: 0.0 R8: Tag: Busy: 0 Value: 0.0 Busy: 0 Value: 0.0 R9: Tag: Busy: 0 Value: 0.0 R10: Tag: R11: Tag: Busy: 0 Value: 0.0 R12: Tag: A1 Busy: 1 Value: 99.0

R13: Tag: Busy: 0 Value: 0.0 R14: Tag: Busy: 0 Value: 0.0 R15: Tag: Busy: 0 Value: 5.0 Busy: 0 Value: 0.0 R16: Tag:

Busy: 0 Value: 0.0 R17: Tag: R18: Tag: Busy: 0 Value: 0.0 Busy: 0 Value: 0.0 R19: Tag:

Memory:

M0: 0.0 M1: 99.0

M2: 2.0 M3: 0.0 M4: 0.0

M5: 0.0 M6: 0.0

Common Data Bus:

Tag: A3 Value: PC value is: 0 Current Instruction in PC: SD R12 1

Instructions To Write: Stall Branch: false

Stall: false

Instruction to be issued: SD R12 1 false

stall is now false : false

Issue cycle of SD R12 1 is 13

Made load read to write

Clock Cycle: 13 PC Value: 3

**Reservation Stations:** 

Adder:

Adder position0: Tag: A1 Start Cycle: 13 Execute End Cycle: 14 Busy: 1 Instruction Qk: A: Duration left: 1 Ready To Write: false Type: ADDI Vj: 99.0 Vk: 99 Qj: Adder position1: Tag: A2 Start Cycle: -1 Execute End Cycle: -1 Busy: 0 Instruction Type: None Vi: Vk: Qi: Qk: A: Duration left: -1 Ready To Write: false Adder position2: Tag: A3 Start Cycle: -1 Execute End Cycle: -1 Busy: 0 Instruction Duration left: -1 Ready To Write: false Type: None Vj: Vk: Qk: Qj: A: Multiplier:

Multiplier position0:

Tag: M1 Start Cycle: -1 Execute End Cycle: -1 Busy: 0 Instruction Type: None Vj: Vk:

Qj: Qk: A: Duration left: -1 Ready To Write: false

Multiplier position1:

Tag: M2 Start Cycle: -1 Execute End Cycle: -1 Busy: 0 Instruction Type: None Vj: Vk:

Qj: Qk: A: Duration left: -1 Ready To Write: false

Load Buffers:

Load buffer position0:

Tag: L1 Busy: 1 Effective Address: 2 Start Cycle: 12 Execute End Cycle: 13 Duration left:

1 Ready To Write: true

Load buffer position1:

Tag: L2 Busy: 0 Effective Address: -1 Start Cycle: -1 Execute End Cycle: -1 Duration left:

-1 Ready To Write: false

Load buffer position2:

Tag: L3 Busy: 0 Effective Address: -1 Start Cycle: -1 Execute End Cycle: -1 Duration left:

-1 Ready To Write: false

Store Buffers:

Store buffer position0:

Tag: S1 Busy: 1 Effective Address: 1 Start Cycle: -1 Execute End Cycle: -1 Duration left:

1 Ready To Write: false

Store buffer position1:

Tag: S2 Busy: 0 Effective Address: -1 Start Cycle: -1 Execute End Cycle: -1 Duration left:

-1 Ready To Write: false

Store buffer position2:

Tag: S3 Busy: 0 Effective Address: -1 Start Cycle: -1 Execute End Cycle: -1 Duration left:

-1 Ready To Write: false

Register File:

R8: Tag:

R0: Tag: L1 Busy: 1 Value: 2.0 Busy: 0 Value: 0.0 R1: Tag: R2: Tag: Busy: 0 Value: 3.0 R3: Tag: Busy: 0 Value: 0.0 R4: Tag: Busy: 0 Value: 1.0 R5: Tag: Busy: 0 Value: 0.0 Busy: 0 Value: 0.0 R6: Tag: R7: Tag: Busy: 0 Value: 0.0

Busy: 0 Value: 0.0

```
R9: Tag:
             Busy: 0 Value: 0.0
R10: Tag:
             Busy: 0 Value: 0.0
             Busy: 0 Value: 0.0
R11: Tag:
R12: Tag: A1 Busy: 1 Value: 99.0
             Busy: 0 Value: 0.0
R13: Tag:
R14: Tag:
             Busy: 0 Value: 0.0
R15: Tag:
             Busy: 0 Value: 5.0
R16: Tag:
             Busy: 0 Value: 0.0
R17: Tag:
             Busy: 0 Value: 0.0
R18: Tag:
             Busy: 0 Value: 0.0
R19: Tag:
             Busy: 0 Value: 0.0
```

Memory: M0: 0.0 M1: 99.0 M2: 2.0 M3: 0.0 M4: 0.0 M5: 0.0 M6: 0.0

Common Data Bus:

Tag: A3 Value: PC value is: 0

Current Instruction in PC: SUBI R15 R15 5

Instructions To Write:

LD F0 2

Stall Branch: false

Stall: false

-----

Instruction to be issued: SUBI R15 R15 5 false

stall is now false: false

Issue cycle of SUBI R15 R15 5 is 14

Value of memory is: 2.0 and effective address is: 2

Instruction to be written: LD F0 2

Clock Cycle: 14 PC Value: 4

**Reservation Stations:** 

Adder:

Adder position0: Tag: A1 Start Cycle: 13 Execute End Cycle: 14 Busy: 1 Instruction Type: ADDI Vj: 99.0 Vk: 99 Qj: Qk: A: Duration left: 1 Ready To Write: true Adder position1: Tag: A2 Start Cycle: -1 Execute End Cycle: -1 Busy: 1 Instruction Type: SUBI Vj: 5.0 Vk: 5 Qj: Qk: A: Duration left: 1 Ready To Write: false Adder position2: Tag: A3 Start Cycle: -1 Execute End Cycle: -1 Busy: 0 Instruction Duration left: -1 Ready To Write: false Type: None Vj: Vk: Qj: Qk: A: Multiplier:

Multiplier position0:

Tag: M1 Start Cycle: -1 Execute End Cycle: -1 Busy: 0 Instruction Type: None Vj: Vk. Qj: Qk: A: Duration left: -1 Ready To Write: false Multiplier position1:

```
Tag: M2 Start Cycle: -1 Execute End Cycle: -1 Busy: 0 Instruction Type: None Vj:
Qj:
     Qk:
           A:
                  Duration left: -1
                                     Ready To Write: false
Load Buffers:
Load buffer position0:
Tag: L1 Busy: 0 Effective Address: -1 Start Cycle: -1 Execute End Cycle: -1 Duration left:
      Ready To Write: false
Load buffer position1:
Tag: L2 Busy: 0 Effective Address: -1 Start Cycle: -1 Execute End Cycle: -1 Duration left:
      Ready To Write: false
Load buffer position2:
Tag: L3 Busy: 0 Effective Address: -1 Start Cycle: -1 Execute End Cycle: -1 Duration left:
      Ready To Write: false
Store Buffers:
Store buffer position0:
Tag: S1 Busy: 1 Effective Address: 1
                                      Start Cycle: -1 Execute End Cycle: -1 Duration left:
      Ready To Write: false
Store buffer position1:
Tag: S2 Busy: 0 Effective Address: -1 Start Cycle: -1 Execute End Cycle: -1 Duration left:
      Ready To Write: false
-1
Store buffer position2:
Tag: S3 Busy: 0 Effective Address: -1 Start Cycle: -1 Execute End Cycle: -1 Duration left:
-1
      Ready To Write: false
Register File:
R0: Tag:
             Busy: 0 Value: 2.0
R1: Tag:
             Busy: 0 Value: 0.0
R2: Tag:
             Busy: 0 Value: 3.0
             Busy: 0 Value: 0.0
R3: Tag:
             Busy: 0 Value: 1.0
R4: Tag:
R5: Tag:
             Busy: 0 Value: 0.0
             Busy: 0 Value: 0.0
R6: Tag:
R7: Tag:
             Busy: 0 Value: 0.0
R8: Tag:
             Busy: 0 Value: 0.0
R9: Tag:
             Busy: 0 Value: 0.0
R10: Tag:
             Busy: 0 Value: 0.0
R11: Tag:
             Busy: 0 Value: 0.0
R12: Tag: A1
               Busy: 1 Value: 99.0
R13: Tag:
             Busy: 0 Value: 0.0
R14: Tag:
             Busy: 0 Value: 0.0
R15: Tag: A2 Busy: 1 Value: 5.0
R16: Tag:
             Busy: 0 Value: 0.0
R17: Tag:
             Busy: 0 Value: 0.0
R18: Tag:
             Busy: 0 Value: 0.0
R19: Tag:
             Busy: 0 Value: 0.0
Memory:
M0: 0.0
M1: 99.0
M2: 2.0
```

M3: 0.0

M4: 0.0 M5: 0.0 M6: 0.0

Common Data Bus: Tag: L1 Value: 2.0

Current Instruction in PC: BNEZ R15 LOOP

Instructions To Write: ADDI R12 R12 99 Stall Branch: false

Stall: false

-----

Instruction to be issued: BNEZ R15 LOOP false

stall is now false: false

------Stall due to Branch------Issue cycle of BNEZ R15 LOOP is 15
Instruction to be written: ADDI R12 R12 99

Clock Cycle: 15 PC Value: 5

Reservation Stations:

Adder:

Adder position0: Tag: A1 Start Cycle: -1 Execute End Cycle: -1 Busy: 0 Instruction Type: None Vj: Vk: Qj: Qk: A: Duration left: -1 Ready To Write: false Adder position1: Tag: A2 Start Cycle: 15 Execute End Cycle: 16 Busy: 1 Instruction Type: SUBI Vj: 5.0 Vk: 5 Qj: Qk: A: Duration left: 1 Ready To Write: false Adder position2: Tag: A3 Start Cycle: -1 Execute End Cycle: -1 Busy: 1 Instruction Type: BNEZ Vj: Vk: Qj: A2 Qk: A: Duration left: 1 Ready To Write: false Multiplier:

Multiplier position0:

Tag: M1 Start Cycle: -1 Execute End Cycle: -1 Busy: 0 Instruction Type: None Vj: Vk: Qj: Qk: A: Duration left: -1 Ready To Write: false

Multiplier position1:

Tag: M2 Start Cycle: -1 Execute End Cycle: -1 Busy: 0 Instruction Type: None Vj: Vk:

Qi: Qk: A: Duration left: -1 Ready To Write: false

Load Buffers:

Load buffer position0:

Tag: L1 Busy: 0 Effective Address: -1 Start Cycle: -1 Execute End Cycle: -1 Duration left:

-1 Ready To Write: false

Load buffer position1:

Tag: L2 Busy: 0 Effective Address: -1 Start Cycle: -1 Execute End Cycle: -1 Duration left:

-1 Ready To Write: false

Load buffer position2:

Tag: L3 Busy: 0 Effective Address: -1 Start Cycle: -1 Execute End Cycle: -1 Duration left:

-1 Ready To Write: false

Store Buffers:

Store buffer position0:

Tag: S1 Busy: 1 Effective Address: 1 Start Cycle: -1 Execute End Cycle: -1 Duration left:

1 Ready To Write: false

Store buffer position1:

```
Tag: S2 Busy: 0 Effective Address: -1 Start Cycle: -1 Execute End Cycle: -1 Duration left:
-1
      Ready To Write: false
Store buffer position2:
Tag: S3 Busy: 0 Effective Address: -1 Start Cycle: -1 Execute End Cycle: -1 Duration left:
-1
      Ready To Write: false
Register File:
             Busy: 0 Value: 2.0
R0: Tag:
R1: Tag:
             Busy: 0 Value: 0.0
             Busy: 0 Value: 3.0
R2: Tag:
             Busy: 0 Value: 0.0
R3: Tag:
R4: Tag:
             Busy: 0 Value: 1.0
             Busy: 0 Value: 0.0
R5: Tag:
R6: Tag:
             Busy: 0 Value: 0.0
R7: Tag:
             Busy: 0 Value: 0.0
             Busy: 0 Value: 0.0
R8: Tag:
             Busy: 0 Value: 0.0
R9: Tag:
R10: Tag:
             Busy: 0 Value: 0.0
R11: Tag:
             Busy: 0 Value: 0.0
             Busy: 0 Value: 198.0
R12: Tag:
R13: Tag:
             Busy: 0 Value: 0.0
R14: Tag:
             Busy: 0 Value: 0.0
R15: Tag: A2 Busy: 1 Value: 5.0
R16: Tag:
             Busy: 0 Value: 0.0
R17: Tag:
             Busy: 0 Value: 0.0
R18: Tag:
             Busy: 0 Value: 0.0
R19: Tag:
             Busy: 0 Value: 0.0
Memory:
M0: 0.0
M1: 99.0
M2: 2.0
M3: 0.0
M4: 0.0
M5: 0.0
M6: 0.0
Common Data Bus:
Tag: A1 Value: 198.0
Current Instruction in PC: ADDI R13 R13 99
Instructions To Write:
Stall Branch: true
Stall: false
Instruction to be issued: ADDI R13 R13 99 false
Clock Cycle: 16
PC Value: 5
Reservation Stations:
Adder:
```

Start Cycle: -1 Execute End Cycle: -1 Busy: 0 Instruction

Duration left: -1 Ready To Write: false

Adder position0: Tag: A1

Type: None Vj: Vk: Qj: Qk: A:

Adder position1: Tag: A2 Start Cycle: 15 Execute End Cycle: 16 Busy: 1 Instruction Type: SUBI Vj: 5.0 Vk: 5 Qj: Qk: A: Duration left: 1 Ready To Write: true Adder position2: Tag: A3 Start Cycle: -1 Execute End Cycle: -1 Busy: 1 Instruction Type: BNEZ Vj: Vk: Qj: A2 Qk: A: Duration left: 1 Ready To Write: false Multiplier:

Multiplier position0:

Tag: M1 Start Cycle: -1 Execute End Cycle: -1 Busy: 0 Instruction Type: None Vj: Vk:

Qj: Qk: A: Duration left: -1 Ready To Write: false

Multiplier position1:

Tag: M2 Start Cycle: -1 Execute End Cycle: -1 Busy: 0 Instruction Type: None Vj: Vk:

Qi: Qk: A: Duration left: -1 Ready To Write: false

Load Buffers:

Load buffer position0:

Tag: L1 Busy: 0 Effective Address: -1 Start Cycle: -1 Execute End Cycle: -1 Duration left:

-1 Ready To Write: false

Load buffer position1:

Tag: L2 Busy: 0 Effective Address: -1 Start Cycle: -1 Execute End Cycle: -1 Duration left:

-1 Ready To Write: false

Load buffer position2:

Tag: L3 Busy: 0 Effective Address: -1 Start Cycle: -1 Execute End Cycle: -1 Duration left:

-1 Ready To Write: false

Store Buffers:

Store buffer position0:

Tag: S1 Busy: 1 Effective Address: 1 Start Cycle: 16 Execute End Cycle: 17 Duration left:

1 Ready To Write: false

Store buffer position1:

Tag: S2 Busy: 0 Effective Address: -1 Start Cycle: -1 Execute End Cycle: -1 Duration left:

-1 Ready To Write: false

Store buffer position2:

Tag: S3 Busy: 0 Effective Address: -1 Start Cycle: -1 Execute End Cycle: -1 Duration left:

-1 Ready To Write: false

Register File:

R0: Tag: Busy: 0 Value: 2.0

R1: Tag: Busy: 0 Value: 0.0

R2: Tag: Busy: 0 Value: 3.0

R3: Tag: Busy: 0 Value: 0.0

R4: Tag: Busy: 0 Value: 1.0

R5: Tag: Busy: 0 Value: 0.0

R6: Tag: Busy: 0 Value: 0.0

R7: Tag: Busy: 0 Value: 0.0

R8: Tag: Busy: 0 Value: 0.0

R9: Tag: Busy: 0 Value: 0.0

R10: Tag: Busy: 0 Value: 0.0

R11: Tag: Busy: 0 Value: 0.0

R12: Tag: Busy: 0 Value: 198.0

R13: Tag: Busy: 0 Value: 0.0

R14: Tag: Busy: 0 Value: 0.0

R15: Tag: A2 Busy: 1 Value: 5.0

R16: Tag: Busy: 0 Value: 0.0 R17: Tag: Busy: 0 Value: 0.0 Busy: 0 Value: 0.0 R18: Tag: Busy: 0 Value: 0.0 R19: Tag: Memory: M0: 0.0 M1: 99.0 M2: 2.0 M3: 0.0 M4: 0.0 M5: 0.0 M6: 0.0 Common Data Bus: Tag: A1 Value: 198.0 Current Instruction in PC: ADDI R13 R13 99 Instructions To Write: SUBI R15 R15 5 Stall Branch: true Stall: false Instruction to be issued: ADDI R13 R13 99 false sTORE FINISHED-----Instruction to be written: SUBI R15 R15 5 Clock Cycle: 17 PC Value: 5 **Reservation Stations:** Adder: Adder position0: Tag: A1 Start Cycle: -1 Execute End Cycle: -1 Busy: 0 Instruction Type: None Vj: Qk: A: Duration left: -1 Ready To Write: false Vk: Qj: Adder position1: Tag: A2 Start Cycle: -1 Execute End Cycle: -1 Busy: 0 Instruction Type: None Vj: Vk: Qk: Duration left: -1 Ready To Write: false Qj: A: Start Cycle: -1 Execute End Cycle: -1 Busy: 1 Instruction Adder position2: Tag: A3 Type: BNEZ Vj: 0.0 Vk: Qi: Qk: A: Duration left: 1 Ready To Write: false Multiplier: Multiplier position0: Tag: M1 Start Cycle: -1 Execute End Cycle: -1 Busy: 0 Instruction Type: None Vi: Vk: A: Duration left: -1 Ready To Write: false Qj: Qk: Multiplier position1: Tag: M2 Start Cycle: -1 Execute End Cycle: -1 Busy: 0 Instruction Type: None Vi: Qj: Qk: A: Duration left: -1 Ready To Write: false Load Buffers: Load buffer position0:

Load buffer position1:

-1

Tag: L2 Busy: 0 Effective Address: -1 Start Cycle: -1 Execute End Cycle: -1 Duration left:

Tag: L1 Busy: 0 Effective Address: -1 Start Cycle: -1 Execute End Cycle: -1 Duration left:

-1 Ready To Write: false

Ready To Write: false

Load buffer position2:

```
Tag: L3 Busy: 0 Effective Address: -1 Start Cycle: -1 Execute End Cycle: -1 Duration left:
-1
      Ready To Write: false
Store Buffers:
Store buffer position0:
Tag: S1 Busy: 0 Effective Address: -1 Start Cycle: -1 Execute End Cycle: -1 Duration left:
      Ready To Write: false
Store buffer position1:
Tag: S2 Busy: 0 Effective Address: -1 Start Cycle: -1 Execute End Cycle: -1 Duration left:
      Ready To Write: false
Store buffer position2:
Tag: S3 Busy: 0 Effective Address: -1 Start Cycle: -1 Execute End Cycle: -1 Duration left:
      Ready To Write: false
Register File:
R0: Tag:
             Busy: 0 Value: 2.0
R1: Tag:
             Busy: 0 Value: 0.0
R2: Tag:
             Busy: 0 Value: 3.0
R3: Tag:
             Busy: 0 Value: 0.0
R4: Tag:
             Busy: 0 Value: 1.0
R5: Tag:
             Busy: 0 Value: 0.0
R6: Tag:
             Busy: 0 Value: 0.0
             Busy: 0 Value: 0.0
R7: Tag:
             Busy: 0 Value: 0.0
R8: Tag:
R9: Tag:
             Busy: 0 Value: 0.0
R10: Tag:
             Busy: 0 Value: 0.0
R11: Tag:
             Busy: 0 Value: 0.0
             Busy: 0 Value: 198.0
R12: Tag:
             Busy: 0 Value: 0.0
R13: Tag:
R14: Tag:
             Busy: 0 Value: 0.0
R15: Tag:
             Busy: 0 Value: 0.0
             Busy: 0 Value: 0.0
R16: Tag:
R17: Tag:
             Busy: 0 Value: 0.0
             Busy: 0 Value: 0.0
R18: Tag:
R19: Tag:
             Busy: 0 Value: 0.0
Memory:
M0: 0.0
M1: 198.0
M2: 2.0
M3: 0.0
M4: 0.0
M5: 0.0
M6: 0.0
Common Data Bus:
Tag: A2 Value: 0.0
Current Instruction in PC: ADDI R13 R13 99
Instructions To Write:
Stall Branch: true
```

\_\_\_\_\_

Stall: false

Instruction to be issued: ADDI R13 R13 99 false

Clock Cycle: 18 PC Value: 5

Reservation Stations:

Adder:

Adder position0: Tag: A1 Start Cycle: -1 Execute End Cycle: -1 Busy: 0 Instruction Vk: Qj: Type: None Vj: Qk: A: Duration left: -1 Ready To Write: false Adder position1: Tag: A2 Start Cycle: -1 Execute End Cycle: -1 Busy: 0 Instruction Type: None Vj: Vk: Qj: Qk: A: Duration left: -1 Ready To Write: false Adder position2: Tag: A3 Start Cycle: 18 Execute End Cycle: 19 Busy: 1 Instruction Duration left: 1 Ready To Write: false Type: BNEZ Vj: 0.0 Vk: Qj: Qk: A: Multiplier:

Multiplier position0:

Tag: M1 Start Cycle: -1 Execute End Cycle: -1 Busy: 0 Instruction Type: None Vj: Vk:

Qj: Qk: A: Duration left: -1 Ready To Write: false

Multiplier position1:

Tag: M2 Start Cycle: -1 Execute End Cycle: -1 Busy: 0 Instruction Type: None Vj: Vk:

Qj: Qk: A: Duration left: -1 Ready To Write: false

Load Buffers:

Load buffer position0:

Tag: L1 Busy: 0 Effective Address: -1 Start Cycle: -1 Execute End Cycle: -1 Duration left:

-1 Ready To Write: false

Load buffer position1:

Tag: L2 Busy: 0 Effective Address: -1 Start Cycle: -1 Execute End Cycle: -1 Duration left:

-1 Ready To Write: false

Load buffer position2:

Tag: L3 Busy: 0 Effective Address: -1 Start Cycle: -1 Execute End Cycle: -1 Duration left:

-1 Ready To Write: false

Store Buffers:

Store buffer position0:

Tag: S1 Busy: 0 Effective Address: -1 Start Cycle: -1 Execute End Cycle: -1 Duration left:

-1 Ready To Write: false

Store buffer position1:

Tag: S2 Busy: 0 Effective Address: -1 Start Cycle: -1 Execute End Cycle: -1 Duration left:

-1 Ready To Write: false

Store buffer position2:

Tag: S3 Busy: 0 Effective Address: -1 Start Cycle: -1 Execute End Cycle: -1 Duration left:

-1 Ready To Write: false

Register File:

R0: Tag: Busy: 0 Value: 2.0
R1: Tag: Busy: 0 Value: 0.0
R2: Tag: Busy: 0 Value: 3.0
R3: Tag: Busy: 0 Value: 0.0

R4: Tag: Busy: 0 Value: 1.0 R5: Tag: Busy: 0 Value: 0.0

R6: Tag: Busy: 0 Value: 0.0 R7: Tag: Busy: 0 Value: 0.0

R8: Tag: Busy: 0 Value: 0.0

```
R9: Tag:
             Busy: 0 Value: 0.0
R10: Tag:
             Busy: 0 Value: 0.0
             Busy: 0 Value: 0.0
R11: Tag:
R12: Tag:
             Busy: 0 Value: 198.0
             Busy: 0 Value: 0.0
R13: Tag:
             Busy: 0 Value: 0.0
R14: Tag:
R15: Tag:
             Busy: 0 Value: 0.0
R16: Tag:
             Busy: 0 Value: 0.0
R17: Tag:
             Busy: 0 Value: 0.0
R18: Tag:
             Busy: 0 Value: 0.0
R19: Tag:
             Busy: 0 Value: 0.0
Memory:
M0: 0.0
M1: 198.0
M2: 2.0
M3: 0.0
M4: 0.0
M5: 0.0
M6: 0.0
Common Data Bus:
Tag: A2 Value: 0.0
Current Instruction in PC: ADDI R13 R13 99
Instructions To Write:
Stall Branch: true
Stall: false
Instruction to be issued: ADDI R13 R13 99 false
Clock Cycle: 19
PC Value: 5
Reservation Stations:
Adder:
                            Start Cycle: -1 Execute End Cycle: -1 Busy: 0 Instruction
Adder position0: Tag: A1
                                          Duration left: -1 Ready To Write: false
Type: None Vi:
                              Qk:
                                    A:
                 Vk:
                        Qj:
Adder position1: Tag: A2
                            Start Cycle: -1 Execute End Cycle: -1 Busy: 0 Instruction
Type: None Vj:
                Vk:
                        Qj:
                              Qk:
                                    A:
                                          Duration left: -1 Ready To Write: false
Adder position2: Tag: A3
                            Start Cycle: 18 Execute End Cycle: 19 Busy: 1 Instruction
Type: BNEZ Vj: 0.0 Vk:
                               Qk: A:
                                            Duration left: 1 Ready To Write: true
                          Qj:
Multiplier:
Multiplier position0:
Tag: M1 Start Cycle: -1 Execute End Cycle: -1 Busy: 0 Instruction Type: None Vj:
                                                                                   Vk:
                                     Ready To Write: false
     Qk:
           A:
                 Duration left: -1
Multiplier position1:
Tag: M2 Start Cycle: -1 Execute End Cycle: -1 Busy: 0 Instruction Type: None Vj:
                                                                                   Vk:
                                     Ready To Write: false
     Qk: A:
                 Duration left: -1
Load Buffers:
Load buffer position0:
```

Tag: L1 Busy: 0 Effective Address: -1 Start Cycle: -1 Execute End Cycle: -1 Duration left: -1 Ready To Write: false

Load buffer position1:
Tag: L2 Busy: 0 Effective Address: -1 Start Cycle: -1 Execute End Cycle: -1 Duration left:
-1 Ready To Write: false
Load buffer position2:
Tag: L3 Busy: 0 Effective Address: -1 Start Cycle: -1 Execute End Cycle: -1 Duration left:
-1 Ready To Write: false
Store Buffers:
Store buffer position0:

Tag: S1 Busy: 0 Effective Address: -1 Start Cycle: -1 Execute End Cycle: -1 Duration left: -1 Ready To Write: false

Store buffer position1:

Tag: S2 Busy: 0 Effective Address: -1 Start Cycle: -1 Execute End Cycle: -1 Duration left:

-1 Ready To Write: false

Store buffer position2:

Tag: S3 Busy: 0 Effective Address: -1 Start Cycle: -1 Execute End Cycle: -1 Duration left:

-1 Ready To Write: false

Register File:

R0: Tag: Busy: 0 Value: 2.0 Busy: 0 Value: 0.0 R1: Tag: Busy: 0 Value: 3.0 R2: Tag: R3: Tag: Busy: 0 Value: 0.0 R4: Tag: Busy: 0 Value: 1.0 R5: Tag: Busy: 0 Value: 0.0 R6: Tag: Busy: 0 Value: 0.0 R7: Tag: Busy: 0 Value: 0.0 R8: Tag: Busy: 0 Value: 0.0 Busy: 0 Value: 0.0 R9: Tag: Busy: 0 Value: 0.0 R10: Tag: R11: Tag: Busy: 0 Value: 0.0 R12: Tag: Busy: 0 Value: 198.0 R13: Tag: Busy: 0 Value: 0.0 R14: Tag: Busy: 0 Value: 0.0 R15: Tag: Busy: 0 Value: 0.0 R16: Tag: Busy: 0 Value: 0.0 R17: Tag: Busy: 0 Value: 0.0 R18: Tag: Busy: 0 Value: 0.0 Busy: 0 Value: 0.0 R19: Tag:

Memory:

M0: 0.0 M1: 198.0 M2: 2.0 M3: 0.0 M4: 0.0 M5: 0.0

M6: 0.0

Common Data Bus:

Tag: A2 Value: 0.0

Current Instruction in PC: ADDI R13 R13 99

Instructions To Write: BNEZ R15 LOOP Stall Branch: true

Stall: false

\_\_\_\_\_

Instruction to be issued: ADDI R13 R13 99 false Instruction to be written: BNEZ R15 LOOP

Clock Cycle: 20 PC Value: 5

**Reservation Stations:** 

Adder:

Adder position0: Tag: A1 Start Cycle: -1 Execute End Cycle: -1 Busy: 0 Instruction Type: None Vj: Qk: Duration left: -1 Ready To Write: false Vk: Qj: A: Adder position1: Tag: A2 Start Cycle: -1 Execute End Cycle: -1 Busy: 0 Instruction Duration left: -1 Ready To Write: false Type: None Vj: Vk: Qk: A: Qj: Adder position2: Tag: A3 Start Cycle: -1 Execute End Cycle: -1 Busy: 0 Instruction Type: None Vj: Vk: Qj: Qk: A: Duration left: -1 Ready To Write: false Multiplier:

Multiplier position0:

Tag: M1 Start Cycle: -1 Execute End Cycle: -1 Busy: 0 Instruction Type: None Vj: Vk:

Qj: Qk: A: Duration left: -1 Ready To Write: false

Multiplier position1:

Tag: M2 Start Cycle: -1 Execute End Cycle: -1 Busy: 0 Instruction Type: None Vj: Vk:

Qj: Qk: A: Duration left: -1 Ready To Write: false

Load Buffers:

Load buffer position0:

Tag: L1 Busy: 0 Effective Address: -1 Start Cycle: -1 Execute End Cycle: -1 Duration left:

-1 Ready To Write: false

Load buffer position1:

Tag: L2 Busy: 0 Effective Address: -1 Start Cycle: -1 Execute End Cycle: -1 Duration left:

-1 Ready To Write: false

Load buffer position2:

Tag: L3 Busy: 0 Effective Address: -1 Start Cycle: -1 Execute End Cycle: -1 Duration left:

-1 Ready To Write: false

Store Buffers:

Store buffer position0:

Tag: S1 Busy: 0 Effective Address: -1 Start Cycle: -1 Execute End Cycle: -1 Duration left:

-1 Ready To Write: false

Store buffer position1:

Tag: S2 Busy: 0 Effective Address: -1 Start Cycle: -1 Execute End Cycle: -1 Duration left:

-1 Ready To Write: false

Store buffer position2:

Tag: S3 Busy: 0 Effective Address: -1 Start Cycle: -1 Execute End Cycle: -1 Duration left:

-1 Ready To Write: false

Register File:

R0: Tag: Busy: 0 Value: 2.0 R1: Tag: Busy: 0 Value: 0.0 R2: Tag: Busy: 0 Value: 3.0

```
R3: Tag:
             Busy: 0 Value: 0.0
R4: Tag:
             Busy: 0 Value: 1.0
             Busy: 0 Value: 0.0
R5: Tag:
R6: Tag:
             Busy: 0 Value: 0.0
R7: Tag:
             Busy: 0 Value: 0.0
R8: Tag:
             Busy: 0 Value: 0.0
R9: Tag:
             Busy: 0 Value: 0.0
R10: Tag:
             Busy: 0 Value: 0.0
R11: Tag:
             Busy: 0 Value: 0.0
R12: Tag:
             Busy: 0 Value: 198.0
R13: Tag:
             Busy: 0 Value: 0.0
             Busy: 0 Value: 0.0
R14: Tag:
R15: Tag:
             Busy: 0 Value: 0.0
R16: Tag:
             Busy: 0 Value: 0.0
             Busy: 0 Value: 0.0
R17: Tag:
             Busy: 0 Value: 0.0
R18: Tag:
R19: Tag:
             Busy: 0 Value: 0.0
Memory:
```

M0: 0.0 M1: 198.0 M2: 2.0 M3: 0.0 M4: 0.0 M5: 0.0 M6: 0.0

Common Data Bus:

Tag: A3 Value: PC value is: 5

Current Instruction in PC: ADDI R13 R13 99

Instructions To Write: Stall Branch: false

Stall: false

Instruction to be issued: ADDI R13 R13 99 false

stall is now false : false

Issue cycle of ADDI R13 R13 99 is 21

Clock Cycle: 21 PC Value: 6

**Reservation Stations:** 

Adder:

Adder position0: Tag: A1 Start Cycle: -1 Execute End Cycle: -1 Busy: 1 Instruction Type: ADDI Vj: 0.0 Vk: 99 Qj: Duration left: 1 Ready To Write: false Qk: A: Adder position1: Tag: A2 Start Cycle: -1 Execute End Cycle: -1 Busy: 0 Instruction Type: None Vj: Duration left: -1 Ready To Write: false Vk: Qj: Qk: A: Adder position2: Tag: A3 Start Cycle: -1 Execute End Cycle: -1 Busy: 0 Instruction Type: None Vj: Duration left: -1 Ready To Write: false Vk: Qk: A: Qj: Multiplier:

Multiplier position0:

```
Tag: M1 Start Cycle: -1 Execute End Cycle: -1 Busy: 0 Instruction Type: None Vi
                                                                                    Vk:
Qj:
     Qk:
           A:
                  Duration left: -1
                                     Ready To Write: false
Multiplier position1:
Tag: M2 Start Cycle: -1 Execute End Cycle: -1 Busy: 0 Instruction Type: None Vj:
                                                                                    Vk:
Qj:
           A:
                  Duration left: -1
                                     Ready To Write: false
     Qk:
Load Buffers:
Load buffer position0:
Tag: L1 Busy: 0 Effective Address: -1 Start Cycle: -1 Execute End Cycle: -1 Duration left:
      Ready To Write: false
Load buffer position1:
Tag: L2 Busy: 0 Effective Address: -1 Start Cycle: -1 Execute End Cycle: -1 Duration left:
      Ready To Write: false
Load buffer position2:
Tag: L3 Busy: 0 Effective Address: -1 Start Cycle: -1 Execute End Cycle: -1 Duration left:
      Ready To Write: false
Store Buffers:
Store buffer position0:
Tag: S1 Busy: 0 Effective Address: -1 Start Cycle: -1 Execute End Cycle: -1 Duration left:
      Ready To Write: false
-1
Store buffer position1:
Tag: S2 Busy: 0 Effective Address: -1 Start Cycle: -1 Execute End Cycle: -1 Duration left:
-1
      Ready To Write: false
Store buffer position2:
Tag: S3 Busy: 0 Effective Address: -1 Start Cycle: -1 Execute End Cycle: -1 Duration left:
-1
      Ready To Write: false
Register File:
R0: Tag:
             Busy: 0 Value: 2.0
R1: Tag:
             Busy: 0 Value: 0.0
R2: Tag:
             Busy: 0 Value: 3.0
             Busy: 0 Value: 0.0
R3: Tag:
R4: Tag:
             Busy: 0 Value: 1.0
R5: Tag:
             Busy: 0 Value: 0.0
R6: Tag:
             Busy: 0 Value: 0.0
R7: Tag:
             Busy: 0 Value: 0.0
R8: Tag:
             Busy: 0 Value: 0.0
R9: Tag:
             Busy: 0 Value: 0.0
             Busy: 0 Value: 0.0
R10: Tag:
R11: Tag:
             Busy: 0 Value: 0.0
             Busy: 0 Value: 198.0
R12: Tag:
R13: Tag: A1 Busy: 1 Value: 0.0
R14: Tag:
             Busy: 0 Value: 0.0
R15: Tag:
             Busy: 0 Value: 0.0
R16: Tag:
             Busy: 0 Value: 0.0
R17: Tag:
             Busy: 0 Value: 0.0
R18: Tag:
             Busy: 0 Value: 0.0
R19: Tag:
             Busy: 0 Value: 0.0
Memory:
```

M0: 0.0

M1: 198.0 M2: 2.0 M3: 0.0 M4: 0.0 M5: 0.0

M6: 0.0

Common Data Bus:

Tag: A3 Value: PC value is: 5

Instructions To Write: Stall Branch: false

Stall: false

\_\_\_\_\_

Clock Cycle: 22 PC Value: 6

Reservation Stations:

Adder:

Adder position0: Tag: A1 Start Cycle: 22 Execute End Cycle: 23 Busy: 1 Instruction Duration left: 1 Ready To Write: false Type: ADDI Vj: 0.0 Vk: 99 Qj: Qk: A: Adder position1: Tag: A2 Start Cycle: -1 Execute End Cycle: -1 Busy: 0 Instruction Type: None Vj: Duration left: -1 Ready To Write: false Vk: Qj: Qk: A: Adder position2: Tag: A3 Start Cycle: -1 Execute End Cycle: -1 Busy: 0 Instruction Duration left: -1 Ready To Write: false Type: None Vi: Vk: Qk: A: Qi: Multiplier:

Multiplier position0:

Tag: M1 Start Cycle: -1 Execute End Cycle: -1 Busy: 0 Instruction Type: None Vj: Vk: Qj: Qk: A: Duration left: -1 Ready To Write: false Multiplier position1:

Tag: M2 Start Cycle: -1 Execute End Cycle: -1 Busy: 0 Instruction Type: None Vj: Qj: Qk: A: Duration left: -1 Ready To Write: false

Load Buffers:

Load buffer position0:

Tag: L1 Busy: 0 Effective Address: -1 Start Cycle: -1 Execute End Cycle: -1 Duration left:

-1 Ready To Write: false

Load buffer position1:

Tag: L2 Busy: 0 Effective Address: -1 Start Cycle: -1 Execute End Cycle: -1 Duration left:

-1 Ready To Write: false

Load buffer position2:

Tag: L3 Busy: 0 Effective Address: -1 Start Cycle: -1 Execute End Cycle: -1 Duration left:

-1 Ready To Write: false

Store Buffers:

Store buffer position0:

Tag: S1 Busy: 0 Effective Address: -1 Start Cycle: -1 Execute End Cycle: -1 Duration left:

-1 Ready To Write: false

Store buffer position1:

Tag: S2 Busy: 0 Effective Address: -1 Start Cycle: -1 Execute End Cycle: -1 Duration left:

-1 Ready To Write: false

Store buffer position2:

```
Tag: S3 Busy: 0 Effective Address: -1 Start Cycle: -1 Execute End Cycle: -1 Duration left:
-1
      Ready To Write: false
Register File:
R0: Tag:
             Busy: 0 Value: 2.0
R1: Tag:
             Busy: 0 Value: 0.0
R2: Tag:
             Busy: 0 Value: 3.0
R3: Tag:
             Busy: 0 Value: 0.0
R4: Tag:
             Busy: 0 Value: 1.0
R5: Tag:
             Busy: 0 Value: 0.0
             Busy: 0 Value: 0.0
R6: Tag:
             Busy: 0 Value: 0.0
R7: Tag:
             Busy: 0 Value: 0.0
R8: Tag:
R9: Tag:
             Busy: 0 Value: 0.0
R10: Tag:
             Busy: 0 Value: 0.0
             Busy: 0 Value: 0.0
R11: Tag:
             Busy: 0 Value: 198.0
R12: Tag:
R13: Tag: A1
               Busy: 1 Value: 0.0
R14: Tag:
             Busy: 0 Value: 0.0
             Busy: 0 Value: 0.0
R15: Tag:
             Busy: 0 Value: 0.0
R16: Tag:
R17: Tag:
             Busy: 0 Value: 0.0
             Busy: 0 Value: 0.0
R18: Tag:
R19: Tag:
             Busy: 0 Value: 0.0
Memory:
M0: 0.0
M1: 198.0
M2: 2.0
M3: 0.0
M4: 0.0
M5: 0.0
M6: 0.0
Common Data Bus:
Tag: A3 Value: PC value is: 5
Instructions To Write:
Stall Branch: false
Stall: false
Clock Cycle: 23
PC Value: 6
Reservation Stations:
Adder:
Adder position0: Tag: A1
                             Start Cycle: 22 Execute End Cycle: 23 Busy: 1 Instruction
Type: ADDI Vj: 0.0 Vk: 99 Qj:
                                             Duration left: 1 Ready To Write: true
                                Qk:
                                       A:
                             Start Cycle: -1 Execute End Cycle: -1 Busy: 0 Instruction
Adder position1: Tag: A2
Type: None Vj:
                                           Duration left: -1 Ready To Write: false
                  Vk:
                              Qk:
                                    A:
                        Qj:
Adder position2: Tag: A3
                             Start Cycle: -1 Execute End Cycle: -1 Busy: 0 Instruction
Type: None Vj:
                                           Duration left: -1 Ready To Write: false
                  Vk:
                        Qj:
                              Qk:
                                    A:
Multiplier:
```

```
Multiplier position0:
```

Tag: M1 Start Cycle: -1 Execute End Cycle: -1 Busy: 0 Instruction Type: None Vj: Vk:

Qj: Qk: A: Duration left: -1 Ready To Write: false

Multiplier position1:

Tag: M2 Start Cycle: -1 Execute End Cycle: -1 Busy: 0 Instruction Type: None Vj: Vk:

Qi: Qk: A: Duration left: -1 Ready To Write: false

Load Buffers:

Load buffer position0:

Tag: L1 Busy: 0 Effective Address: -1 Start Cycle: -1 Execute End Cycle: -1 Duration left:

-1 Ready To Write: false

Load buffer position1:

Tag: L2 Busy: 0 Effective Address: -1 Start Cycle: -1 Execute End Cycle: -1 Duration left:

-1 Ready To Write: false

Load buffer position2:

Tag: L3 Busy: 0 Effective Address: -1 Start Cycle: -1 Execute End Cycle: -1 Duration left:

-1 Ready To Write: false

Store Buffers:

Store buffer position0:

Tag: S1 Busy: 0 Effective Address: -1 Start Cycle: -1 Execute End Cycle: -1 Duration left:

-1 Ready To Write: false

Store buffer position1:

Tag: S2 Busy: 0 Effective Address: -1 Start Cycle: -1 Execute End Cycle: -1 Duration left:

-1 Ready To Write: false

Store buffer position2:

Tag: S3 Busy: 0 Effective Address: -1 Start Cycle: -1 Execute End Cycle: -1 Duration left:

-1 Ready To Write: false

Register File:

R0: Tag: Busy: 0 Value: 2.0

R1: Tag: Busy: 0 Value: 0.0

R2: Tag: Busy: 0 Value: 3.0

R3: Tag: Busy: 0 Value: 0.0

R4: Tag: Busy: 0 Value: 1.0

R5: Tag: Busy: 0 Value: 0.0

R6: Tag: Busy: 0 Value: 0.0

R7: Tag: Busy: 0 Value: 0.0

R8: Tag: Busy: 0 Value: 0.0

R9: Tag: Busy: 0 Value: 0.0

R10: Tag: Busy: 0 Value: 0.0

R11: Tag: Busy: 0 Value: 0.0

R12: Tag: Busy: 0 Value: 198.0

R13: Tag: A1 Busy: 1 Value: 0.0

R14: Tag: Busy: 0 Value: 0.0

R15: Tag: Busy: 0 Value: 0.0

R16: Tag: Busy: 0 Value: 0.0

R17: Tag: Busy: 0 Value: 0.0

R18: Tag: Busy: 0 Value: 0.0

R19: Tag: Busy: 0 Value: 0.0

Memory:

```
M0: 0.0
M1: 198.0
M2: 2.0
M3: 0.0
M4: 0.0
M5: 0.0
M6: 0.0
Common Data Bus:
Tag: A3 Value: PC value is: 5
Instructions To Write:
ADDI R13 R13 99
Stall Branch: false
Stall: false
Instruction to be written: ADDI R13 R13 99
Clock Cycle: 24
PC Value: 6
Reservation Stations:
Adder:
Adder position0: Tag: A1
                            Start Cycle: -1 Execute End Cycle: -1 Busy: 0 Instruction
                             Qk: A:
                                          Duration left: -1 Ready To Write: false
Type: None Vi:
                Vk: Qj:
Adder position1: Tag: A2
                            Start Cycle: -1 Execute End Cycle: -1 Busy: 0 Instruction
Type: None Vj:
                 Vk: Qj:
                              Qk:
                                    A:
                                          Duration left: -1 Ready To Write: false
Adder position2: Tag: A3
                            Start Cycle: -1 Execute End Cycle: -1 Busy: 0 Instruction
Type: None Vj:
                Vk:
                        Qj: Qk:
                                   A:
                                          Duration left: -1 Ready To Write: false
Multiplier:
Multiplier position0:
Tag: M1 Start Cycle: -1 Execute End Cycle: -1 Busy: 0 Instruction Type: None Vj:
                                                                                   Vk:
Qi: Qk: A:
                 Duration left: -1
                                     Ready To Write: false
Multiplier position1:
Tag: M2 Start Cycle: -1 Execute End Cycle: -1 Busy: 0 Instruction Type: None Vj:
                                                                                   Vk:
                 Duration left: -1
                                     Ready To Write: false
     Qk:
           A:
Load Buffers:
Load buffer position0:
Tag: L1 Busy: 0 Effective Address: -1 Start Cycle: -1 Execute End Cycle: -1 Duration left:
-1
      Ready To Write: false
Load buffer position1:
Tag: L2 Busy: 0 Effective Address: -1 Start Cycle: -1 Execute End Cycle: -1 Duration left:
-1
      Ready To Write: false
Load buffer position2:
Tag: L3 Busy: 0 Effective Address: -1 Start Cycle: -1 Execute End Cycle: -1 Duration left:
-1
      Ready To Write: false
```

Store buffer position0:

Tag: S1 Busy: 0 Effective Address: -1 Start Cycle: -1 Execute End Cycle: -1 Duration left:
-1 Ready To Write: false

Store buffer position1:

Store Buffers:

```
Tag: S2 Busy: 0 Effective Address: -1 Start Cycle: -1 Execute End Cycle: -1 Duration left:
      Ready To Write: false
-1
Store buffer position2:
Tag: S3 Busy: 0 Effective Address: -1 Start Cycle: -1 Execute End Cycle: -1 Duration left:
-1
      Ready To Write: false
Register File:
R0: Tag:
             Busy: 0 Value: 2.0
R1: Tag:
             Busy: 0 Value: 0.0
             Busy: 0 Value: 3.0
R2: Tag:
             Busy: 0 Value: 0.0
R3: Tag:
             Busy: 0 Value: 1.0
R4: Tag:
R5: Tag:
             Busy: 0 Value: 0.0
R6: Tag:
             Busy: 0 Value: 0.0
R7: Tag:
             Busy: 0 Value: 0.0
R8: Tag:
             Busy: 0 Value: 0.0
R9: Tag:
             Busy: 0 Value: 0.0
R10: Tag:
             Busy: 0 Value: 0.0
             Busy: 0 Value: 0.0
R11: Tag:
R12: Tag:
             Busy: 0 Value: 198.0
R13: Tag:
             Busy: 0 Value: 99.0
             Busy: 0 Value: 0.0
R14: Tag:
             Busy: 0 Value: 0.0
R15: Tag:
R16: Tag:
             Busy: 0 Value: 0.0
R17: Tag:
             Busy: 0 Value: 0.0
R18: Tag:
             Busy: 0 Value: 0.0
R19: Tag:
             Busy: 0 Value: 0.0
Memory:
M0: 0.0
M1: 198.0
M2: 2.0
M3: 0.0
M4: 0.0
M5: 0.0
M6: 0.0
Common Data Bus:
```

Tag: A1 Value: 99.0 Instructions To Write: Stall Branch: false

Stall: false

\_\_\_\_\_

Input: LD F0 2 MUL F4 F0 F2 SD F4 0 SUBI R15 R15 8 ADDI R16 R16 1 DIV R18 R16 R15 Result: end is 6

stall is now false : false Issue cycle of LD F0 2 is 1

Clock Cycle: 1 PC Value: 1

**Reservation Stations:** 

Adder:

Adder position0: Tag: A1 Start Cycle: -1 Execute End Cycle: -1 Busy: 0 Instruction Type: None Vj: Duration left: -1 Ready To Write: false Vk: Qk: A: Qi: Adder position1: Tag: A2 Start Cycle: -1 Execute End Cycle: -1 Busy: 0 Instruction Type: None Vj: Qk: A: Duration left: -1 Ready To Write: false Vk: Qj: Multiplier:

Multiplier position0:

Tag: M1 Start Cycle: -1 Execute End Cycle: -1 Busy: 0 Instruction Type: None Vj: Vk:

Qj: Qk: A: Duration left: -1 Ready To Write: false

Multiplier position1:

Tag: M2 Start Cycle: -1 Execute End Cycle: -1 Busy: 0 Instruction Type: None Vj: Vk:

Qj: Qk: A: Duration left: -1 Ready To Write: false

Load Buffers:

Load buffer position0:

Tag: L1 Busy: 1 Effective Address: 2 Start Cycle: -1 Execute End Cycle: -1 Duration left: 1

Ready To Write: false Load buffer position1:

Tag: L2 Busy: 0 Effective Address: -1 Start Cycle: -1 Execute End Cycle: -1 Duration left:

-1 Ready To Write: false

Store Buffers:

Store buffer position0:

Tag: S1 Busy: 0 Effective Address: -1 Start Cycle: -1 Execute End Cycle: -1 Duration left:

-1 Ready To Write: false

Store buffer position1:

Tag: S2 Busy: 0 Effective Address: -1 Start Cycle: -1 Execute End Cycle: -1 Duration left:

-1 Ready To Write: false

Register File:

R0: Tag: L1 Busy: 1 Value: -1.0 Busy: 0 Value: -1.0 R1: Tag: R2: Tag: Busy: 0 Value: 5.3 Busy: 0 Value: -1.0 R3: Tag: R4: Tag: Busy: 0 Value: -1.0 Busy: 0 Value: -1.0 R5: Tag: R6: Tag: Busy: 0 Value: -1.0 R7: Tag: Busy: 0 Value: -1.0 R8: Tag: Busy: 0 Value: -1.0 R9: Tag: Busy: 0 Value: -1.0

R10: Tag: Busy: 0 Value: -1.0 R11: Tag: Busy: 0 Value: -1.0

R12: Tag: Busy: 0 Value: -1.0

```
R13: Tag:
             Busy: 0 Value: -1.0
R14: Tag:
             Busy: 0 Value: -1.0
             Busy: 0 Value: 9.0
R15: Tag:
             Busy: 0 Value: 10.0
R16: Tag:
             Busy: 0 Value: -1.0
R17: Tag:
             Busy: 0 Value: -1.0
R18: Tag:
R19: Tag:
             Busy: 0 Value: -1.0
Memory:
M0: 0.0
M1: 0.0
M2: 2.0
M3: 0.0
M4: 0.0
M5: 0.0
M6: 0.0
Common Data Bus:
Tag: Value:
Current Instruction in PC: MUL F4 F0 F2
Instructions To Write:
stall is now false: false
Issue cycle of MUL F4 F0 F2 is 2
Clock Cycle: 2
PC Value: 2
Reservation Stations:
Adder:
Adder position0: Tag: A1
                            Start Cycle: -1 Execute End Cycle: -1 Busy: 0 Instruction
                                          Duration left: -1 Ready To Write: false
Type: None Vj: Vk: Qj:
                              Qk:
                                    A:
Adder position1: Tag: A2
                            Start Cycle: -1 Execute End Cycle: -1 Busy: 0 Instruction
Type: None Vj:
                                          Duration left: -1 Ready To Write: false
                Vk:
                        Qj:
                              Qk: A:
Multiplier:
Multiplier position0:
Tag: M1 Start Cycle: -1 Execute End Cycle: -1 Busy: 1 Instruction Type: MUL Vj:
                                                                                   Vk: 5.3
Qj: L1 Qk:
             A:
                   Duration left: 3
                                      Ready To Write: false
Multiplier position1:
Tag: M2 Start Cycle: -1 Execute End Cycle: -1 Busy: 0 Instruction Type: None Vj:
                                                                                   Vk:
     Qk: A:
                 Duration left: -1
                                     Ready To Write: false
Qi:
Load Buffers:
Load buffer position0:
Tag: L1 Busy: 1 Effective Address: 2
                                     Start Cycle: 2 Execute End Cycle: 3 Duration left: 1
Ready To Write: false
Load buffer position1:
Tag: L2 Busy: 0 Effective Address: -1 Start Cycle: -1 Execute End Cycle: -1 Duration left:
-1
      Ready To Write: false
Store Buffers:
```

Tag: S1 Busy: 0 Effective Address: -1 Start Cycle: -1 Execute End Cycle: -1 Duration left:

Store buffer position0:

Ready To Write: false

-1

Store buffer position1: Tag: S2 Busy: 0 Effective Address: -1 Start Cycle: -1 Execute End Cycle: -1 Duration left: Ready To Write: false -1 Register File: R0: Tag: L1 Busy: 1 Value: -1.0 Busy: 0 Value: -1.0 R1: Tag: R2: Tag: Busy: 0 Value: 5.3 R3: Tag: Busy: 0 Value: -1.0 R4: Tag: M1 Busy: 1 Value: -1.0 Busy: 0 Value: -1.0 R5: Tag: R6: Tag: Busy: 0 Value: -1.0 Busy: 0 Value: -1.0 R7: Tag: R8: Tag: Busy: 0 Value: -1.0 R9: Tag: Busy: 0 Value: -1.0 Busy: 0 Value: -1.0 R10: Tag: R11: Tag: Busy: 0 Value: -1.0 R12: Tag: Busy: 0 Value: -1.0 R13: Tag: Busy: 0 Value: -1.0 Busy: 0 Value: -1.0 R14: Tag: Busy: 0 Value: 9.0 R15: Tag: R16: Tag: Busy: 0 Value: 10.0 R17: Tag: Busy: 0 Value: -1.0 R18: Tag: Busy: 0 Value: -1.0 R19: Tag: Busy: 0 Value: -1.0 Memory: M0: 0.0 M1: 0.0 M2: 2.0 M3: 0.0 M4: 0.0 M5: 0.0 M6: 0.0 Common Data Bus: Tag: Value: Current Instruction in PC: SD F4 0 Instructions To Write: stall is now false : false Issue cycle of SD F4 0 is 3 Made load read to write Clock Cycle: 3 PC Value: 3 **Reservation Stations:** Adder: Adder position0: Tag: A1 Start Cycle: -1 Execute End Cycle: -1 Busy: 0 Instruction Type: None Vi: Duration left: -1 Ready To Write: false Vk: Qj: Qk: A: Start Cycle: -1 Execute End Cycle: -1 Busy: 0 Instruction Adder position1: Tag: A2

Duration left: -1 Ready To Write: false

Type: None Vj: Vk:

Qj:

Qk: A:

```
Multiplier:
Multiplier position0:
Tag: M1 Start Cycle: -1 Execute End Cycle: -1 Busy: 1 Instruction Type: MUL Vj:
                                                                                    Vk: 5.3
                                       Ready To Write: false
Qj: L1 Qk:
                   Duration left: 3
            A:
Multiplier position1:
Tag: M2 Start Cycle: -1 Execute End Cycle: -1 Busy: 0 Instruction Type: None Vi:
                                                                                     Vk:
                  Duration left: -1
                                      Ready To Write: false
           A:
Load Buffers:
Load buffer position0:
Tag: L1 Busy: 1 Effective Address: 2
                                      Start Cycle: 2 Execute End Cycle: 3 Duration left: 1
Ready To Write: true
Load buffer position1:
Tag: L2 Busy: 0 Effective Address: -1 Start Cycle: -1 Execute End Cycle: -1 Duration left:
-1
      Ready To Write: false
Store Buffers:
Store buffer position0:
Tag: S1 Busy: 1 Effective Address: 0
                                      Start Cycle: -1 Execute End Cycle: -1 Duration left:
      Ready To Write: false
Store buffer position1:
Tag: S2 Busy: 0 Effective Address: -1 Start Cycle: -1 Execute End Cycle: -1 Duration left:
      Ready To Write: false
Register File:
R0: Tag: L1
              Busy: 1 Value: -1.0
R1: Tag:
             Busy: 0 Value: -1.0
R2: Tag:
             Busy: 0 Value: 5.3
             Busy: 0 Value: -1.0
R3: Tag:
R4: Tag: M1
               Busy: 1 Value: -1.0
R5: Tag:
             Busy: 0 Value: -1.0
R6: Tag:
             Busy: 0 Value: -1.0
             Busy: 0 Value: -1.0
R7: Tag:
R8: Tag:
             Busy: 0 Value: -1.0
             Busy: 0 Value: -1.0
R9: Tag:
R10: Tag:
             Busy: 0 Value: -1.0
R11: Tag:
             Busy: 0 Value: -1.0
R12: Tag:
             Busy: 0 Value: -1.0
R13: Tag:
             Busy: 0 Value: -1.0
             Busy: 0 Value: -1.0
R14: Tag:
R15: Tag:
             Busy: 0 Value: 9.0
             Busy: 0 Value: 10.0
R16: Tag:
R17: Tag:
             Busy: 0 Value: -1.0
             Busy: 0 Value: -1.0
R18: Tag:
R19: Tag:
             Busy: 0 Value: -1.0
Memory:
M0: 0.0
M1: 0.0
```

M2: 2.0 M3: 0.0 M4: 0.0 M5: 0.0 M6: 0.0

Common Data Bus:

Tag: Value:

Current Instruction in PC: SUBI R15 R15 8

Instructions To Write:

LD F0 2

\_\_\_\_\_

stall is now false: false

Issue cycle of SUBI R15 R15 8 is 4

Value of memory is: 2.0 and effective address is: 2

Instruction to be written: LD F0 2

Clock Cycle: 4 PC Value: 4

**Reservation Stations:** 

Adder:

Adder position0: Tag: A1 Start Cycle: -1 Execute End Cycle: -1 Busy: 1 Instruction Type: SUBI Vj: 9.0 Vk: 8 Qj: Qk: A: Duration left: 1 Ready To Write: false Adder position1: Tag: A2 Start Cycle: -1 Execute End Cycle: -1 Busy: 0 Instruction Type: None Vj: Vk: Qj: Qk: A: Duration left: -1 Ready To Write: false Multiplier:

Multiplier position0:

Tag: M1 Start Cycle: -1 Execute End Cycle: -1 Busy: 1 Instruction Type: MUL Vj: 2.0 Vk:

5.3 Qi: Qk: A: Duration left: 3 Ready To Write: false

Multiplier position1:

Tag: M2 Start Cycle: -1 Execute End Cycle: -1 Busy: 0 Instruction Type: None Vj: Vk:

Qj: Qk: A: Duration left: -1 Ready To Write: false

Load Buffers:

Load buffer position0:

Tag: L1 Busy: 0 Effective Address: -1 Start Cycle: -1 Execute End Cycle: -1 Duration left:

-1 Ready To Write: false

Load buffer position1:

Tag: L2 Busy: 0 Effective Address: -1 Start Cycle: -1 Execute End Cycle: -1 Duration left:

-1 Ready To Write: false

Store Buffers:

Store buffer position0:

Tag: S1 Busy: 1 Effective Address: 0 Start Cycle: -1 Execute End Cycle: -1 Duration left:

1 Ready To Write: false

Store buffer position1:

Tag: S2 Busy: 0 Effective Address: -1 Start Cycle: -1 Execute End Cycle: -1 Duration left:

-1 Ready To Write: false

Register File:

R0: Tag: Busy: 0 Value: 2.0
R1: Tag: Busy: 0 Value: -1.0
R2: Tag: Busy: 0 Value: 5.3
R3: Tag: Busy: 0 Value: -1.0
R4: Tag: M1 Busy: 1 Value: -1.0
R5: Tag: Busy: 0 Value: -1.0

```
R6: Tag:
             Busy: 0 Value: -1.0
R7: Tag:
             Busy: 0 Value: -1.0
             Busy: 0 Value: -1.0
R8: Tag:
             Busy: 0 Value: -1.0
R9: Tag:
             Busy: 0 Value: -1.0
R10: Tag:
R11: Tag:
             Busy: 0 Value: -1.0
R12: Tag:
             Busy: 0 Value: -1.0
R13: Tag:
             Busy: 0 Value: -1.0
R14: Tag:
             Busy: 0 Value: -1.0
R15: Tag: A1
               Busy: 1 Value: 9.0
R16: Tag:
             Busy: 0 Value: 10.0
             Busy: 0 Value: -1.0
R17: Tag:
R18: Tag:
             Busy: 0 Value: -1.0
R19: Tag:
             Busy: 0 Value: -1.0
Memory:
M0: 0.0
M1: 0.0
M2: 2.0
M3: 0.0
M4: 0.0
M5: 0.0
M6: 0.0
Common Data Bus:
Tag: L1 Value: 2.0
Current Instruction in PC: ADDI R16 R16 1
Instructions To Write:
stall is now false : false
Issue cycle of ADDI R16 R16 1 is 5
CAN EXECUTE MULTIPLY MUL F4 F0 F2
Clock Cycle: 5
PC Value: 5
Reservation Stations:
Adder:
Adder position0: Tag: A1
                             Start Cycle: 5 Execute End Cycle: 6 Busy: 1 Instruction
Type: SUBI Vj: 9.0 Vk: 8 Qj:
                                                             Ready To Write: false
                                Qk:
                                      A:
                                            Duration left: 1
Adder position1: Tag: A2
                             Start Cycle: -1 Execute End Cycle: -1 Busy: 1 Instruction
Type: ADDI Vj: 10.0
                        Vk: 1 Qj:
                                     Qk:
                                            A: Duration left: 1 Ready To Write: false
Multiplier:
Multiplier position0:
Tag: M1 Start Cycle: 5 Execute End Cycle: 8 Busy: 1 Instruction Type: MUL Vj: 2.0 Vk:
                                         Ready To Write: false
5.3 Qi:
         Qk:
                A:
                     Duration left: 3
Multiplier position1:
Tag: M2 Start Cycle: -1 Execute End Cycle: -1 Busy: 0 Instruction Type: None Vj:
                  Duration left: -1
                                     Ready To Write: false
Qj:
     Qk:
            A:
Load Buffers:
Load buffer position0:
```

```
Tag: L1 Busy: 0 Effective Address: -1 Start Cycle: -1 Execute End Cycle: -1 Duration left:
-1
      Ready To Write: false
Load buffer position1:
Tag: L2 Busy: 0 Effective Address: -1 Start Cycle: -1 Execute End Cycle: -1 Duration left:
-1
      Ready To Write: false
Store Buffers:
Store buffer position0:
Tag: S1 Busy: 1 Effective Address: 0 Start Cycle: -1 Execute End Cycle: -1 Duration left:
      Ready To Write: false
Store buffer position1:
Tag: S2 Busy: 0 Effective Address: -1 Start Cycle: -1 Execute End Cycle: -1 Duration left:
      Ready To Write: false
Register File:
R0: Tag:
             Busy: 0 Value: 2.0
             Busy: 0 Value: -1.0
R1: Tag:
R2: Tag:
             Busy: 0 Value: 5.3
R3: Tag:
             Busy: 0 Value: -1.0
R4: Tag: M1
              Busy: 1 Value: -1.0
             Busy: 0 Value: -1.0
R5: Tag:
             Busy: 0 Value: -1.0
R6: Tag:
R7: Tag:
             Busy: 0 Value: -1.0
R8: Tag:
             Busy: 0 Value: -1.0
R9: Tag:
             Busy: 0 Value: -1.0
R10: Tag:
             Busy: 0 Value: -1.0
R11: Tag:
             Busy: 0 Value: -1.0
R12: Tag:
             Busy: 0 Value: -1.0
             Busy: 0 Value: -1.0
R13: Tag:
             Busy: 0 Value: -1.0
R14: Tag:
R15: Tag: A1
               Busy: 1 Value: 9.0
R16: Tag: A2 Busy: 1 Value: 10.0
R17: Tag:
             Busy: 0 Value: -1.0
             Busy: 0 Value: -1.0
R18: Tag:
             Busy: 0 Value: -1.0
R19: Tag:
Memory:
M0: 0.0
M1: 0.0
M2: 2.0
M3: 0.0
M4: 0.0
M5: 0.0
M6: 0.0
Common Data Bus:
Tag: L1 Value: 2.0
Current Instruction in PC: DIV R18 R16 R15
Instructions To Write:
```

\_\_\_\_\_

stall is now false : false

Issue cycle of DIV R18 R16 R15 is 6

Clock Cycle: 6 PC Value: 6

**Reservation Stations:** 

Adder:

Adder position0: Tag: A1 Start Cycle: 5 Execute End Cycle: 6 Busy: 1 Instruction Type: SUBI Vj: 9.0 Vk: 8 Qj: Qk: A: Duration left: 1 Ready To Write: true Adder position1: Tag: A2 Start Cycle: 6 Execute End Cycle: 7 Busy: 1 Instruction Type: ADDI Vj: 10.0 Vk: 1 Qj: Qk: A: Duration left: 1 Ready To Write: false Multiplier:

Multiplier position0:

Tag: M1 Start Cycle: 5 Execute End Cycle: 8 Busy: 1 Instruction Type: MUL Vj: 2.0 Vk:

5.3 Qj: Qk: A: Duration left: 2 Ready To Write: false

Multiplier position1:

Tag: M2 Start Cycle: -1 Execute End Cycle: -1 Busy: 1 Instruction Type: DIV Vj: Vk:

Qj: A2 Qk: A1 A: Duration left: 3 Ready To Write: false

Load Buffers:

Load buffer position0:

Tag: L1 Busy: 0 Effective Address: -1 Start Cycle: -1 Execute End Cycle: -1 Duration left:

-1 Ready To Write: false

Load buffer position1:

Tag: L2 Busy: 0 Effective Address: -1 Start Cycle: -1 Execute End Cycle: -1 Duration left:

-1 Ready To Write: false

Store Buffers:

Store buffer position0:

Tag: S1 Busy: 1 Effective Address: 0 Start Cycle: -1 Execute End Cycle: -1 Duration left:

1 Ready To Write: false

Store buffer position1:

Tag: S2 Busy: 0 Effective Address: -1 Start Cycle: -1 Execute End Cycle: -1 Duration left:

-1 Ready To Write: false

Register File:

R0: Tag: Busy: 0 Value: 2.0 R1: Tag: Busy: 0 Value: -1.0 R2: Tag: Busy: 0 Value: 5.3 R3: Tag: Busy: 0 Value: -1.0 R4: Tag: M1 Busy: 1 Value: -1.0 R5: Tag: Busy: 0 Value: -1.0 Busy: 0 Value: -1.0 R6: Tag: R7: Tag: Busy: 0 Value: -1.0 Busy: 0 Value: -1.0 R8: Tag: R9: Tag: Busy: 0 Value: -1.0 Busy: 0 Value: -1.0 R10: Tag: R11: Tag: Busy: 0 Value: -1.0 R12: Tag: Busy: 0 Value: -1.0 R13: Tag: Busy: 0 Value: -1.0 R14: Tag: Busy: 0 Value: -1.0 Busy: 1 Value: 9.0

R15: Tag: A1 Busy: 1 Value: 9.0 R16: Tag: A2 Busy: 1 Value: 10.0

R17: Tag: Busy: 0 Value: -1.0

```
R18: Tag: M2 Busy: 1 Value: -1.0
             Busy: 0 Value: -1.0
R19: Tag:
Memory:
M0: 0.0
M1: 0.0
M2: 2.0
M3: 0.0
M4: 0.0
M5: 0.0
M6: 0.0
Common Data Bus:
Tag: L1 Value: 2.0
Instructions To Write:
SUBI R15 R15 8
Instruction to be written: SUBI R15 R15 8
Clock Cycle: 7
PC Value: 6
Reservation Stations:
Adder:
Adder position0: Tag: A1
                            Start Cycle: -1 Execute End Cycle: -1 Busy: 0 Instruction
                                          Duration left: -1 Ready To Write: false
Type: None Vi: Vk: Qi:
                             Qk:
                                    A:
Adder position1: Tag: A2
                            Start Cycle: 6 Execute End Cycle: 7 Busy: 1 Instruction
Type: ADDI Vi: 10.0
                        Vk: 1 Qi:
                                     Qk: A: Duration left: 1 Ready To Write: true
Multiplier:
Multiplier position0:
Tag: M1 Start Cycle: 5 Execute End Cycle: 8 Busy: 1 Instruction Type: MUL Vj: 2.0 Vk:
                                        Ready To Write: true
5.3 Qj:
         Qk:
                     Duration left: 1
               A:
Multiplier position1:
Tag: M2 Start Cycle: -1 Execute End Cycle: -1 Busy: 1 Instruction Type: DIV Vj: Vk: 1.0
            A:
Qj: A2 Qk:
                   Duration left: 3
                                      Ready To Write: false
Load Buffers:
Load buffer position0:
Tag: L1 Busy: 0 Effective Address: -1 Start Cycle: -1 Execute End Cycle: -1 Duration left:
      Ready To Write: false
Load buffer position1:
Tag: L2 Busy: 0 Effective Address: -1 Start Cycle: -1 Execute End Cycle: -1 Duration left:
      Ready To Write: false
Store Buffers:
```

Store buffer position0:

Tag: S1 Busy: 1 Effective Address: 0 Start Cycle: -1 Execute End Cycle: -1 Duration left:

1 Ready To Write: false

Store buffer position1:

Tag: S2 Busy: 0 Effective Address: -1 Start Cycle: -1 Execute End Cycle: -1 Duration left:

-1 Ready To Write: false

Register File:

Busy: 0 Value: 2.0 R0: Tag: Busy: 0 Value: -1.0 R1: Tag:

```
R2: Tag:
             Busy: 0 Value: 5.3
R3: Tag:
             Busy: 0 Value: -1.0
              Busy: 1 Value: -1.0
R4: Tag: M1
             Busy: 0 Value: -1.0
R5: Tag:
             Busy: 0 Value: -1.0
R6: Tag:
R7: Tag:
             Busy: 0 Value: -1.0
R8: Tag:
             Busy: 0 Value: -1.0
R9: Tag:
             Busy: 0 Value: -1.0
R10: Tag:
             Busy: 0 Value: -1.0
R11: Tag:
             Busy: 0 Value: -1.0
R12: Tag:
             Busy: 0 Value: -1.0
R13: Tag:
             Busy: 0 Value: -1.0
R14: Tag:
             Busy: 0 Value: -1.0
R15: Tag:
             Busy: 0 Value: 1.0
R16: Tag: A2 Busy: 1 Value: 10.0
R17: Tag:
             Busy: 0 Value: -1.0
R18: Tag: M2 Busy: 1 Value: -1.0
R19: Tag:
             Busy: 0 Value: -1.0
Memory:
M0: 0.0
M1: 0.0
M2: 2.0
M3: 0.0
M4: 0.0
M5: 0.0
M6: 0.0
Common Data Bus:
Tag: A1 Value: 1.0
Instructions To Write:
MUL F4 F0 F2
ADDI R16 R16 1
Instruction to be written: MUL F4 F0 F2
Clock Cycle: 8
PC Value: 6
Reservation Stations:
Adder:
Adder position0: Tag: A1
                            Start Cycle: -1 Execute End Cycle: -1 Busy: 0 Instruction
Type: None Vi:
                                    A:
                                          Duration left: -1 Ready To Write: false
                 Vk:
                        Qi:
                              Qk:
Adder position1: Tag: A2
                             Start Cycle: 6 Execute End Cycle: 7 Busy: 1 Instruction
```

Type: ADDI Vj: 10.0

Multiplier:
Multiplier position0:
Tag: M1 Start Cycle: -1 Execute End Cycle: -1 Busy: 0 Instruction Type: None Vj: Vk: Qj: Qk: A: Duration left: -1 Ready To Write: false
Multiplier position1:
Tag: M2 Start Cycle: -1 Execute End Cycle: -1 Busy: 1 Instruction Type: DIV Vi: Vk: 1

Qk:

Vk: 1 Qj:

A: Duration left: 1 Ready To Write: true

Tag: M2 Start Cycle: -1 Execute End Cycle: -1 Busy: 1 Instruction Type: DIV Vj: Vk: 1.0 Qj: A2 Qk: A: Duration left: 3 Ready To Write: false

```
Load buffer position0:
Tag: L1 Busy: 0 Effective Address: -1 Start Cycle: -1 Execute End Cycle: -1 Duration left:
-1
      Ready To Write: false
Load buffer position1:
Tag: L2 Busy: 0 Effective Address: -1 Start Cycle: -1 Execute End Cycle: -1 Duration left:
      Ready To Write: false
Store Buffers:
Store buffer position0:
                                      Start Cycle: -1 Execute End Cycle: -1 Duration left:
Tag: S1 Busy: 1 Effective Address: 0
      Ready To Write: false
Store buffer position1:
Tag: S2 Busy: 0 Effective Address: -1 Start Cycle: -1 Execute End Cycle: -1 Duration left:
-1
      Ready To Write: false
Register File:
R0: Tag:
             Busy: 0 Value: 2.0
R1: Tag:
             Busy: 0 Value: -1.0
             Busy: 0 Value: 5.3
R2: Tag:
R3: Tag:
             Busy: 0 Value: -1.0
R4: Tag:
             Busy: 0 Value: 10.600000381469727
             Busy: 0 Value: -1.0
R5: Tag:
             Busy: 0 Value: -1.0
R6: Tag:
R7: Tag:
             Busy: 0 Value: -1.0
R8: Tag:
             Busy: 0 Value: -1.0
R9: Tag:
             Busy: 0 Value: -1.0
R10: Tag:
             Busy: 0 Value: -1.0
R11: Tag:
             Busy: 0 Value: -1.0
R12: Tag:
             Busy: 0 Value: -1.0
R13: Tag:
             Busy: 0 Value: -1.0
             Busy: 0 Value: -1.0
R14: Tag:
R15: Tag:
             Busy: 0 Value: 1.0
R16: Tag: A2 Busy: 1 Value: 10.0
R17: Tag:
             Busy: 0 Value: -1.0
R18: Tag: M2 Busy: 1 Value: -1.0
R19: Tag:
             Busy: 0 Value: -1.0
Memory:
M0: 0.0
M1: 0.0
M2: 2.0
M3: 0.0
M4: 0.0
M5: 0.0
M6: 0.0
Common Data Bus:
Tag: M1 Value: 10.6
Instructions To Write:
```

\_\_\_\_\_

ADDI R16 R16 1

Load Buffers:

Instruction to be written: ADDI R16 R16 1

Clock Cycle: 9 PC Value: 6

**Reservation Stations:** 

Adder:

Adder position0: Tag: A1 Start Cycle: -1 Execute End Cycle: -1 Busy: 0 Instruction Type: None Vj: Vk: Qj: Qk: A: Duration left: -1 Ready To Write: false Adder position1: Tag: A2 Start Cycle: -1 Execute End Cycle: -1 Busy: 0 Instruction Type: None Vj: Vk: Qj: Qk: A: Duration left: -1 Ready To Write: false

Multiplier:

Multiplier position0:

Tag: M1 Start Cycle: -1 Execute End Cycle: -1 Busy: 0 Instruction Type: None Vj: Vk:

Qj: Qk: A: Duration left: -1 Ready To Write: false

Multiplier position1:

Tag: M2 Start Cycle: -1 Execute End Cycle: -1 Busy: 1 Instruction Type: DIV Vj: 11.0

Vk: 1.0 Qj: Qk: A: Duration left: 3 Ready To Write: false

Load Buffers:

Load buffer position0:

Tag: L1 Busy: 0 Effective Address: -1 Start Cycle: -1 Execute End Cycle: -1 Duration left:

-1 Ready To Write: false

Load buffer position1:

Tag: L2 Busy: 0 Effective Address: -1 Start Cycle: -1 Execute End Cycle: -1 Duration left:

-1 Ready To Write: false

Store Buffers:

Store buffer position0:

Tag: S1 Busy: 1 Effective Address: 0 Start Cycle: 9 Execute End Cycle: 10 Duration left:

1 Ready To Write: false

Store buffer position1:

Tag: S2 Busy: 0 Effective Address: -1 Start Cycle: -1 Execute End Cycle: -1 Duration left:

-1 Ready To Write: false

Register File:

R0: Tag: Busy: 0 Value: 2.0 R1: Tag: Busy: 0 Value: -1.0 R2: Tag: Busy: 0 Value: 5.3 R3: Tag: Busy: 0 Value: -1.0

R4: Tag: Busy: 0 Value: 10.600000381469727

R5: Tag: Busy: 0 Value: -1.0
R6: Tag: Busy: 0 Value: -1.0
R7: Tag: Busy: 0 Value: -1.0
R8: Tag: Busy: 0 Value: -1.0
R9: Tag: Busy: 0 Value: -1.0
R9: Tag: Busy: 0 Value: -1.0
R10: Tag: Busy: 0 Value: -1.0
R11: Tag: Busy: 0 Value: -1.0

R12: Tag: Busy: 0 Value: -1.0 R13: Tag: Busy: 0 Value: -1.0

R14: Tag: Busy: 0 Value: -1.0 R15: Tag: Busy: 0 Value: 1.0

R16: Tag: Busy: 0 Value: 11.0

```
R17: Tag: Busy: 0 Value: -1.0
R18: Tag: M2 Busy: 1 Value: -1.0
R19: Tag: Busy: 0 Value: -1.0
```

Memory: M0: 0.0 M1: 0.0 M2: 2.0 M3: 0.0 M4: 0.0 M5: 0.0 M6: 0.0

Common Data Bus: Tag: A2 Value: 11.0 Instructions To Write:

-----

CAN EXECUTE MULTIPLY DIV R18 R16 R15

Clock Cycle: 10 PC Value: 6

Reservation Stations:

Adder:

Adder position0: Tag: A1 Start Cycle: -1 Execute End Cycle: -1 Busy: 0 Instruction Type: None Vj: Vk: Qj: Qk: A: Duration left: -1 Ready To Write: false Adder position1: Tag: A2 Start Cycle: -1 Execute End Cycle: -1 Busy: 0 Instruction Type: None Vj: Vk: Qj: Qk: A: Duration left: -1 Ready To Write: false Multiplier:

Multiplier position0:

Tag: M1 Start Cycle: -1 Execute End Cycle: -1 Busy: 0 Instruction Type: None Vj: Vk:

Qj: Qk: A: Duration left: -1 Ready To Write: false

Multiplier position1:

Tag: M2 Start Cycle: 10 Execute End Cycle: 13 Busy: 1 Instruction Type: DIV Vj: 11.0

Vk: 1.0 Qj: Qk: A: Duration left: 3 Ready To Write: false

Load Buffers:

Load buffer position0:

Tag: L1 Busy: 0 Effective Address: -1 Start Cycle: -1 Execute End Cycle: -1 Duration left:

-1 Ready To Write: false

Load buffer position1:

Tag: L2 Busy: 0 Effective Address: -1 Start Cycle: -1 Execute End Cycle: -1 Duration left:

-1 Ready To Write: false

Store Buffers:

Store buffer position0:

Tag: S1 Busy: 0 Effective Address: -1 Start Cycle: -1 Execute End Cycle: -1 Duration left:

-1 Ready To Write: false

Store buffer position1:

Tag: S2 Busy: 0 Effective Address: -1 Start Cycle: -1 Execute End Cycle: -1 Duration left:

-1 Ready To Write: false

Register File:

R0: Tag: Busy: 0 Value: 2.0 R1: Tag: Busy: 0 Value: -1.0

```
R2: Tag:
             Busy: 0 Value: 5.3
R3: Tag:
             Busy: 0 Value: -1.0
             Busy: 0 Value: 10.600000381469727
R4: Tag:
             Busy: 0 Value: -1.0
R5: Tag:
             Busy: 0 Value: -1.0
R6: Tag:
R7: Tag:
             Busy: 0 Value: -1.0
R8: Tag:
             Busy: 0 Value: -1.0
R9: Tag:
             Busy: 0 Value: -1.0
R10: Tag:
             Busy: 0 Value: -1.0
R11: Tag:
             Busy: 0 Value: -1.0
R12: Tag:
             Busy: 0 Value: -1.0
             Busy: 0 Value: -1.0
R13: Tag:
R14: Tag:
             Busy: 0 Value: -1.0
R15: Tag:
             Busy: 0 Value: 1.0
             Busy: 0 Value: 11.0
R16: Tag:
R17: Tag:
             Busy: 0 Value: -1.0
R18: Tag: M2 Busy: 1 Value: -1.0
R19: Tag:
             Busy: 0 Value: -1.0
Memory:
M0: 10.600000381469727
M1: 0.0
M2: 2.0
M3: 0.0
M4: 0.0
M5: 0.0
M6: 0.0
Common Data Bus:
Tag: A2 Value: 11.0
Instructions To Write:
Clock Cycle: 11
PC Value: 6
Reservation Stations:
Adder:
Adder position0: Tag: A1
                            Start Cycle: -1 Execute End Cycle: -1 Busy: 0 Instruction
                                          Duration left: -1 Ready To Write: false
Type: None Vi:
                 Vk: Qi:
                              Qk:
                                    A:
Adder position1: Tag: A2
                            Start Cycle: -1 Execute End Cycle: -1 Busy: 0 Instruction
                                          Duration left: -1 Ready To Write: false
Type: None Vj: Vk:
                        Qj:
                              Qk: A:
Multiplier:
Multiplier position0:
Tag: M1 Start Cycle: -1 Execute End Cycle: -1 Busy: 0 Instruction Type: None Vj:
                                                                                   Vk:
Qj:
     Qk:
            A:
                 Duration left: -1
                                     Ready To Write: false
Multiplier position1:
Tag: M2 Start Cycle: 10 Execute End Cycle: 13 Busy: 1 Instruction Type: DIV Vj: 11.0
                         Duration left: 2 Ready To Write: false
Vk: 1.0 Qj:
             Qk:
                   A:
Load Buffers:
Load buffer position0:
```

```
Tag: L1 Busy: 0 Effective Address: -1 Start Cycle: -1 Execute End Cycle: -1 Duration left:
-1
      Ready To Write: false
Load buffer position1:
Tag: L2 Busy: 0 Effective Address: -1 Start Cycle: -1 Execute End Cycle: -1 Duration left:
-1
      Ready To Write: false
Store Buffers:
Store buffer position0:
Tag: S1 Busy: 0 Effective Address: -1 Start Cycle: -1 Execute End Cycle: -1 Duration left:
      Ready To Write: false
Store buffer position1:
Tag: S2 Busy: 0 Effective Address: -1 Start Cycle: -1 Execute End Cycle: -1 Duration left:
      Ready To Write: false
Register File:
R0: Tag:
             Busy: 0 Value: 2.0
             Busy: 0 Value: -1.0
R1: Tag:
R2: Tag:
             Busy: 0 Value: 5.3
R3: Tag:
             Busy: 0 Value: -1.0
             Busy: 0 Value: 10.600000381469727
R4: Tag:
             Busy: 0 Value: -1.0
R5: Tag:
             Busy: 0 Value: -1.0
R6: Tag:
R7: Tag:
             Busy: 0 Value: -1.0
R8: Tag:
             Busy: 0 Value: -1.0
R9: Tag:
             Busy: 0 Value: -1.0
R10: Tag: Busy: 0 Value: -1.0
R11: Tag:
             Busy: 0 Value: -1.0
R12: Tag:
             Busy: 0 Value: -1.0
             Busy: 0 Value: -1.0
R13: Tag:
             Busy: 0 Value: -1.0
R14: Tag:
R15: Tag:
             Busy: 0 Value: 1.0
             Busy: 0 Value: 11.0
R16: Tag:
R17: Tag:
             Busy: 0 Value: -1.0
R18: Tag: M2 Busy: 1 Value: -1.0
R19: Tag:
             Busy: 0 Value: -1.0
Memory:
M0: 10.600000381469727
M1: 0.0
M2: 2.0
M3: 0.0
M4: 0.0
M5: 0.0
M6: 0.0
Common Data Bus:
Tag: A2 Value: 11.0
Instructions To Write:
```

Clock Cycle: 12 PC Value: 6

**Reservation Stations:** 

```
Adder:
Adder position0: Tag: A1
                             Start Cycle: -1 Execute End Cycle: -1 Busy: 0 Instruction
                                          Duration left: -1 Ready To Write: false
Type: None Vj:
                  Vk:
                        Qj:
                              Qk:
                                    A:
Adder position1: Tag: A2
                             Start Cycle: -1 Execute End Cycle: -1 Busy: 0 Instruction
Type: None Vj:
                                          Duration left: -1 Ready To Write: false
                  Vk:
                              Qk:
                                    A:
                        Qj:
Multiplier:
Multiplier position0:
Tag: M1 Start Cycle: -1 Execute End Cycle: -1 Busy: 0 Instruction Type: None Vj:
     Qk:
           A:
                  Duration left: -1
                                     Ready To Write: false
Multiplier position1:
Tag: M2 Start Cycle: 10 Execute End Cycle: 13 Busy: 1 Instruction Type: DIV Vj: 11.0
Vk: 1.0 Qi: Qk: A:
                         Duration left: 1 Ready To Write: true
Load Buffers:
Load buffer position0:
Tag: L1 Busy: 0 Effective Address: -1 Start Cycle: -1 Execute End Cycle: -1 Duration left:
      Ready To Write: false
-1
Load buffer position1:
Tag: L2 Busy: 0 Effective Address: -1 Start Cycle: -1 Execute End Cycle: -1 Duration left:
-1
      Ready To Write: false
Store Buffers:
Store buffer position0:
Tag: S1 Busy: 0 Effective Address: -1 Start Cycle: -1 Execute End Cycle: -1 Duration left:
      Ready To Write: false
Store buffer position1:
Tag: S2 Busy: 0 Effective Address: -1 Start Cycle: -1 Execute End Cycle: -1 Duration left:
-1
      Ready To Write: false
Register File:
R0: Tag:
             Busy: 0 Value: 2.0
R1: Tag:
             Busy: 0 Value: -1.0
             Busy: 0 Value: 5.3
R2: Tag:
R3: Tag:
             Busy: 0 Value: -1.0
             Busy: 0 Value: 10.600000381469727
R4: Tag:
R5: Tag:
             Busy: 0 Value: -1.0
R6: Tag:
             Busy: 0 Value: -1.0
R7: Tag:
             Busy: 0 Value: -1.0
R8: Tag:
             Busy: 0 Value: -1.0
             Busy: 0 Value: -1.0
R9: Tag:
R10: Tag:
             Busy: 0 Value: -1.0
             Busy: 0 Value: -1.0
R11: Tag:
R12: Tag:
             Busy: 0 Value: -1.0
             Busy: 0 Value: -1.0
R13: Tag:
R14: Tag:
             Busy: 0 Value: -1.0
R15: Tag:
             Busy: 0 Value: 1.0
R16: Tag:
             Busy: 0 Value: 11.0
R17: Tag:
             Busy: 0 Value: -1.0
R18: Tag: M2 Busy: 1 Value: -1.0
```

Busy: 0 Value: -1.0

R19: Tag: Memory:

M0: 10.600000381469727 M1: 0.0

M2: 2.0 M3: 0.0 M4: 0.0

M5: 0.0 M6: 0.0

Common Data Bus: Tag: A2 Value: 11.0 Instructions To Write: DIV R18 R16 R15

\_\_\_\_\_

Instruction to be written: DIV R18 R16 R15

Clock Cycle: 13 PC Value: 6

**Reservation Stations:** 

Adder:

Adder position0: Tag: A1 Start Cycle: -1 Execute End Cycle: -1 Busy: 0 Instruction Type: None Vj: Vk: Qj: Qk: A: Duration left: -1 Ready To Write: false Adder position1: Tag: A2 Start Cycle: -1 Execute End Cycle: -1 Busy: 0 Instruction Type: None Vj: Vk: Qj: Qk: A: Duration left: -1 Ready To Write: false Multiplier:

Multiplier position0:

Tag: M1 Start Cycle: -1 Execute End Cycle: -1 Busy: 0 Instruction Type: None Vj: Vk:

Qj: Qk: A: Duration left: -1 Ready To Write: false

Multiplier position1:

Tag: M2 Start Cycle: -1 Execute End Cycle: -1 Busy: 0 Instruction Type: None Vj: Vk:

Qj: Qk: A: Duration left: -1 Ready To Write: false

Load Buffers:

Load buffer position0:

Tag: L1 Busy: 0 Effective Address: -1 Start Cycle: -1 Execute End Cycle: -1 Duration left:

-1 Ready To Write: false

Load buffer position1:

Tag: L2 Busy: 0 Effective Address: -1 Start Cycle: -1 Execute End Cycle: -1 Duration left:

-1 Ready To Write: false

Store Buffers:

Store buffer position0:

Tag: S1 Busy: 0 Effective Address: -1 Start Cycle: -1 Execute End Cycle: -1 Duration left:

-1 Ready To Write: false

Store buffer position1:

Tag: S2 Busy: 0 Effective Address: -1 Start Cycle: -1 Execute End Cycle: -1 Duration left:

-1 Ready To Write: false

Register File:

R0: Tag: Busy: 0 Value: 2.0 R1: Tag: Busy: 0 Value: -1.0 R2: Tag: Busy: 0 Value: 5.3 R3: Tag: Busy: 0 Value: -1.0

R4: Tag: Busy: 0 Value: 10.600000381469727

```
R5: Tag:
             Busy: 0 Value: -1.0
R6: Tag:
             Busy: 0 Value: -1.0
R7: Tag:
             Busy: 0 Value: -1.0
R8: Tag:
             Busy: 0 Value: -1.0
R9: Tag:
             Busy: 0 Value: -1.0
R10: Tag:
             Busy: 0 Value: -1.0
R11: Tag:
             Busy: 0 Value: -1.0
R12: Tag:
             Busy: 0 Value: -1.0
R13: Tag:
             Busy: 0 Value: -1.0
R14: Tag:
             Busy: 0 Value: -1.0
R15: Tag:
             Busy: 0 Value: 1.0
             Busy: 0 Value: 11.0
R16: Tag:
             Busy: 0 Value: -1.0
R17: Tag:
R18: Tag:
             Busy: 0 Value: 11.0
R19: Tag:
             Busy: 0 Value: -1.0
```

Memory:

M0: 10.600000381469727

M1: 0.0 M2: 2.0 M3: 0.0 M4: 0.0 M5: 0.0 M6: 0.0

Common Data Bus: Tag: M2 Value: 11.0 Instructions To Write:

-----

## Input:

LD R0, 1 LD R1, 2 MUL R0,R0,R20 MUL R1,R1,R20 ADD R2,R0,R1 ADD R20,R20,R20 SD R2,5

## Result:

stall is now false : false Issue cycle of LD R0, 1 is 1

Clock Cycle: 1 PC Value: 1

Reservation Stations:

```
Adder:
Adder position0: Tag: A1
                             Start Cycle: -1 Execute End Cycle: -1 Busy: 0 Instruction
                        Qj:
                                           Duration left: -1 Ready To Write: false
Type: None Vj:
                  Vk:
                              Qk:
                                     A:
Adder position1: Tag: A2
                             Start Cycle: -1 Execute End Cycle: -1 Busy: 0 Instruction
Type: None Vj:
                                           Duration left: -1 Ready To Write: false
                  Vk:
                              Qk:
                                     A:
                        Qj:
Multiplier:
Multiplier position0:
Tag: M1 Start Cycle: -1 Execute End Cycle: -1 Busy: 0 Instruction Type: None Vj:
                                                                                     Vk:
                  Duration left: -1
     Qk:
           A:
                                      Ready To Write: false
Multiplier position1:
Tag: M2 Start Cycle: -1 Execute End Cycle: -1 Busy: 0 Instruction Type: None Vj:
                                                                                     Vk:
           A:
                  Duration left: -1
                                      Ready To Write: false
     Qk:
Load Buffers:
Load buffer position0:
                                      Start Cycle: -1 Execute End Cycle: -1 Duration left: 1
Tag: L1 Busy: 1 Effective Address: 1
Ready To Write: false
Load buffer position1:
Tag: L2 Busy: 0 Effective Address: -1 Start Cycle: -1 Execute End Cycle: -1 Duration left:
-1
      Ready To Write: false
Store Buffers:
Store buffer position0:
Tag: S1 Busy: 0 Effective Address: -1 Start Cycle: -1 Execute End Cycle: -1 Duration left:
      Ready To Write: false
Store buffer position1:
Tag: S2 Busy: 0 Effective Address: -1 Start Cycle: -1 Execute End Cycle: -1 Duration left:
-1
      Ready To Write: false
Register File:
R0: Tag: L1
              Busy: 1 Value: -1.0
R1: Tag:
             Busy: 0 Value: -1.0
             Busy: 0 Value: -1.0
R2: Tag:
R3: Tag:
             Busy: 0 Value: -1.0
R4: Tag:
             Busy: 0 Value: -1.0
R5: Tag:
             Busy: 0 Value: -1.0
R6: Tag:
             Busy: 0 Value: -1.0
R7: Tag:
             Busy: 0 Value: -1.0
R8: Tag:
             Busy: 0 Value: -1.0
             Busy: 0 Value: -1.0
R9: Tag:
R10: Tag:
             Busy: 0 Value: -1.0
             Busy: 0 Value: -1.0
R11: Tag:
R12: Tag:
             Busy: 0 Value: -1.0
             Busy: 0 Value: -1.0
R13: Tag:
R14: Tag:
             Busy: 0 Value: -1.0
R15: Tag:
             Busy: 0 Value: -1.0
R16: Tag:
             Busy: 0 Value: -1.0
R17: Tag:
             Busy: 0 Value: -1.0
             Busy: 0 Value: -1.0
R18: Tag:
```

R19: Tag:

R20: Tag:

Busy: 0 Value: -1.0 Busy: 0 Value: 3.0

```
R21: Tag:
             Busy: 0 Value: -1.0
Memory:
M0: 0.0
M1: 1.0
M2: 2.0
M3: 0.0
M4: 0.0
M5: 0.0
M6: 0.0
Common Data Bus:
Tag: Value:
Current Instruction in PC: LD R1, 2
Instructions To Write:
stall is now false: false
Issue cycle of LD R1, 2 is 2
Clock Cycle: 2
PC Value: 2
Reservation Stations:
Adder:
Adder position0: Tag: A1
                             Start Cycle: -1 Execute End Cycle: -1 Busy: 0 Instruction
                                          Duration left: -1 Ready To Write: false
Type: None Vi: Vk:
                              Qk:
                                    A:
                        Qj:
Adder position1: Tag: A2
                             Start Cycle: -1 Execute End Cycle: -1 Busy: 0 Instruction
Type: None Vi:
                              Qk:
                                          Duration left: -1 Ready To Write: false
                Vk: Qj:
                                   A:
Multiplier:
Multiplier position0:
Tag: M1 Start Cycle: -1 Execute End Cycle: -1 Busy: 0 Instruction Type: None Vj:
                                                                                    Vk:
Qj:
     Qk:
            A:
                  Duration left: -1
                                     Ready To Write: false
Multiplier position1:
Tag: M2 Start Cycle: -1 Execute End Cycle: -1 Busy: 0 Instruction Type: None Vj:
                                                                                   Vk:
Qi:
     Qk:
           A:
                  Duration left: -1
                                     Ready To Write: false
Load Buffers:
Load buffer position0:
Tag: L1 Busy: 1 Effective Address: 1
                                      Start Cycle: 2 Execute End Cycle: 3 Duration left: 1
Ready To Write: false
Load buffer position1:
Tag: L2 Busy: 1 Effective Address: 2 Start Cycle: -1 Execute End Cycle: -1 Duration left: 1
Ready To Write: false
Store Buffers:
Store buffer position0:
Tag: S1 Busy: 0 Effective Address: -1 Start Cycle: -1 Execute End Cycle: -1 Duration left:
-1
      Ready To Write: false
Store buffer position1:
Tag: S2 Busy: 0 Effective Address: -1 Start Cycle: -1 Execute End Cycle: -1 Duration left:
-1
      Ready To Write: false
Register File:
R0: Tag: L1
              Busy: 1 Value: -1.0
R1: Tag: L2 Busy: 1 Value: -1.0
```

```
R2: Tag:
             Busy: 0 Value: -1.0
R3: Tag:
             Busy: 0 Value: -1.0
R4: Tag:
             Busy: 0 Value: -1.0
             Busy: 0 Value: -1.0
R5: Tag:
             Busy: 0 Value: -1.0
R6: Tag:
R7: Tag:
             Busy: 0 Value: -1.0
R8: Tag:
             Busy: 0 Value: -1.0
R9: Tag:
             Busy: 0 Value: -1.0
R10: Tag:
             Busy: 0 Value: -1.0
R11: Tag:
             Busy: 0 Value: -1.0
R12: Tag:
             Busy: 0 Value: -1.0
R13: Tag:
             Busy: 0 Value: -1.0
R14: Tag:
             Busy: 0 Value: -1.0
R15: Tag:
             Busy: 0 Value: -1.0
R16: Tag:
             Busy: 0 Value: -1.0
             Busy: 0 Value: -1.0
R17: Tag:
R18: Tag:
             Busy: 0 Value: -1.0
R19: Tag:
             Busy: 0 Value: -1.0
             Busy: 0 Value: 3.0
R20: Tag:
             Busy: 0 Value: -1.0
R21: Tag:
Memory:
M0: 0.0
M1: 1.0
M2: 2.0
M3: 0.0
M4: 0.0
M5: 0.0
M6: 0.0
Common Data Bus:
Tag: Value:
Current Instruction in PC: MUL R0,R0,R20
Instructions To Write:
stall is now false : false
Issue cycle of MUL R0,R0,R20 is 3
Made load read to write
Clock Cycle: 3
PC Value: 3
Reservation Stations:
Adder:
                             Start Cycle: -1 Execute End Cycle: -1 Busy: 0 Instruction
Adder position0: Tag: A1
Type: None Vj: Vk:
                        Qj:
                              Qk:
                                    A:
                                          Duration left: -1 Ready To Write: false
                             Start Cycle: -1 Execute End Cycle: -1 Busy: 0 Instruction
Adder position1: Tag: A2
                                          Duration left: -1 Ready To Write: false
Type: None Vj:
                 Vk:
                        Qj:
                              Qk:
                                    A:
Multiplier:
Multiplier position0:
Tag: M1 Start Cycle: -1 Execute End Cycle: -1 Busy: 1 Instruction Type: MUL Vj:
                                                                                   Vk: 3.0
Qj: L1 Qk:
                   Duration left: 3
                                      Ready To Write: false
           A:
```

```
Multiplier position1:
Tag: M2 Start Cycle: -1 Execute End Cycle: -1 Busy: 0 Instruction Type: None Vj:
           A:
                  Duration left: -1
                                      Ready To Write: false
Qi:
     Qk:
Load Buffers:
Load buffer position0:
Tag: L1 Busy: 1 Effective Address: 1
                                      Start Cycle: 2 Execute End Cycle: 3 Duration left: 1
Ready To Write: true
Load buffer position1:
                                      Start Cycle: 3 Execute End Cycle: 4 Duration left: 1
Tag: L2 Busy: 1 Effective Address: 2
Ready To Write: false
Store Buffers:
Store buffer position0:
Tag: S1 Busy: 0 Effective Address: -1 Start Cycle: -1 Execute End Cycle: -1 Duration left:
-1
      Ready To Write: false
Store buffer position1:
Tag: S2 Busy: 0 Effective Address: -1 Start Cycle: -1 Execute End Cycle: -1 Duration left:
-1
      Ready To Write: false
Register File:
R0: Tag: M1
               Busy: 1 Value: -1.0
R1: Tag: L2
              Busy: 1 Value: -1.0
             Busy: 0 Value: -1.0
R2: Tag:
             Busy: 0 Value: -1.0
R3: Tag:
R4: Tag:
             Busy: 0 Value: -1.0
R5: Tag:
             Busy: 0 Value: -1.0
R6: Tag:
             Busy: 0 Value: -1.0
             Busy: 0 Value: -1.0
R7: Tag:
             Busy: 0 Value: -1.0
R8: Tag:
R9: Tag:
             Busy: 0 Value: -1.0
R10: Tag:
             Busy: 0 Value: -1.0
             Busy: 0 Value: -1.0
R11: Tag:
R12: Tag:
             Busy: 0 Value: -1.0
R13: Tag:
             Busy: 0 Value: -1.0
R14: Tag:
             Busy: 0 Value: -1.0
R15: Tag:
             Busy: 0 Value: -1.0
R16: Tag:
             Busy: 0 Value: -1.0
R17: Tag:
             Busy: 0 Value: -1.0
             Busy: 0 Value: -1.0
R18: Tag:
R19: Tag:
             Busy: 0 Value: -1.0
             Busy: 0 Value: 3.0
R20: Tag:
R21: Tag:
             Busy: 0 Value: -1.0
Memory:
M0: 0.0
M1: 1.0
M2: 2.0
M3: 0.0
M4: 0.0
```

M5: 0.0 M6: 0.0 Common Data Bus: Tag: Value: Current Instruction in PC: MUL R1,R1,R20 Instructions To Write: LD R0, 1 stall is now false: false Issue cycle of MUL R1,R1,R20 is 4 Made load read to write Value of memory is: 1.0 and effective address is: 1 Instruction to be written: LD R0, 1 Clock Cycle: 4 PC Value: 4 **Reservation Stations:** Adder: Adder position0: Tag: A1 Start Cycle: -1 Execute End Cycle: -1 Busy: 0 Instruction Type: None Vj: Vk: Qj: Qk: Duration left: -1 Ready To Write: false Start Cycle: -1 Execute End Cycle: -1 Busy: 0 Instruction Adder position1: Tag: A2 Type: None Vj: Vk: Qj: Qk: A: Duration left: -1 Ready To Write: false Multiplier: Multiplier position0: Tag: M1 Start Cycle: -1 Execute End Cycle: -1 Busy: 1 Instruction Type: MUL Vi: 1.0 Vk: 3.0 Qj: Qk: A: Duration left: 3 Ready To Write: false Multiplier position1: Tag: M2 Start Cycle: -1 Execute End Cycle: -1 Busy: 1 Instruction Type: MUL Vj: Vk: 3.0 Qj: L2 Qk: A: Duration left: 3 Ready To Write: false Load Buffers: Load buffer position0: Tag: L1 Busy: 0 Effective Address: -1 Start Cycle: -1 Execute End Cycle: -1 Duration left: -1 Ready To Write: false Load buffer position1: Tag: L2 Busy: 1 Effective Address: 2 Start Cycle: 3 Execute End Cycle: 4 Duration left: 1 Ready To Write: true Store Buffers: Store buffer position0: Tag: S1 Busy: 0 Effective Address: -1 Start Cycle: -1 Execute End Cycle: -1 Duration left: Ready To Write: false -1 Store buffer position1: Tag: S2 Busy: 0 Effective Address: -1 Start Cycle: -1 Execute End Cycle: -1 Duration left: Ready To Write: false -1 Register File: R0: Tag: M1 Busy: 1 Value: 1.0 R1: Tag: M2 Busy: 1 Value: -1.0 R2: Tag: Busy: 0 Value: -1.0 R3: Tag: Busy: 0 Value: -1.0

Busy: 0 Value: -1.0

Busy: 0 Value: -1.0 Busy: 0 Value: -1.0

R4: Tag: R5: Tag:

R6: Tag:

```
R7: Tag:
             Busy: 0 Value: -1.0
R8: Tag:
             Busy: 0 Value: -1.0
             Busy: 0 Value: -1.0
R9: Tag:
R10: Tag:
             Busy: 0 Value: -1.0
             Busy: 0 Value: -1.0
R11: Tag:
             Busy: 0 Value: -1.0
R12: Tag:
R13: Tag:
             Busy: 0 Value: -1.0
R14: Tag:
             Busy: 0 Value: -1.0
R15: Tag:
             Busy: 0 Value: -1.0
R16: Tag:
             Busy: 0 Value: -1.0
R17: Tag:
             Busy: 0 Value: -1.0
             Busy: 0 Value: -1.0
R18: Tag:
R19: Tag:
             Busy: 0 Value: -1.0
R20: Tag:
             Busy: 0 Value: 3.0
             Busy: 0 Value: -1.0
R21: Tag:
Memory:
M0: 0.0
M1: 1.0
M2: 2.0
M3: 0.0
M4: 0.0
M5: 0.0
M6: 0.0
Common Data Bus:
Tag: L1 Value: 1.0
Current Instruction in PC: ADD R2,R0,R1
Instructions To Write:
LD R1, 2
stall is now false: false
Issue cycle of ADD R2,R0,R1 is 5
CAN EXECUTE MULTIPLY MUL R0,R0,R20
Value of memory is: 2.0 and effective address is: 2
Instruction to be written: LD R1, 2
Clock Cycle: 5
PC Value: 5
Reservation Stations:
Adder:
Adder position0: Tag: A1
                             Start Cycle: -1 Execute End Cycle: -1 Busy: 1 Instruction
Type: ADD Vj:
                 Vk:
                        Qj: M1 Qk: M2 A:
                                              Duration left: 2 Ready To Write: false
Adder position1: Tag: A2
                            Start Cycle: -1 Execute End Cycle: -1 Busy: 0 Instruction
Type: None Vj:
                 Vk:
                        Qj: Qk: A:
                                          Duration left: -1 Ready To Write: false
Multiplier:
Multiplier position0:
Tag: M1 Start Cycle: 5 Execute End Cycle: 8 Busy: 1 Instruction Type: MUL Vj: 1.0 Vk:
         Qk:
                     Duration left: 3
                                         Ready To Write: false
3.0 Qj:
              A:
Multiplier position1:
```

```
Tag: M2 Start Cycle: -1 Execute End Cycle: -1 Busy: 1 Instruction Type: MUL Vj: 2.0 Vk:
                                         Ready To Write: false
3.0 Qj:
         Qk:
                A:
                      Duration left: 3
Load Buffers:
Load buffer position0:
Tag: L1 Busy: 0 Effective Address: -1 Start Cycle: -1 Execute End Cycle: -1 Duration left:
      Ready To Write: false
Load buffer position1:
Tag: L2 Busy: 0 Effective Address: -1 Start Cycle: -1 Execute End Cycle: -1 Duration left:
      Ready To Write: false
Store Buffers:
Store buffer position0:
Tag: S1 Busy: 0 Effective Address: -1 Start Cycle: -1 Execute End Cycle: -1 Duration left:
-1
      Ready To Write: false
Store buffer position1:
Tag: S2 Busy: 0 Effective Address: -1 Start Cycle: -1 Execute End Cycle: -1 Duration left:
      Ready To Write: false
-1
Register File:
R0: Tag: M1
               Busy: 1 Value: 1.0
               Busy: 1 Value: 2.0
R1: Tag: M2
               Busy: 1 Value: -1.0
R2: Tag: A1
R3: Tag:
             Busy: 0 Value: -1.0
R4: Tag:
             Busy: 0 Value: -1.0
R5: Tag:
             Busy: 0 Value: -1.0
R6: Tag:
             Busy: 0 Value: -1.0
R7: Tag:
             Busy: 0 Value: -1.0
R8: Tag:
             Busy: 0 Value: -1.0
             Busy: 0 Value: -1.0
R9: Tag:
             Busy: 0 Value: -1.0
R10: Tag:
R11: Tag:
             Busy: 0 Value: -1.0
R12: Tag:
             Busy: 0 Value: -1.0
             Busy: 0 Value: -1.0
R13: Tag:
R14: Tag:
             Busy: 0 Value: -1.0
R15: Tag:
             Busy: 0 Value: -1.0
R16: Tag:
             Busy: 0 Value: -1.0
R17: Tag:
             Busy: 0 Value: -1.0
R18: Tag:
             Busy: 0 Value: -1.0
             Busy: 0 Value: -1.0
R19: Tag:
R20: Tag:
             Busy: 0 Value: 3.0
             Busy: 0 Value: -1.0
R21: Tag:
Memory:
M0: 0.0
M1: 1.0
M2: 2.0
M3: 0.0
M4: 0.0
M5: 0.0
M6: 0.0
```

Common Data Bus:

Tag: L2 Value: 2.0

Current Instruction in PC: ADD R20,R20,R20

Instructions To Write:

-----

stall is now false: false

Issue cycle of ADD R20,R20,R20 is 6

CAN EXECUTE MULTIPLY MUL R1,R1,R20

Clock Cycle: 6 PC Value: 6

**Reservation Stations:** 

Adder:

Adder position0: Tag: A1 Start Cycle: -1 Execute End Cycle: -1 Busy: 1 Instruction Type: ADD Vj: Vk: Qj: M1 Qk: M2 A: Duration left: 2 Ready To Write: false Adder position1: Tag: A2 Start Cycle: -1 Execute End Cycle: -1 Busy: 1 Instruction Type: ADD Vj: 3.0 Vk: 3.0 Qj: Qk: A: Duration left: 2 Ready To Write: false Multiplier:

Multiplier position0:

Tag: M1 Start Cycle: 5 Execute End Cycle: 8 Busy: 1 Instruction Type: MUL Vj: 1.0 Vk:

3.0 Qj: Qk: A: Duration left: 2 Ready To Write: false

Multiplier position1:

Tag: M2 Start Cycle: 6 Execute End Cycle: 9 Busy: 1 Instruction Type: MUL Vj: 2.0 Vk:

3.0 Qj: Qk: A: Duration left: 3 Ready To Write: false

Load Buffers:

Load buffer position0:

Tag: L1 Busy: 0 Effective Address: -1 Start Cycle: -1 Execute End Cycle: -1 Duration left:

-1 Ready To Write: false

Load buffer position1:

Tag: L2 Busy: 0 Effective Address: -1 Start Cycle: -1 Execute End Cycle: -1 Duration left:

-1 Ready To Write: false

Store Buffers:

Store buffer position0:

Tag: S1 Busy: 0 Effective Address: -1 Start Cycle: -1 Execute End Cycle: -1 Duration left:

-1 Ready To Write: false

Store buffer position1:

Tag: S2 Busy: 0 Effective Address: -1 Start Cycle: -1 Execute End Cycle: -1 Duration left:

-1 Ready To Write: false

Register File:

R0: Tag: M1 Busy: 1 Value: 1.0 R1: Tag: M2 Busy: 1 Value: 2.0 R2: Tag: A1 Busy: 1 Value: -1.0 Busy: 0 Value: -1.0 R3: Tag: R4: Tag: Busy: 0 Value: -1.0 R5: Tag: Busy: 0 Value: -1.0 R6: Tag: Busy: 0 Value: -1.0 R7: Tag: Busy: 0 Value: -1.0 Busy: 0 Value: -1.0 R8: Tag:

R9: Tag: Busy: 0 Value: -1.0 R10: Tag: Busy: 0 Value: -1.0

```
R11: Tag:
             Busy: 0 Value: -1.0
R12: Tag:
             Busy: 0 Value: -1.0
R13: Tag:
             Busy: 0 Value: -1.0
             Busy: 0 Value: -1.0
R14: Tag:
             Busy: 0 Value: -1.0
R15: Tag:
             Busy: 0 Value: -1.0
R16: Tag:
R17: Tag:
             Busy: 0 Value: -1.0
R18: Tag:
             Busy: 0 Value: -1.0
R19: Tag:
             Busy: 0 Value: -1.0
R20: Tag: A2 Busy: 1 Value: 3.0
             Busy: 0 Value: -1.0
R21: Tag:
Memory:
M0: 0.0
M1: 1.0
M2: 2.0
M3: 0.0
M4: 0.0
M5: 0.0
M6: 0.0
Common Data Bus:
Tag: L2 Value: 2.0
Current Instruction in PC: SD R2,5
Instructions To Write:
stall is now false: false
Issue cycle of SD R2,5 is 7
Clock Cycle: 7
PC Value: 7
Reservation Stations:
Adder:
Adder position0: Tag: A1
                            Start Cycle: -1 Execute End Cycle: -1 Busy: 1 Instruction
                                              Duration left: 2 Ready To Write: false
Type: ADD Vj: Vk:
                        Qj: M1 Qk: M2 A:
Adder position1: Tag: A2
                            Start Cycle: 7 Execute End Cycle: 9 Busy: 1 Instruction
Type: ADD Vj: 3.0 Vk: 3.0 Qj:
                                Qk:
                                     A:
                                            Duration left: 2 Ready To Write: false
Multiplier:
Multiplier position0:
Tag: M1 Start Cycle: 5 Execute End Cycle: 8 Busy: 1 Instruction Type: MUL Vj: 1.0 Vk:
3.0 Qj:
         Qk:
              A:
                     Duration left: 1
                                         Ready To Write: true
Multiplier position1:
Tag: M2 Start Cycle: 6 Execute End Cycle: 9 Busy: 1 Instruction Type: MUL Vj: 2.0 Vk:
                     Duration left: 2
                                         Ready To Write: false
3.0 Qj: Qk:
              A:
Load Buffers:
```

Tag: L2 Busy: 0 Effective Address: -1 Start Cycle: -1 Execute End Cycle: -1 Duration left: -1 Ready To Write: false

Tag: L1 Busy: 0 Effective Address: -1 Start Cycle: -1 Execute End Cycle: -1 Duration left:

Load buffer position0:

Load buffer position1:

Ready To Write: false

-1

```
Store Buffers:
Store buffer position0:
Tag: S1 Busy: 1 Effective Address: 5
                                      Start Cycle: -1 Execute End Cycle: -1 Duration left:
      Ready To Write: false
Store buffer position1:
Tag: S2 Busy: 0 Effective Address: -1 Start Cycle: -1 Execute End Cycle: -1 Duration left:
      Ready To Write: false
-1
Register File:
R0: Tag: M1
               Busy: 1 Value: 1.0
R1: Tag: M2
              Busy: 1 Value: 2.0
R2: Tag: A1
              Busy: 1 Value: -1.0
             Busy: 0 Value: -1.0
R3: Tag:
R4: Tag:
             Busy: 0 Value: -1.0
R5: Tag:
             Busy: 0 Value: -1.0
             Busy: 0 Value: -1.0
R6: Tag:
R7: Tag:
             Busy: 0 Value: -1.0
R8: Tag:
             Busy: 0 Value: -1.0
R9: Tag:
             Busy: 0 Value: -1.0
             Busy: 0 Value: -1.0
R10: Tag:
             Busy: 0 Value: -1.0
R11: Tag:
             Busy: 0 Value: -1.0
R12: Tag:
             Busy: 0 Value: -1.0
R13: Tag:
R14: Tag:
             Busy: 0 Value: -1.0
R15: Tag:
             Busy: 0 Value: -1.0
R16: Tag:
             Busy: 0 Value: -1.0
R17: Tag:
             Busy: 0 Value: -1.0
             Busy: 0 Value: -1.0
R18: Tag:
R19: Tag:
             Busy: 0 Value: -1.0
R20: Tag: A2 Busy: 1 Value: 3.0
             Busy: 0 Value: -1.0
R21: Tag:
Memory:
M0: 0.0
M1: 1.0
M2: 2.0
M3: 0.0
M4: 0.0
M5: 0.0
M6: 0.0
Common Data Bus:
Tag: L2 Value: 2.0
Instructions To Write:
MUL R0,R0,R20
Instruction to be written: MUL R0,R0,R20
Clock Cycle: 8
```

Adder:

PC Value: 7

**Reservation Stations:** 

Adder position0: Tag: A1 Start Cycle: -1 Execute End Cycle: -1 Busy: 1 Instruction Type: ADD Vj: 3.0 Vk: Qj: Qk: M2 A: Duration left: 2 Ready To Write: false Adder position1: Tag: A2 Start Cycle: 7 Execute End Cycle: 9 Busy: 1 Instruction Type: ADD Vj: 3.0 Vk: 3.0 Qj: Qk: A: Duration left: 1 Ready To Write: true Multiplier:

Multiplier position0:

Tag: M1 Start Cycle: -1 Execute End Cycle: -1 Busy: 0 Instruction Type: None Vj: Vk:

Qj: Qk: A: Duration left: -1 Ready To Write: false

Multiplier position1:

Tag: M2 Start Cycle: 6 Execute End Cycle: 9 Busy: 1 Instruction Type: MUL Vj: 2.0 Vk:

3.0 Qj: Qk: A: Duration left: 1 Ready To Write: true

Load Buffers:

Load buffer position0:

Tag: L1 Busy: 0 Effective Address: -1 Start Cycle: -1 Execute End Cycle: -1 Duration left:

-1 Ready To Write: false

Load buffer position1:

Tag: L2 Busy: 0 Effective Address: -1 Start Cycle: -1 Execute End Cycle: -1 Duration left:

-1 Ready To Write: false

Store Buffers:

Store buffer position0:

Tag: S1 Busy: 1 Effective Address: 5 Start Cycle: -1 Execute End Cycle: -1 Duration left:

1 Ready To Write: false

Store buffer position1:

Tag: S2 Busy: 0 Effective Address: -1 Start Cycle: -1 Execute End Cycle: -1 Duration left:

-1 Ready To Write: false

Register File:

R0: Tag: Busy: 0 Value: 3.0
R1: Tag: M2 Busy: 1 Value: 2.0
R2: Tag: A1 Busy: 1 Value: -1.0
R3: Tag: Busy: 0 Value: -1.0
R4: Tag: Busy: 0 Value: -1.0
R5: Tag: Busy: 0 Value: -1.0
R6: Tag: Busy: 0 Value: -1.0
R6: Tag: Busy: 0 Value: -1.0

R7: Tag: Busy: 0 Value: -1.0

R8: Tag: Busy: 0 Value: -1.0 R9: Tag: Busy: 0 Value: -1.0

R10: Tag: Busy: 0 Value: -1.0

R11: Tag: Busy: 0 Value: -1.0

R12: Tag: Busy: 0 Value: -1.0

R13: Tag: Busy: 0 Value: -1.0

R14: Tag: Busy: 0 Value: -1.0

R15: Tag: Busy: 0 Value: -1.0

R16: Tag: Busy: 0 Value: -1.0 R17: Tag: Busy: 0 Value: -1.0

R18: Tag: Busy: 0 Value: -1.0

R19: Tag: Busy: 0 Value: -1.0

R20: Tag: A2 Busy: 1 Value: 3.0

R21: Tag: Busy: 0 Value: -1.0

```
Memory:
M0: 0.0
M1: 1.0
M2: 2.0
M3: 0.0
M4: 0.0
M5: 0.0
M6: 0.0
Common Data Bus:
Tag: M1 Value: 3.0
Instructions To Write:
MUL R1,R1,R20
ADD R20,R20,R20
Instruction to be written: MUL R1,R1,R20
Clock Cycle: 9
PC Value: 7
Reservation Stations:
Adder:
Adder position0: Tag: A1
                            Start Cycle: -1 Execute End Cycle: -1 Busy: 1 Instruction
Type: ADD Vi: 3.0 Vk: 6.0 Qi: Qk:
                                             Duration left: 2 Ready To Write: false
                                       A:
Adder position1: Tag: A2
                             Start Cycle: 7 Execute End Cycle: 9 Busy: 1 Instruction
Type: ADD Vj: 3.0 Vk: 3.0 Qj:
                                Qk: A:
                                             Duration left: 1 Ready To Write: true
Multiplier:
Multiplier position0:
Tag: M1 Start Cycle: -1 Execute End Cycle: -1 Busy: 0 Instruction Type: None Vj:
                                                                                   Vk:
                 Duration left: -1
                                     Ready To Write: false
     Qk: A:
Multiplier position1:
Tag: M2 Start Cycle: -1 Execute End Cycle: -1 Busy: 0 Instruction Type: None Vj:
                                                                                   Vk:
                                     Ready To Write: false
Qi:
     Qk: A:
                 Duration left: -1
Load Buffers:
Load buffer position0:
Tag: L1 Busy: 0 Effective Address: -1 Start Cycle: -1 Execute End Cycle: -1 Duration left:
      Ready To Write: false
Load buffer position1:
Tag: L2 Busy: 0 Effective Address: -1 Start Cycle: -1 Execute End Cycle: -1 Duration left:
      Ready To Write: false
-1
Store Buffers:
Store buffer position0:
Tag: S1 Busy: 1 Effective Address: 5 Start Cycle: -1 Execute End Cycle: -1 Duration left:
      Ready To Write: false
Store buffer position1:
Tag: S2 Busy: 0 Effective Address: -1 Start Cycle: -1 Execute End Cycle: -1 Duration left:
-1
      Ready To Write: false
```

Register File: R0: Tag:

R1: Tag:

Busy: 0 Value: 3.0

Busy: 0 Value: 6.0

R2: Tag: A1 Busy: 1 Value: -1.0

```
R3: Tag:
             Busy: 0 Value: -1.0
R4: Tag:
             Busy: 0 Value: -1.0
R5: Tag:
             Busy: 0 Value: -1.0
R6: Tag:
             Busy: 0 Value: -1.0
             Busy: 0 Value: -1.0
R7: Tag:
R8: Tag:
             Busy: 0 Value: -1.0
R9: Tag:
             Busy: 0 Value: -1.0
R10: Tag:
             Busy: 0 Value: -1.0
R11: Tag:
             Busy: 0 Value: -1.0
R12: Tag:
             Busy: 0 Value: -1.0
R13: Tag:
             Busy: 0 Value: -1.0
R14: Tag:
             Busy: 0 Value: -1.0
R15: Tag:
             Busy: 0 Value: -1.0
R16: Tag:
             Busy: 0 Value: -1.0
             Busy: 0 Value: -1.0
R17: Tag:
             Busy: 0 Value: -1.0
R18: Tag:
R19: Tag:
             Busy: 0 Value: -1.0
R20: Tag: A2 Busy: 1 Value: 3.0
             Busy: 0 Value: -1.0
R21: Tag:
Memory:
M0: 0.0
M1: 1.0
M2: 2.0
M3: 0.0
M4: 0.0
M5: 0.0
M6: 0.0
Common Data Bus:
Tag: M2 Value: 6.0
Instructions To Write:
ADD R20,R20,R20
Instruction to be written: ADD R20,R20,R20
Clock Cycle: 10
PC Value: 7
Reservation Stations:
Adder:
Adder position0: Tag: A1
                             Start Cycle: 10 Execute End Cycle: 12 Busy: 1 Instruction
Type: ADD Vj: 3.0 Vk: 6.0 Qj:
                                Qk:
                                       A:
                                             Duration left: 2 Ready To Write: false
Adder position1: Tag: A2
                             Start Cycle: -1 Execute End Cycle: -1 Busy: 0 Instruction
Type: None Vj: Vk: Qj:
                                          Duration left: -1 Ready To Write: false
                              Qk: A:
Multiplier:
Multiplier position0:
Tag: M1 Start Cycle: -1 Execute End Cycle: -1 Busy: 0 Instruction Type: None Vj:
                                                                                    Vk:
                  Duration left: -1
                                     Ready To Write: false
Qj:
     Qk:
            A:
Multiplier position1:
Tag: M2 Start Cycle: -1 Execute End Cycle: -1 Busy: 0 Instruction Type: None Vj:
                                                                                    Vk:
           A:
                  Duration left: -1
                                     Ready To Write: false
Qj:
     Qk:
```

```
Load Buffers:
Load buffer position0:
Tag: L1 Busy: 0 Effective Address: -1 Start Cycle: -1 Execute End Cycle: -1 Duration left:
-1
      Ready To Write: false
Load buffer position1:
Tag: L2 Busy: 0 Effective Address: -1 Start Cycle: -1 Execute End Cycle: -1 Duration left:
      Ready To Write: false
-1
Store Buffers:
Store buffer position0:
Tag: S1 Busy: 1 Effective Address: 5
                                      Start Cycle: -1 Execute End Cycle: -1 Duration left:
      Ready To Write: false
Store buffer position1:
Tag: S2 Busy: 0 Effective Address: -1 Start Cycle: -1 Execute End Cycle: -1 Duration left:
-1
      Ready To Write: false
Register File:
R0: Tag:
             Busy: 0 Value: 3.0
R1: Tag:
             Busy: 0 Value: 6.0
R2: Tag: A1
               Busy: 1 Value: -1.0
R3: Tag:
             Busy: 0 Value: -1.0
R4: Tag:
             Busy: 0 Value: -1.0
             Busy: 0 Value: -1.0
R5: Tag:
R6: Tag:
             Busy: 0 Value: -1.0
R7: Tag:
             Busy: 0 Value: -1.0
R8: Tag:
             Busy: 0 Value: -1.0
R9: Tag:
             Busy: 0 Value: -1.0
R10: Tag:
             Busy: 0 Value: -1.0
             Busy: 0 Value: -1.0
R11: Tag:
R12: Tag:
              Busy: 0 Value: -1.0
R13: Tag:
             Busy: 0 Value: -1.0
             Busy: 0 Value: -1.0
R14: Tag:
R15: Tag:
             Busy: 0 Value: -1.0
             Busy: 0 Value: -1.0
R16: Tag:
R17: Tag:
             Busy: 0 Value: -1.0
R18: Tag:
             Busy: 0 Value: -1.0
R19: Tag:
             Busy: 0 Value: -1.0
R20: Tag:
             Busy: 0 Value: 6.0
             Busy: 0 Value: -1.0
R21: Tag:
Memory:
M0: 0.0
M1: 1.0
M2: 2.0
M3: 0.0
M4: 0.0
M5: 0.0
M6: 0.0
```

Common Data Bus:

Tag: A2 Value: 6.0 Instructions To Write:

\_\_\_\_\_

Clock Cycle: 11 PC Value: 7

**Reservation Stations:** 

Adder:

Adder position0: Tag: A1 Start Cycle: 10 Execute End Cycle: 12 Busy: 1 Instruction Type: ADD Vj: 3.0 Vk: 6.0 Qj: Qk: A: Duration left: 1 Ready To Write: true Adder position1: Tag: A2 Start Cycle: -1 Execute End Cycle: -1 Busy: 0 Instruction Type: None Vj: Vk: Qj: Qk: A: Duration left: -1 Ready To Write: false Multiplier:

Multiplier position0:

Tag: M1 Start Cycle: -1 Execute End Cycle: -1 Busy: 0 Instruction Type: None Vj: Vk:

Qj: Qk: A: Duration left: -1 Ready To Write: false

Multiplier position1:

Tag: M2 Start Cycle: -1 Execute End Cycle: -1 Busy: 0 Instruction Type: None Vj: Vk:

Qj: Qk: A: Duration left: -1 Ready To Write: false

Load Buffers:

Load buffer position0:

Tag: L1 Busy: 0 Effective Address: -1 Start Cycle: -1 Execute End Cycle: -1 Duration left:

-1 Ready To Write: false

Load buffer position1:

Tag: L2 Busy: 0 Effective Address: -1 Start Cycle: -1 Execute End Cycle: -1 Duration left:

-1 Ready To Write: false

Store Buffers:

Store buffer position0:

Tag: S1 Busy: 1 Effective Address: 5 Start Cycle: -1 Execute End Cycle: -1 Duration left:

1 Ready To Write: false

Store buffer position1:

Tag: S2 Busy: 0 Effective Address: -1 Start Cycle: -1 Execute End Cycle: -1 Duration left:

-1 Ready To Write: false

Register File:

R0: Tag: Busy: 0 Value: 3.0 R1: Tag: Busy: 0 Value: 6.0 R2: Tag: A1 Busy: 1 Value: -1.0 R3: Tag: Busy: 0 Value: -1.0 R4: Tag: Busy: 0 Value: -1.0 Busy: 0 Value: -1.0 R5: Tag: R6: Tag: Busy: 0 Value: -1.0 Busy: 0 Value: -1.0 R7: Tag: R8: Tag: Busy: 0 Value: -1.0 Busy: 0 Value: -1.0 R9: Tag:

R10: Tag: Busy: 0 Value: -1.0

R11: Tag: Busy: 0 Value: -1.0

R12: Tag: Busy: 0 Value: -1.0 R13: Tag: Busy: 0 Value: -1.0

R14: Tag: Busy: 0 Value: -1.0

R15: Tag: Busy: 0 Value: -1.0

R16: Tag: Busy: 0 Value: -1.0

```
R17: Tag:
             Busy: 0 Value: -1.0
R18: Tag:
             Busy: 0 Value: -1.0
R19: Tag:
             Busy: 0 Value: -1.0
R20: Tag:
             Busy: 0 Value: 6.0
             Busy: 0 Value: -1.0
R21: Tag:
Memory:
M0: 0.0
M1: 1.0
M2: 2.0
M3: 0.0
M4: 0.0
M5: 0.0
M6: 0.0
Common Data Bus:
Tag: A2 Value: 6.0
Instructions To Write:
ADD R2,R0,R1
Instruction to be written: ADD R2,R0,R1
Clock Cycle: 12
PC Value: 7
Reservation Stations:
Adder:
Adder position0: Tag: A1
                            Start Cycle: -1 Execute End Cycle: -1 Busy: 0 Instruction
Type: None Vj: Vk:
                              Qk:
                                    A:
                                          Duration left: -1 Ready To Write: false
                        Qj:
Adder position1: Tag: A2
                            Start Cycle: -1 Execute End Cycle: -1 Busy: 0 Instruction
Type: None Vi:
                                          Duration left: -1 Ready To Write: false
                Vk:
                        Qj:
                              Qk:
                                   A:
Multiplier:
Multiplier position0:
Tag: M1 Start Cycle: -1 Execute End Cycle: -1 Busy: 0 Instruction Type: None Vj:
                                                                                   Vk:
     Qk:
           A:
                 Duration left: -1
                                     Ready To Write: false
Qi:
Multiplier position1:
Tag: M2 Start Cycle: -1 Execute End Cycle: -1 Busy: 0 Instruction Type: None Vj:
                                                                                   Vk:
Qj:
     Qk:
           A:
                 Duration left: -1
                                     Ready To Write: false
Load Buffers:
Load buffer position0:
Tag: L1 Busy: 0 Effective Address: -1 Start Cycle: -1 Execute End Cycle: -1 Duration left:
      Ready To Write: false
Load buffer position1:
Tag: L2 Busy: 0 Effective Address: -1 Start Cycle: -1 Execute End Cycle: -1 Duration left:
```

Tag: S2 Busy: 0 Effective Address: -1 Start Cycle: -1 Execute End Cycle: -1 Duration left:

Start Cycle: -1 Execute End Cycle: -1 Duration left:

Ready To Write: false

Ready To Write: false

Ready To Write: false

Tag: S1 Busy: 1 Effective Address: 5

-1

1

-1

Store Buffers:

Store buffer position0:

Store buffer position1:

```
Register File:
R0: Tag:
             Busy: 0 Value: 3.0
             Busy: 0 Value: 6.0
R1: Tag:
R2: Tag:
             Busy: 0 Value: 9.0
             Busy: 0 Value: -1.0
R3: Tag:
R4: Tag:
             Busy: 0 Value: -1.0
R5: Tag:
             Busy: 0 Value: -1.0
R6: Tag:
             Busy: 0 Value: -1.0
R7: Tag:
             Busy: 0 Value: -1.0
R8: Tag:
             Busy: 0 Value: -1.0
R9: Tag:
             Busy: 0 Value: -1.0
             Busy: 0 Value: -1.0
R10: Tag:
R11: Tag:
             Busy: 0 Value: -1.0
R12: Tag:
             Busy: 0 Value: -1.0
             Busy: 0 Value: -1.0
R13: Tag:
             Busy: 0 Value: -1.0
R14: Tag:
R15: Tag:
             Busy: 0 Value: -1.0
R16: Tag:
             Busy: 0 Value: -1.0
             Busy: 0 Value: -1.0
R17: Tag:
             Busy: 0 Value: -1.0
R18: Tag:
R19: Tag:
             Busy: 0 Value: -1.0
R20: Tag:
             Busy: 0 Value: 6.0
R21: Tag:
             Busy: 0 Value: -1.0
Memory:
M0: 0.0
M1: 1.0
M2: 2.0
M3: 0.0
M4: 0.0
M5: 0.0
M6: 0.0
Common Data Bus:
Tag: A1 Value: 9.0
Instructions To Write:
Clock Cycle: 13
PC Value: 7
Reservation Stations:
Adder:
                             Start Cycle: -1 Execute End Cycle: -1 Busy: 0 Instruction
Adder position0: Tag: A1
Type: None Vj:
                                           Duration left: -1 Ready To Write: false
                  Vk:
                        Qj:
                              Qk:
                                     A:
                             Start Cycle: -1 Execute End Cycle: -1 Busy: 0 Instruction
Adder position1: Tag: A2
Type: None Vj:
                                           Duration left: -1 Ready To Write: false
                  Vk:
                        Qj:
                              Qk:
                                     A:
Multiplier:
Multiplier position0:
Tag: M1 Start Cycle: -1 Execute End Cycle: -1 Busy: 0 Instruction Type: None Vj:
                                                                                     Vk:
                                      Ready To Write: false
Qj:
     Qk:
           A:
                  Duration left: -1
Multiplier position1:
```

```
Tag: M2 Start Cycle: -1 Execute End Cycle: -1 Busy: 0 Instruction Type: None Vj:
Qj:
     Qk:
            A:
                  Duration left: -1
                                      Ready To Write: false
Load Buffers:
Load buffer position0:
Tag: L1 Busy: 0 Effective Address: -1 Start Cycle: -1 Execute End Cycle: -1 Duration left:
      Ready To Write: false
Load buffer position1:
Tag: L2 Busy: 0 Effective Address: -1 Start Cycle: -1 Execute End Cycle: -1 Duration left:
      Ready To Write: false
Store Buffers:
Store buffer position0:
Tag: S1 Busy: 1 Effective Address: 5
                                      Start Cycle: 13 Execute End Cycle: 14 Duration left:
      Ready To Write: false
1
Store buffer position1:
Tag: S2 Busy: 0 Effective Address: -1 Start Cycle: -1 Execute End Cycle: -1 Duration left:
      Ready To Write: false
-1
Register File:
R0: Tag:
             Busy: 0 Value: 3.0
             Busy: 0 Value: 6.0
R1: Tag:
             Busy: 0 Value: 9.0
R2: Tag:
R3: Tag:
             Busy: 0 Value: -1.0
R4: Tag:
             Busy: 0 Value: -1.0
R5: Tag:
             Busy: 0 Value: -1.0
R6: Tag:
             Busy: 0 Value: -1.0
R7: Tag:
             Busy: 0 Value: -1.0
R8: Tag:
             Busy: 0 Value: -1.0
             Busy: 0 Value: -1.0
R9: Tag:
             Busy: 0 Value: -1.0
R10: Tag:
R11: Tag:
             Busy: 0 Value: -1.0
R12: Tag:
             Busy: 0 Value: -1.0
R13: Tag:
             Busy: 0 Value: -1.0
R14: Tag:
             Busy: 0 Value: -1.0
R15: Tag:
             Busy: 0 Value: -1.0
R16: Tag:
             Busy: 0 Value: -1.0
R17: Tag:
             Busy: 0 Value: -1.0
R18: Tag:
             Busy: 0 Value: -1.0
             Busy: 0 Value: -1.0
R19: Tag:
R20: Tag:
             Busy: 0 Value: 6.0
             Busy: 0 Value: -1.0
R21: Tag:
Memory:
M0: 0.0
M1: 1.0
M2: 2.0
M3: 0.0
M4: 0.0
M5: 0.0
M6: 0.0
```

Common Data Bus:

Tag: A1 Value: 9.0 Instructions To Write:

\_\_\_\_\_

Clock Cycle: 14 PC Value: 7

Reservation Stations:

Adder:

Adder position0: Tag: A1 Start Cycle: -1 Execute End Cycle: -1 Busy: 0 Instruction Type: None Vj: Vk: Qj: Qk: A: Duration left: -1 Ready To Write: false Adder position1: Tag: A2 Start Cycle: -1 Execute End Cycle: -1 Busy: 0 Instruction Type: None Vj: Vk: Qj: Qk: A: Duration left: -1 Ready To Write: false Multiplier:

Multiplier position0:

Tag: M1 Start Cycle: -1 Execute End Cycle: -1 Busy: 0 Instruction Type: None Vj: Vk:

Qj: Qk: A: Duration left: -1 Ready To Write: false

Multiplier position1:

Tag: M2 Start Cycle: -1 Execute End Cycle: -1 Busy: 0 Instruction Type: None Vj: Vk:

Qj: Qk: A: Duration left: -1 Ready To Write: false

Load Buffers:

Load buffer position0:

Tag: L1 Busy: 0 Effective Address: -1 Start Cycle: -1 Execute End Cycle: -1 Duration left:

-1 Ready To Write: false

Load buffer position1:

Tag: L2 Busy: 0 Effective Address: -1 Start Cycle: -1 Execute End Cycle: -1 Duration left:

-1 Ready To Write: false

Store Buffers:

Store buffer position0:

Tag: S1 Busy: 0 Effective Address: -1 Start Cycle: -1 Execute End Cycle: -1 Duration left:

-1 Ready To Write: false

Store buffer position1:

Tag: S2 Busy: 0 Effective Address: -1 Start Cycle: -1 Execute End Cycle: -1 Duration left:

-1 Ready To Write: false

Register File:

R0: Tag: Busy: 0 Value: 3.0 R1: Tag: Busy: 0 Value: 6.0 R2: Tag: Busy: 0 Value: 9.0 Busy: 0 Value: -1.0 R3: Tag: R4: Tag: Busy: 0 Value: -1.0 Busy: 0 Value: -1.0 R5: Tag: R6: Tag: Busy: 0 Value: -1.0 Busy: 0 Value: -1.0 R7: Tag: R8: Tag: Busy: 0 Value: -1.0

R9: Tag: Busy: 0 Value: -1.0

R10: Tag: Busy: 0 Value: -1.0 R11: Tag: Busy: 0 Value: -1.0

R12: Tag: Busy: 0 Value: -1.0

R13: Tag: Busy: 0 Value: -1.0 R14: Tag: Busy: 0 Value: -1.0

```
R15: Tag: Busy: 0 Value: -1.0 R16: Tag: Busy: 0 Value: -1.0 R17: Tag: Busy: 0 Value: -1.0 R18: Tag: Busy: 0 Value: -1.0 R19: Tag: Busy: 0 Value: -1.0 R20: Tag: Busy: 0 Value: 6.0 R21: Tag: Busy: 0 Value: -1.0
```

Memory: M0: 0.0 M1: 1.0 M2: 2.0 M3: 0.0 M4: 0.0 M5: 9.0 M6: 0.0

Common Data Bus: Tag: A1 Value: 9.0 Instructions To Write:

-----

## Input:

MUL R3, R1, R2 ADD R5, R3, R4 ADD R7, R2, R6 ADD R10, R8, R9 MUL R11, R7, R10 ADD R5, R5, R11

## Result:

end is 6

stall is now false : false

Issue cycle of MUL R3, R1, R2 is 1

Clock Cycle: 1 PC Value: 1

**Reservation Stations:** 

Adder:

Adder position0: Tag: A1 Start Cycle: -1 Execute End Cycle: -1 Busy: 0 Instruction Type: None Vj: Vk: Qj: A: Duration left: -1 Ready To Write: false Adder position1: Tag: A2 Start Cycle: -1 Execute End Cycle: -1 Busy: 0 Instruction Type: None Vj: Qk: A: Duration left: -1 Ready To Write: false Vk: Qj: Adder position2: Tag: A3 Start Cycle: -1 Execute End Cycle: -1 Busy: 0 Instruction Type: None Vj: Vk: Qk: A: Duration left: -1 Ready To Write: false Qj:

```
Multiplier:
Multiplier position0:
Tag: M1 Start Cycle: -1 Execute End Cycle: -1 Busy: 1 Instruction Type: MUL Vj: 1.0 Vk:
                      Duration left: 6 Ready To Write: false
2.0 Qj:
         Qk:
              A:
Multiplier position1:
Tag: M2 Start Cycle: -1 Execute End Cycle: -1 Busy: 0 Instruction Type: None Vj: Vk:
                  Duration left: -1 Ready To Write: false
Load Buffers:
Load buffer position0:
Tag: L1 Busy: 0 Effective Address: -1 Start Cycle: -1 Execute End Cycle: -1 Duration left:
      Ready To Write: false
Load buffer position1:
Tag: L2 Busy: 0 Effective Address: -1 Start Cycle: -1 Execute End Cycle: -1 Duration left:
      Ready To Write: false
Load buffer position2:
Tag: L3 Busy: 0 Effective Address: -1 Start Cycle: -1 Execute End Cycle: -1 Duration left:
      Ready To Write: false
Store Buffers:
Store buffer position0:
Tag: S1 Busy: 0 Effective Address: -1 Start Cycle: -1 Execute End Cycle: -1 Duration left:
      Ready To Write: false
Store buffer position1:
Tag: S2 Busy: 0 Effective Address: -1 Start Cycle: -1 Execute End Cycle: -1 Duration left:
      Ready To Write: false
Store buffer position2:
Tag: S3 Busy: 0 Effective Address: -1 Start Cycle: -1 Execute End Cycle: -1 Duration left:
      Ready To Write: false
-1
Register File:
R0: Tag:
             Busy: 0 Value: -1.0
             Busy: 0 Value: 1.0
R1: Tag:
R2: Tag:
             Busy: 0 Value: 2.0
R3: Tag: M1
               Busy: 1 Value: -1.0
R4: Tag:
             Busy: 0 Value: 3.0
R5: Tag:
             Busy: 0 Value: -1.0
R6: Tag:
             Busy: 0 Value: 4.0
R7: Tag:
             Busy: 0 Value: -1.0
             Busy: 0 Value: 5.0
R8: Tag:
R9: Tag:
             Busy: 0 Value: 6.0
R10: Tag:
             Busy: 0 Value: -1.0
R11: Tag:
             Busy: 0 Value: -1.0
R12: Tag:
             Busy: 0 Value: -1.0
R13: Tag:
             Busy: 0 Value: -1.0
R14: Tag:
             Busy: 0 Value: -1.0
Memory:
M0: 0.0
```

M1: 1.0 M2: 2.0 M3: 0.0

```
M4: 3.0
M5: 0.0
M6: 4.0
M7: 0.0
M8: 5.0
M9: 6.0
M10: 0.0
M11: 0.0
M12: 0.0
M13: 0.0
M14: 0.0
Common Data Bus:
Tag: Value:
Current Instruction in PC: ADD R5, R3, R4
Instructions To Write:
stall is now false : false
Issue cycle of ADD R5, R3, R4 is 2
CAN EXECUTE MULTIPLY MUL R3, R1, R2
Clock Cycle: 2
PC Value: 2
Reservation Stations:
Adder:
Adder position0: Tag: A1
                            Start Cycle: -1 Execute End Cycle: -1 Busy: 1 Instruction
Type: ADD Vj: Vk: 3.0 Qj: M1 Qk: A: Duration left: 4 Ready To Write: false
Adder position1: Tag: A2
                          Start Cycle: -1 Execute End Cycle: -1 Busy: 0 Instruction
                             Qk: A: Duration left: -1
                                                           Ready To Write: false
Type: None Vi:
                Vk: Qj:
Adder position2: Tag: A3
                            Start Cycle: -1 Execute End Cycle: -1 Busy: 0 Instruction
Type: None Vj: Vk: Qj:
                             Qk: A: Duration left: -1
                                                           Ready To Write: false
Multiplier:
Multiplier position0:
Tag: M1 Start Cycle: 2 Execute End Cycle: 7 Busy: 1 Instruction Type: MUL Vj: 1.0 Vk:
2.0 Qi:
         Qk:
                     Duration left: 6 Ready To Write: false
              A:
Multiplier position1:
Tag: M2 Start Cycle: -1 Execute End Cycle: -1 Busy: 0 Instruction Type: None Vj: Vk:
                 Duration left: -1 Ready To Write: false
Qi:
     Qk: A:
Load Buffers:
Load buffer position0:
Tag: L1 Busy: 0 Effective Address: -1 Start Cycle: -1 Execute End Cycle: -1 Duration left:
      Ready To Write: false
Load buffer position1:
Tag: L2 Busy: 0 Effective Address: -1 Start Cycle: -1 Execute End Cycle: -1 Duration left:
      Ready To Write: false
Load buffer position2:
Tag: L3 Busy: 0 Effective Address: -1 Start Cycle: -1 Execute End Cycle: -1 Duration left:
      Ready To Write: false
-1
Store Buffers:
```

Store buffer position0:

```
Tag: S1 Busy: 0 Effective Address: -1 Start Cycle: -1 Execute End Cycle: -1 Duration left:
-1
      Ready To Write: false
Store buffer position1:
Tag: S2 Busy: 0 Effective Address: -1 Start Cycle: -1 Execute End Cycle: -1 Duration left:
-1
      Ready To Write: false
Store buffer position2:
Tag: S3 Busy: 0 Effective Address: -1 Start Cycle: -1 Execute End Cycle: -1 Duration left:
-1
      Ready To Write: false
Register File:
R0: Tag:
             Busy: 0 Value: -1.0
             Busy: 0 Value: 1.0
R1: Tag:
             Busy: 0 Value: 2.0
R2: Tag:
R3: Tag: M1
               Busy: 1 Value: -1.0
R4: Tag:
             Busy: 0 Value: 3.0
              Busy: 1 Value: -1.0
R5: Tag: A1
R6: Tag:
             Busy: 0 Value: 4.0
R7: Tag:
             Busy: 0 Value: -1.0
R8: Tag:
             Busy: 0 Value: 5.0
R9: Tag:
             Busy: 0 Value: 6.0
R10: Tag:
             Busy: 0 Value: -1.0
R11: Tag:
             Busy: 0 Value: -1.0
R12: Tag:
             Busy: 0 Value: -1.0
R13: Tag:
             Busy: 0 Value: -1.0
R14: Tag:
             Busy: 0 Value: -1.0
Memory:
M0: 0.0
M1: 1.0
M2: 2.0
M3: 0.0
M4: 3.0
M5: 0.0
M6: 4.0
M7: 0.0
M8: 5.0
M9: 6.0
M10: 0.0
M11: 0.0
M12: 0.0
M13: 0.0
M14: 0.0
Common Data Bus:
Tag: Value:
Current Instruction in PC: ADD R7, R2, R6
Instructions To Write:
```

Clock Cycle: 3

stall is now false: false

Issue cycle of ADD R7, R2, R6 is 3

PC Value: 3

Reservation Stations:

Adder:

Adder position0: Tag: A1 Start Cycle: -1 Execute End Cycle: -1 Busy: 1 Instruction

Type: ADD Vj: Vk: 3.0 Qj: M1 Qk: A: Duration left: 4 Ready To Write: false

Adder position1: Tag: A2 Start Cycle: -1 Execute End Cycle: -1 Busy: 1 Instruction

Type: ADD Vj: 2.0 Vk: 4.0 Qj: Qk: A: Duration left: 4 Ready To Write: false

Adder position2: Tag: A3 Start Cycle: -1 Execute End Cycle: -1 Busy: 0 Instruction

Type: None Vj: Vk: Qj: Qk: A: Duration left: -1 Ready To Write: false

Multiplier:

Multiplier position0:

Tag: M1 Start Cycle: 2 Execute End Cycle: 7 Busy: 1 Instruction Type: MUL Vj: 1.0 Vk:

2.0 Qj: Qk: A: Duration left: 5 Ready To Write: false

Multiplier position1:

Tag: M2 Start Cycle: -1 Execute End Cycle: -1 Busy: 0 Instruction Type: None Vj: Vk:

Qi: Qk: A: Duration left: -1 Ready To Write: false

Load Buffers:

Load buffer position0:

Tag: L1 Busy: 0 Effective Address: -1 Start Cycle: -1 Execute End Cycle: -1 Duration left:

-1 Ready To Write: false

Load buffer position1:

Tag: L2 Busy: 0 Effective Address: -1 Start Cycle: -1 Execute End Cycle: -1 Duration left:

-1 Ready To Write: false

Load buffer position2:

Tag: L3 Busy: 0 Effective Address: -1 Start Cycle: -1 Execute End Cycle: -1 Duration left:

-1 Ready To Write: false

Store Buffers:

Store buffer position0:

Tag: S1 Busy: 0 Effective Address: -1 Start Cycle: -1 Execute End Cycle: -1 Duration left:

-1 Ready To Write: false

Store buffer position1:

Tag: S2 Busy: 0 Effective Address: -1 Start Cycle: -1 Execute End Cycle: -1 Duration left:

-1 Ready To Write: false

Store buffer position2:

Tag: S3 Busy: 0 Effective Address: -1 Start Cycle: -1 Execute End Cycle: -1 Duration left:

-1 Ready To Write: false

Register File:

R0: Tag: Busy: 0 Value: -1.0

R1: Tag: Busy: 0 Value: 1.0

R2: Tag: Busy: 0 Value: 2.0

R3: Tag: M1 Busy: 1 Value: -1.0

R4: Tag: Busy: 0 Value: 3.0

R5: Tag: A1 Busy: 1 Value: -1.0

R6: Tag: Busy: 0 Value: 4.0

R7: Tag: A2 Busy: 1 Value: -1.0

R8: Tag: Busy: 0 Value: 5.0

R9: Tag: Busy: 0 Value: 6.0

R10: Tag: Busy: 0 Value: -1.0

```
R11: Tag:
             Busy: 0 Value: -1.0
R12: Tag:
             Busy: 0 Value: -1.0
R13: Tag:
             Busy: 0 Value: -1.0
             Busy: 0 Value: -1.0
R14: Tag:
Memory:
M0: 0.0
M1: 1.0
M2: 2.0
M3: 0.0
M4: 3.0
M5: 0.0
M6: 4.0
M7: 0.0
M8: 5.0
M9: 6.0
M10: 0.0
M11: 0.0
M12: 0.0
M13: 0.0
M14: 0.0
Common Data Bus:
Tag: Value:
Current Instruction in PC: ADD R10, R8, R9
Instructions To Write:
stall is now false : false
Issue cycle of ADD R10, R8, R9 is 4
Clock Cycle: 4
PC Value: 4
Reservation Stations:
Adder:
                            Start Cycle: -1 Execute End Cycle: -1 Busy: 1 Instruction
Adder position0: Tag: A1
Type: ADD Vj: Vk: 3.0 Qj: M1 Qk: A: Duration left: 4 Ready To Write: false
Adder position1: Tag: A2
                            Start Cycle: 4 Execute End Cycle: 7 Busy: 1 Instruction
Type: ADD Vj: 2.0 Vk: 4.0 Qj:
                                Qk: A: Duration left: 4 Ready To Write: false
                            Start Cycle: -1 Execute End Cycle: -1 Busy: 1 Instruction
Adder position2: Tag: A3
Type: ADD Vj: 5.0 Vk: 6.0 Qj: Qk: A: Duration left: 4 Ready To Write: false
Multiplier:
Multiplier position0:
Tag: M1 Start Cycle: 2 Execute End Cycle: 7 Busy: 1 Instruction Type: MUL Vj: 1.0 Vk:
                     Duration left: 4 Ready To Write: false
2.0 Qj:
        Qk:
             A:
Multiplier position1:
Tag: M2 Start Cycle: -1 Execute End Cycle: -1 Busy: 0 Instruction Type: None Vj: Vk:
                 Duration left: -1 Ready To Write: false
     Qk: A:
Load Buffers:
Load buffer position0:
Tag: L1 Busy: 0 Effective Address: -1 Start Cycle: -1 Execute End Cycle: -1 Duration left:
```

-1

Ready To Write: false

```
Load buffer position1:
Tag: L2 Busy: 0 Effective Address: -1 Start Cycle: -1 Execute End Cycle: -1 Duration left:
      Ready To Write: false
Load buffer position2:
Tag: L3 Busy: 0 Effective Address: -1 Start Cycle: -1 Execute End Cycle: -1 Duration left:
      Ready To Write: false
Store Buffers:
Store buffer position0:
Tag: S1 Busy: 0 Effective Address: -1 Start Cycle: -1 Execute End Cycle: -1 Duration left:
-1
      Ready To Write: false
Store buffer position1:
Tag: S2 Busy: 0 Effective Address: -1 Start Cycle: -1 Execute End Cycle: -1 Duration left:
-1
      Ready To Write: false
Store buffer position2:
Tag: S3 Busy: 0 Effective Address: -1 Start Cycle: -1 Execute End Cycle: -1 Duration left:
      Ready To Write: false
-1
Register File:
R0: Tag:
             Busy: 0 Value: -1.0
R1: Tag:
             Busy: 0 Value: 1.0
R2: Tag:
             Busy: 0 Value: 2.0
              Busy: 1 Value: -1.0
R3: Tag: M1
R4: Tag:
             Busy: 0 Value: 3.0
R5: Tag: A1
              Busy: 1 Value: -1.0
R6: Tag:
             Busy: 0 Value: 4.0
R7: Tag: A2
              Busy: 1 Value: -1.0
R8: Tag:
             Busy: 0 Value: 5.0
             Busy: 0 Value: 6.0
R9: Tag:
R10: Tag: A3 Busy: 1 Value: -1.0
R11: Tag:
             Busy: 0 Value: -1.0
             Busy: 0 Value: -1.0
R12: Tag:
R13: Tag:
             Busy: 0 Value: -1.0
             Busy: 0 Value: -1.0
R14: Tag:
Memory:
M0: 0.0
M1: 1.0
M2: 2.0
M3: 0.0
M4: 3.0
M5: 0.0
M6: 4.0
M7: 0.0
M8: 5.0
M9: 6.0
```

M10: 0.0 M11: 0.0 M12: 0.0 M13: 0.0 M14: 0.0 Common Data Bus:

Tag: Value:

Current Instruction in PC: MUL R11, R7, R10

Instructions To Write:

\_\_\_\_\_

stall is now false : false

Issue cycle of MUL R11, R7, R10 is 5

Clock Cycle: 5 PC Value: 5

**Reservation Stations:** 

Adder:

Adder position0: Tag: A1 Start Cycle: -1 Execute End Cycle: -1 Busy: 1 Instruction

Type: ADD Vj: Vk: 3.0 Qj: M1 Qk: A: Duration left: 4 Ready To Write: false

Adder position1: Tag: A2 Start Cycle: 4 Execute End Cycle: 7 Busy: 1 Instruction

Type: ADD Vj: 2.0 Vk: 4.0 Qj: Qk: A: Duration left: 3 Ready To Write: false

Adder position2: Tag: A3 Start Cycle: 5 Execute End Cycle: 8 Busy: 1 Instruction

Type: ADD Vj: 5.0 Vk: 6.0 Qj: Qk: A: Duration left: 4 Ready To Write: false

Multiplier:

Multiplier position0:

Tag: M1 Start Cycle: 2 Execute End Cycle: 7 Busy: 1 Instruction Type: MUL Vj: 1.0 Vk:

2.0 Qj: Qk: A: Duration left: 3 Ready To Write: false

Multiplier position1:

Tag: M2 Start Cycle: -1 Execute End Cycle: -1 Busy: 1 Instruction Type: MUL Vj: Vk:

Qi: A2 Qk: A3 A: Duration left: 6 Ready To Write: false

Load Buffers:

Load buffer position0:

Tag: L1 Busy: 0 Effective Address: -1 Start Cycle: -1 Execute End Cycle: -1 Duration left:

-1 Ready To Write: false

Load buffer position1:

Tag: L2 Busy: 0 Effective Address: -1 Start Cycle: -1 Execute End Cycle: -1 Duration left:

-1 Ready To Write: false

Load buffer position2:

Tag: L3 Busy: 0 Effective Address: -1 Start Cycle: -1 Execute End Cycle: -1 Duration left:

-1 Ready To Write: false

Store Buffers:

Store buffer position0:

Tag: S1 Busy: 0 Effective Address: -1 Start Cycle: -1 Execute End Cycle: -1 Duration left:

-1 Ready To Write: false

Store buffer position1:

Tag: S2 Busy: 0 Effective Address: -1 Start Cycle: -1 Execute End Cycle: -1 Duration left:

-1 Ready To Write: false

Store buffer position2:

Tag: S3 Busy: 0 Effective Address: -1 Start Cycle: -1 Execute End Cycle: -1 Duration left:

-1 Ready To Write: false

Register File:

R0: Tag: Busy: 0 Value: -1.0 R1: Tag: Busy: 0 Value: 1.0

R2: Tag: Busy: 0 Value: 2.0

```
R3: Tag: M1
              Busy: 1 Value: -1.0
R4: Tag:
            Busy: 0 Value: 3.0
              Busy: 1 Value: -1.0
R5: Tag: A1
R6: Tag:
            Busy: 0 Value: 4.0
R7: Tag: A2
              Busy: 1 Value: -1.0
            Busy: 0 Value: 5.0
R8: Tag:
            Busy: 0 Value: 6.0
R9: Tag:
R10: Tag: A3 Busy: 1 Value: -1.0
R11: Tag: M2 Busy: 1 Value: -1.0
R12: Tag:
             Busy: 0 Value: -1.0
             Busy: 0 Value: -1.0
R13: Tag:
             Busy: 0 Value: -1.0
R14: Tag:
Memory:
M0: 0.0
M1: 1.0
M2: 2.0
M3: 0.0
M4: 3.0
M5: 0.0
M6: 4.0
M7: 0.0
M8: 5.0
M9: 6.0
M10: 0.0
M11: 0.0
M12: 0.0
M13: 0.0
M14: 0.0
Common Data Bus:
Tag: Value:
Current Instruction in PC: ADD R5, R5, R11
Instructions To Write:
-----Stall due to Issue-----
STALL
Clock Cycle: 6
PC Value: 5
Reservation Stations:
Adder:
                            Start Cycle: -1 Execute End Cycle: -1 Busy: 1 Instruction
Adder position0: Tag: A1
Type: ADD Vj: Vk: 3.0 Qj: M1 Qk: A: Duration left: 4 Ready To Write: false
Adder position1: Tag: A2
                           Start Cycle: 4 Execute End Cycle: 7 Busy: 1 Instruction
Type: ADD Vj: 2.0 Vk: 4.0 Qj:
                                     A: Duration left: 2 Ready To Write: false
                               Qk:
Adder position2: Tag: A3
                           Start Cycle: 5 Execute End Cycle: 8 Busy: 1 Instruction
Type: ADD Vj: 5.0 Vk: 6.0 Qj: Qk: A: Duration left: 3 Ready To Write: false
Multiplier:
```

Multiplier position0:

```
Tag: M1 Start Cycle: 2 Execute End Cycle: 7 Busy: 1 Instruction Type: MUL Vj: 1.0 Vk:
2.0 Qj:
         Qk:
                A:
                     Duration left: 2 Ready To Write: false
Multiplier position1:
Tag: M2 Start Cycle: -1 Execute End Cycle: -1 Busy: 1 Instruction Type: MUL Vj:
                                                                                   Vk:
Qj: A2 Qk: A3 A:
                     Duration left: 6 Ready To Write: false
Load Buffers:
Load buffer position0:
Tag: L1 Busy: 0 Effective Address: -1 Start Cycle: -1 Execute End Cycle: -1 Duration left:
      Ready To Write: false
Load buffer position1:
Tag: L2 Busy: 0 Effective Address: -1 Start Cycle: -1 Execute End Cycle: -1 Duration left:
      Ready To Write: false
Load buffer position2:
Tag: L3 Busy: 0 Effective Address: -1 Start Cycle: -1 Execute End Cycle: -1 Duration left:
      Ready To Write: false
Store Buffers:
Store buffer position0:
Tag: S1 Busy: 0 Effective Address: -1 Start Cycle: -1 Execute End Cycle: -1 Duration left:
      Ready To Write: false
-1
Store buffer position1:
Tag: S2 Busy: 0 Effective Address: -1 Start Cycle: -1 Execute End Cycle: -1 Duration left:
-1
      Ready To Write: false
Store buffer position2:
Tag: S3 Busy: 0 Effective Address: -1 Start Cycle: -1 Execute End Cycle: -1 Duration left:
-1
      Ready To Write: false
Register File:
R0: Tag:
             Busy: 0 Value: -1.0
R1: Tag:
             Busy: 0 Value: 1.0
R2: Tag:
             Busy: 0 Value: 2.0
R3: Tag: M1
              Busy: 1 Value: -1.0
             Busy: 0 Value: 3.0
R4: Tag:
R5: Tag: A1
              Busy: 1 Value: -1.0
R6: Tag:
             Busy: 0 Value: 4.0
R7: Tag: A2
              Busy: 1 Value: -1.0
R8: Tag:
             Busy: 0 Value: 5.0
R9: Tag:
             Busy: 0 Value: 6.0
R10: Tag: A3 Busy: 1 Value: -1.0
R11: Tag: M2 Busy: 1 Value: -1.0
R12: Tag:
             Busy: 0 Value: -1.0
R13: Tag:
             Busy: 0 Value: -1.0
R14: Tag:
             Busy: 0 Value: -1.0
Memory:
M0: 0.0
M1: 1.0
M2: 2.0
M3: 0.0
M4: 3.0
```

M5: 0.0

```
M6: 4.0
M7: 0.0
M8: 5.0
M9: 6.0
M10: 0.0
M11: 0.0
M12: 0.0
M13: 0.0
M14: 0.0
Common Data Bus:
Tag: Value:
Current Instruction in PC: ADD R5, R5, R11
Instructions To Write:
-----Stall due to Issue-----
STALL
Clock Cycle: 7
PC Value: 5
Reservation Stations:
Adder:
Adder position0: Tag: A1
                            Start Cycle: -1 Execute End Cycle: -1 Busy: 1 Instruction
Type: ADD Vj: Vk: 3.0 Qj: M1 Qk: A: Duration left: 4 Ready To Write: false
Adder position1: Tag: A2
                            Start Cycle: 4 Execute End Cycle: 7 Busy: 1 Instruction
Type: ADD Vj: 2.0 Vk: 4.0 Qj: Qk: A: Duration left: 1 Ready To Write: true
Adder position2: Tag: A3
                            Start Cycle: 5 Execute End Cycle: 8 Busy: 1 Instruction
Type: ADD Vj: 5.0 Vk: 6.0 Qj: Qk: A: Duration left: 2 Ready To Write: false
Multiplier:
Multiplier position0:
Tag: M1 Start Cycle: 2 Execute End Cycle: 7 Busy: 1 Instruction Type: MUL Vj: 1.0 Vk:
2.0 Qi:
                     Duration left: 1 Ready To Write: true
         Qk:
              A:
Multiplier position1:
Tag: M2 Start Cycle: -1 Execute End Cycle: -1 Busy: 1 Instruction Type: MUL Vj: Vk:
                    Duration left: 6 Ready To Write: false
Qi: A2 Qk: A3 A:
Load Buffers:
Load buffer position0:
Tag: L1 Busy: 0 Effective Address: -1 Start Cycle: -1 Execute End Cycle: -1 Duration left:
      Ready To Write: false
-1
Load buffer position1:
Tag: L2 Busy: 0 Effective Address: -1 Start Cycle: -1 Execute End Cycle: -1 Duration left:
      Ready To Write: false
Load buffer position2:
Tag: L3 Busy: 0 Effective Address: -1 Start Cycle: -1 Execute End Cycle: -1 Duration left:
      Ready To Write: false
-1
Store Buffers:
Store buffer position0:
Tag: S1 Busy: 0 Effective Address: -1 Start Cycle: -1 Execute End Cycle: -1 Duration left:
```

-1

Ready To Write: false

Store buffer position1:

```
Tag: S2 Busy: 0 Effective Address: -1 Start Cycle: -1 Execute End Cycle: -1 Duration left:
-1
      Ready To Write: false
Store buffer position2:
Tag: S3 Busy: 0 Effective Address: -1 Start Cycle: -1 Execute End Cycle: -1 Duration left:
-1
     Ready To Write: false
Register File:
R0: Tag:
            Busy: 0 Value: -1.0
R1: Tag:
            Busy: 0 Value: 1.0
R2: Tag:
            Busy: 0 Value: 2.0
R3: Tag: M1
              Busy: 1 Value: -1.0
R4: Tag:
            Busy: 0 Value: 3.0
             Busy: 1 Value: -1.0
R5: Tag: A1
R6: Tag:
            Busy: 0 Value: 4.0
R7: Tag: A2 Busy: 1 Value: -1.0
            Busy: 0 Value: 5.0
R8: Tag:
            Busy: 0 Value: 6.0
R9: Tag:
R10: Tag: A3 Busy: 1 Value: -1.0
R11: Tag: M2 Busy: 1 Value: -1.0
            Busy: 0 Value: -1.0
R12: Tag:
R13: Tag:
            Busy: 0 Value: -1.0
R14: Tag:
            Busy: 0 Value: -1.0
Memory:
M0: 0.0
M1: 1.0
M2: 2.0
M3: 0.0
M4: 3.0
M5: 0.0
M6: 4.0
M7: 0.0
M8: 5.0
M9: 6.0
M10: 0.0
M11: 0.0
M12: 0.0
M13: 0.0
M14: 0.0
Common Data Bus:
Tag: Value:
Current Instruction in PC: ADD R5, R5, R11
Instructions To Write:
MUL R3, R1, R2
ADD R7, R2, R6
_____
-----Stall due to Issue-----
STALL
```

Instruction to be written: MUL R3, R1, R2

Clock Cycle: 8

PC Value: 5

Reservation Stations:

Adder:

Adder position0: Tag: A1 Start Cycle: -1 Execute End Cycle: -1 Busy: 1 Instruction

Type: ADD Vj: 2.0 Vk: 3.0 Qj: Qk: A: Duration left: 4 Ready To Write: false

Adder position1: Tag: A2 Start Cycle: 4 Execute End Cycle: 7 Busy: 1 Instruction

Type: ADD Vj: 2.0 Vk: 4.0 Qj: Qk: A: Duration left: 1 Ready To Write: true

Adder position2: Tag: A3 Start Cycle: 5 Execute End Cycle: 8 Busy: 1 Instruction

Type: ADD Vj: 5.0 Vk: 6.0 Qj: Qk: A: Duration left: 1 Ready To Write: true

Multiplier:

Multiplier position0:

Tag: M1 Start Cycle: -1 Execute End Cycle: -1 Busy: 0 Instruction Type: None Vj: Vk:

Qj: Qk: A: Duration left: -1 Ready To Write: false

Multiplier position1:

Tag: M2 Start Cycle: -1 Execute End Cycle: -1 Busy: 1 Instruction Type: MUL Vj: Vk:

Qj: A2 Qk: A3 A: Duration left: 6 Ready To Write: false

Load Buffers:

Load buffer position0:

Tag: L1 Busy: 0 Effective Address: -1 Start Cycle: -1 Execute End Cycle: -1 Duration left:

-1 Ready To Write: false

Load buffer position1:

Tag: L2 Busy: 0 Effective Address: -1 Start Cycle: -1 Execute End Cycle: -1 Duration left:

-1 Ready To Write: false

Load buffer position2:

Tag: L3 Busy: 0 Effective Address: -1 Start Cycle: -1 Execute End Cycle: -1 Duration left:

-1 Ready To Write: false

Store Buffers:

Store buffer position0:

Tag: S1 Busy: 0 Effective Address: -1 Start Cycle: -1 Execute End Cycle: -1 Duration left:

-1 Ready To Write: false

Store buffer position1:

Tag: S2 Busy: 0 Effective Address: -1 Start Cycle: -1 Execute End Cycle: -1 Duration left:

-1 Ready To Write: false

Store buffer position2:

Tag: S3 Busy: 0 Effective Address: -1 Start Cycle: -1 Execute End Cycle: -1 Duration left:

-1 Ready To Write: false

Register File:

R0: Tag: Busy: 0 Value: -1.0

R1: Tag: Busy: 0 Value: 1.0

R2: Tag: Busy: 0 Value: 2.0

R3: Tag: Busy: 0 Value: 2.0

R4: Tag: Busy: 0 Value: 3.0

R5: Tag: A1 Busy: 1 Value: -1.0

R6: Tag: Busy: 0 Value: 4.0

R7: Tag: A2 Busy: 1 Value: -1.0

R8: Tag: Busy: 0 Value: 5.0

R9: Tag: Busy: 0 Value: 6.0

R10: Tag: A3 Busy: 1 Value: -1.0

```
R11: Tag: M2 Busy: 1 Value: -1.0
R12: Tag:
             Busy: 0 Value: -1.0
             Busy: 0 Value: -1.0
R13: Tag:
             Busy: 0 Value: -1.0
R14: Tag:
Memory:
M0: 0.0
M1: 1.0
M2: 2.0
M3: 0.0
M4: 3.0
M5: 0.0
M6: 4.0
M7: 0.0
M8: 5.0
M9: 6.0
M10: 0.0
M11: 0.0
M12: 0.0
M13: 0.0
M14: 0.0
Common Data Bus:
Tag: M1 Value: 2.0
Current Instruction in PC: ADD R5, R5, R11
Instructions To Write:
ADD R7, R2, R6
ADD R10, R8, R9
-----Stall due to Issue-----
Instruction to be written: ADD R7, R2, R6
Clock Cycle: 9
PC Value: 5
Reservation Stations:
Adder:
Adder position0: Tag: A1
                           Start Cycle: 9 Execute End Cycle: 12 Busy: 1 Instruction
Type: ADD Vj: 2.0 Vk: 3.0 Qj: Qk: A: Duration left: 4 Ready To Write: false
Adder position1: Tag: A2
                           Start Cycle: -1 Execute End Cycle: -1 Busy: 0 Instruction
Type: None Vj: Vk: Qj: Qk: A: Duration left: -1
                                                        Ready To Write: false
Adder position2: Tag: A3
                           Start Cycle: 5 Execute End Cycle: 8 Busy: 1 Instruction
Type: ADD Vj: 5.0 Vk: 6.0 Qj: Qk: A: Duration left: 1 Ready To Write: true
Multiplier:
Multiplier position0:
Tag: M1 Start Cycle: -1 Execute End Cycle: -1 Busy: 0 Instruction Type: None Vj: Vk:
                 Duration left: -1 Ready To Write: false
Multiplier position1:
Tag: M2 Start Cycle: -1 Execute End Cycle: -1 Busy: 1 Instruction Type: MUL Vj: 6.0 Vk:
     Qk: A3 A: Duration left: 6 Ready To Write: false
Qj:
```

Load Buffers:

```
Load buffer position0:
Tag: L1 Busy: 0 Effective Address: -1 Start Cycle: -1 Execute End Cycle: -1 Duration left:
      Ready To Write: false
Load buffer position1:
Tag: L2 Busy: 0 Effective Address: -1 Start Cycle: -1 Execute End Cycle: -1 Duration left:
      Ready To Write: false
Load buffer position2:
Tag: L3 Busy: 0 Effective Address: -1 Start Cycle: -1 Execute End Cycle: -1 Duration left:
      Ready To Write: false
Store Buffers:
Store buffer position0:
Tag: S1 Busy: 0 Effective Address: -1 Start Cycle: -1 Execute End Cycle: -1 Duration left:
-1
      Ready To Write: false
Store buffer position1:
Tag: S2 Busy: 0 Effective Address: -1 Start Cycle: -1 Execute End Cycle: -1 Duration left:
      Ready To Write: false
-1
Store buffer position2:
Tag: S3 Busy: 0 Effective Address: -1 Start Cycle: -1 Execute End Cycle: -1 Duration left:
-1
      Ready To Write: false
Register File:
             Busy: 0 Value: -1.0
R0: Tag:
R1: Tag:
             Busy: 0 Value: 1.0
R2: Tag:
             Busy: 0 Value: 2.0
R3: Tag:
             Busy: 0 Value: 2.0
R4: Tag:
             Busy: 0 Value: 3.0
R5: Tag: A1
               Busy: 1 Value: -1.0
             Busy: 0 Value: 4.0
R6: Tag:
R7: Tag:
             Busy: 0 Value: 6.0
R8: Tag:
             Busy: 0 Value: 5.0
             Busy: 0 Value: 6.0
R9: Tag:
R10: Tag: A3 Busy: 1 Value: -1.0
R11: Tag: M2 Busy: 1 Value: -1.0
R12: Tag:
             Busy: 0 Value: -1.0
R13: Tag:
             Busy: 0 Value: -1.0
R14: Tag:
             Busy: 0 Value: -1.0
Memory:
M0: 0.0
M1: 1.0
M2: 2.0
M3: 0.0
M4: 3.0
M5: 0.0
M6: 4.0
```

M7: 0.0 M8: 5.0 M9: 6.0 M10: 0.0 M11: 0.0 M12: 0.0 M13: 0.0 M14: 0.0

Common Data Bus: Tag: A2 Value: 6.0

Current Instruction in PC: ADD R5, R5, R11

Instructions To Write: ADD R10, R8, R9

\_\_\_\_\_

stall is now false : false

Issue cycle of ADD R5, R5, R11 is 10 Instruction to be written: ADD R10, R8, R9

Clock Cycle: 10 PC Value: 6

**Reservation Stations:** 

Adder:

Adder position0: Tag: A1 Start Cycle: 9 Execute End Cycle: 12 Busy: 1 Instruction

Type: ADD Vj: 2.0 Vk: 3.0 Qj: Qk: A: Duration left: 3 Ready To Write: false

Adder position1: Tag: A2 Start Cycle: -1 Execute End Cycle: -1 Busy: 1 Instruction

Type: ADD Vj: Vk: Qj: A1 Qk: M2 A: Duration left: 4 Ready To Write: false

Adder position2: Tag: A3 Start Cycle: -1 Execute End Cycle: -1 Busy: 0 Instruction Type: None Vj: Vk: Qj: Qk: A: Duration left: -1 Ready To Write: false

Multiplier:

Multiplier position0:

Tag: M1 Start Cycle: -1 Execute End Cycle: -1 Busy: 0 Instruction Type: None Vj: Vk:

Qj: Qk: A: Duration left: -1 Ready To Write: false

Multiplier position1:

Tag: M2 Start Cycle: -1 Execute End Cycle: -1 Busy: 1 Instruction Type: MUL Vj: 6.0 Vk:

11.0 Qj: Qk: A: Duration left: 6 Ready To Write: false

Load Buffers:

Load buffer position0:

Tag: L1 Busy: 0 Effective Address: -1 Start Cycle: -1 Execute End Cycle: -1 Duration left:

-1 Ready To Write: false

Load buffer position1:

Tag: L2 Busy: 0 Effective Address: -1 Start Cycle: -1 Execute End Cycle: -1 Duration left:

-1 Ready To Write: false

Load buffer position2:

Tag: L3 Busy: 0 Effective Address: -1 Start Cycle: -1 Execute End Cycle: -1 Duration left:

-1 Ready To Write: false

Store Buffers:

Store buffer position0:

Tag: S1 Busy: 0 Effective Address: -1 Start Cycle: -1 Execute End Cycle: -1 Duration left:

-1 Ready To Write: false

Store buffer position1:

Tag: S2 Busy: 0 Effective Address: -1 Start Cycle: -1 Execute End Cycle: -1 Duration left:

-1 Ready To Write: false

Store buffer position2:

```
Tag: S3 Busy: 0 Effective Address: -1 Start Cycle: -1 Execute End Cycle: -1 Duration left:
-1
      Ready To Write: false
Register File:
R0: Tag:
            Busy: 0 Value: -1.0
R1: Tag:
             Busy: 0 Value: 1.0
R2: Tag:
             Busy: 0 Value: 2.0
R3: Tag:
             Busy: 0 Value: 2.0
R4: Tag:
             Busy: 0 Value: 3.0
R5: Tag: A2
              Busy: 1 Value: -1.0
             Busy: 0 Value: 4.0
R6: Tag:
R7: Tag:
             Busy: 0 Value: 6.0
             Busy: 0 Value: 5.0
R8: Tag:
R9: Tag:
             Busy: 0 Value: 6.0
R10: Tag:
             Busy: 0 Value: 11.0
R11: Tag: M2 Busy: 1 Value: -1.0
             Busy: 0 Value: -1.0
R12: Tag:
R13: Tag:
             Busy: 0 Value: -1.0
R14: Tag:
             Busy: 0 Value: -1.0
Memory:
M0: 0.0
M1: 1.0
M2: 2.0
M3: 0.0
M4: 3.0
M5: 0.0
M6: 4.0
M7: 0.0
M8: 5.0
M9: 6.0
M10: 0.0
M11: 0.0
M12: 0.0
M13: 0.0
M14: 0.0
Common Data Bus:
Tag: A3 Value: 11.0
Instructions To Write:
CAN EXECUTE MULTIPLY MUL R11, R7, R10
Clock Cycle: 11
PC Value: 6
Reservation Stations:
Adder:
Adder position0: Tag: A1
                            Start Cycle: 9 Execute End Cycle: 12 Busy: 1 Instruction
Type: ADD Vj: 2.0 Vk: 3.0 Qj:
                                Qk:
                                      A: Duration left: 2 Ready To Write: false
Adder position1: Tag: A2
                            Start Cycle: -1 Execute End Cycle: -1 Busy: 1 Instruction
```

Type: ADD Vj: Vk: Qj: A1 Qk: M2 A: Duration left: 4 Ready To Write: false

Adder position2: Tag: A3 Start Cycle: -1 Execute End Cycle: -1 Busy: 0 Instruction Type: None Vj: Vk: Qj: Qk: A: Duration left: -1 Ready To Write: false Multiplier: Multiplier position0: Tag: M1 Start Cycle: -1 Execute End Cycle: -1 Busy: 0 Instruction Type: None Vj: Vk: Qj: Qk: A: Duration left: -1 Ready To Write: false Multiplier position1:

Tag: M2 Start Cycle: 11 Execute End Cycle: 16 Busy: 1 Instruction Type: MUL Vj: 6.0 Vk: 11.0 Qj: Qk: A: Duration left: 6 Ready To Write: false

Load Buffers:

Load buffer position0:

Tag: L1 Busy: 0 Effective Address: -1 Start Cycle: -1 Execute End Cycle: -1 Duration left: -1 Ready To Write: false

Load buffer position1:

Tag: L2 Busy: 0 Effective Address: -1 Start Cycle: -1 Execute End Cycle: -1 Duration left: -1 Ready To Write: false

Load buffer position2:

Tag: L3 Busy: 0 Effective Address: -1 Start Cycle: -1 Execute End Cycle: -1 Duration left:

-1 Ready To Write: false

Store Buffers:

Store buffer position0:

Tag: S1 Busy: 0 Effective Address: -1 Start Cycle: -1 Execute End Cycle: -1 Duration left:

-1 Ready To Write: false

Store buffer position1:

Tag: S2 Busy: 0 Effective Address: -1 Start Cycle: -1 Execute End Cycle: -1 Duration left:

-1 Ready To Write: false

Store buffer position2:

Tag: S3 Busy: 0 Effective Address: -1 Start Cycle: -1 Execute End Cycle: -1 Duration left:

-1 Ready To Write: false

Register File:

R0: Tag: Busy: 0 Value: -1.0 R1: Tag: Busy: 0 Value: 1.0 R2: Tag: Busy: 0 Value: 2.0 R3: Tag: Busy: 0 Value: 2.0 R4: Tag: Busy: 0 Value: 3.0 R5: Tag: A2 Busy: 1 Value: -1.0 Busy: 0 Value: 4.0 R6: Tag: R7: Tag: Busy: 0 Value: 6.0 R8: Tag: Busy: 0 Value: 5.0 R9: Tag: Busy: 0 Value: 6.0 R10: Tag: Busy: 0 Value: 11.0 R11: Tag: M2 Busy: 1 Value: -1.0 R12: Tag: Busy: 0 Value: -1.0 R13: Tag: Busy: 0 Value: -1.0 R14: Tag: Busy: 0 Value: -1.0

Memory: M0: 0.0 M1: 1.0

```
M2: 2.0
M3: 0.0
M4: 3.0
M5: 0.0
M6: 4.0
M7: 0.0
M8: 5.0
M9: 6.0
M10: 0.0
M11: 0.0
M12: 0.0
M13: 0.0
M14: 0.0
Common Data Bus:
Tag: A3 Value: 11.0
Instructions To Write:
Clock Cycle: 12
PC Value: 6
Reservation Stations:
Adder:
                            Start Cycle: 9 Execute End Cycle: 12 Busy: 1 Instruction
Adder position0: Tag: A1
Type: ADD Vj: 2.0 Vk: 3.0 Qj:
                                Qk: A: Duration left: 1 Ready To Write: true
Adder position1: Tag: A2
                            Start Cycle: -1 Execute End Cycle: -1 Busy: 1 Instruction
Type: ADD Vj:
                Vk:
                        Qj: A1 Qk: M2 A: Duration left: 4 Ready To Write: false
Adder position2: Tag: A3
                            Start Cycle: -1 Execute End Cycle: -1 Busy: 0 Instruction
Type: None Vi:
                Vk: Qi: Qk: A: Duration left: -1
                                                           Ready To Write: false
Multiplier:
Multiplier position0:
Tag: M1 Start Cycle: -1 Execute End Cycle: -1 Busy: 0 Instruction Type: None Vj: Vk:
     Qk:
           A:
                 Duration left: -1 Ready To Write: false
Qi:
Multiplier position1:
Tag: M2 Start Cycle: 11 Execute End Cycle: 16 Busy: 1 Instruction Type: MUL Vi: 6.0 Vk:
11.0
         Qi:
              Qk: A:
                          Duration left: 5 Ready To Write: false
Load Buffers:
Load buffer position0:
Tag: L1 Busy: 0 Effective Address: -1 Start Cycle: -1 Execute End Cycle: -1 Duration left:
      Ready To Write: false
Load buffer position1:
Tag: L2 Busy: 0 Effective Address: -1 Start Cycle: -1 Execute End Cycle: -1 Duration left:
      Ready To Write: false
Load buffer position2:
Tag: L3 Busy: 0 Effective Address: -1 Start Cycle: -1 Execute End Cycle: -1 Duration left:
-1
      Ready To Write: false
Store Buffers:
```

Tag: S1 Busy: 0 Effective Address: -1 Start Cycle: -1 Execute End Cycle: -1 Duration left:

Store buffer position0:

-1

Ready To Write: false

Store buffer position1: Tag: S2 Busy: 0 Effective Address: -1 Start Cycle: -1 Execute End Cycle: -1 Duration left: Ready To Write: false Store buffer position2: Tag: S3 Busy: 0 Effective Address: -1 Start Cycle: -1 Execute End Cycle: -1 Duration left: Ready To Write: false Register File: R0: Tag: Busy: 0 Value: -1.0 Busy: 0 Value: 1.0 R1: Tag: Busy: 0 Value: 2.0 R2: Tag: R3: Tag: Busy: 0 Value: 2.0 Busy: 0 Value: 3.0 R4: Tag: R5: Tag: A2 Busy: 1 Value: -1.0 R6: Tag: Busy: 0 Value: 4.0 R7: Tag: Busy: 0 Value: 6.0 R8: Tag: Busy: 0 Value: 5.0 R9: Tag: Busy: 0 Value: 6.0 R10: Tag: Busy: 0 Value: 11.0 R11: Tag: M2 Busy: 1 Value: -1.0 R12: Tag: Busy: 0 Value: -1.0 Busy: 0 Value: -1.0 R13: Tag: Busy: 0 Value: -1.0 R14: Tag: Memory: M0: 0.0 M1: 1.0 M2: 2.0 M3: 0.0 M4: 3.0 M5: 0.0 M6: 4.0 M7: 0.0 M8: 5.0 M9: 6.0 M10: 0.0 M11: 0.0 M12: 0.0 M13: 0.0 M14: 0.0 Common Data Bus: Tag: A3 Value: 11.0 Instructions To Write: ADD R5, R3, R4

Instruction to be written: ADD R5, R3, R4

Clock Cycle: 13 PC Value: 6

**Reservation Stations:** 

Adder:

Adder position0: Tag: A1 Start Cycle: -1 Execute End Cycle: -1 Busy: 0 Instruction Type: None Vj: Vk: Qj: Qk: A: Duration left: -1 Ready To Write: false Start Cycle: -1 Execute End Cycle: -1 Busy: 1 Instruction Adder position1: Tag: A2 Type: ADD Vj: 5.0 Vk: Qj: Qk: M2 A: Duration left: 4 Ready To Write: false Adder position2: Tag: A3 Start Cycle: -1 Execute End Cycle: -1 Busy: 0 Instruction Type: None Vj: Vk: Qj: Qk: A: Duration left: -1 Ready To Write: false Multiplier: Multiplier position0:

Tag: M1 Start Cycle: -1 Execute End Cycle: -1 Busy: 0 Instruction Type: None Vi: Vk: Duration left: -1 Ready To Write: false Multiplier position1:

Tag: M2 Start Cycle: 11 Execute End Cycle: 16 Busy: 1 Instruction Type: MUL Vi: 6.0 Vk: 11.0 Qk: A: Duration left: 4 Ready To Write: false Load Buffers:

Load buffer position0:

Tag: L1 Busy: 0 Effective Address: -1 Start Cycle: -1 Execute End Cycle: -1 Duration left: Ready To Write: false

Load buffer position1:

Tag: L2 Busy: 0 Effective Address: -1 Start Cycle: -1 Execute End Cycle: -1 Duration left: Ready To Write: false -1

Load buffer position2:

Tag: L3 Busy: 0 Effective Address: -1 Start Cycle: -1 Execute End Cycle: -1 Duration left: Ready To Write: false

Store Buffers:

Store buffer position0:

Tag: S1 Busy: 0 Effective Address: -1 Start Cycle: -1 Execute End Cycle: -1 Duration left: Ready To Write: false -1

Store buffer position1:

Tag: S2 Busy: 0 Effective Address: -1 Start Cycle: -1 Execute End Cycle: -1 Duration left: -1 Ready To Write: false

Store buffer position2:

Tag: S3 Busy: 0 Effective Address: -1 Start Cycle: -1 Execute End Cycle: -1 Duration left: -1 Ready To Write: false

Register File:

R0: Tag: Busy: 0 Value: -1.0 R1: Tag: Busy: 0 Value: 1.0 Busy: 0 Value: 2.0 R2: Tag: R3: Tag: Busy: 0 Value: 2.0 Busy: 0 Value: 3.0 R4: Tag: R5: Tag: A2 Busy: 1 Value: -1.0 Busy: 0 Value: 4.0 R6: Tag: R7: Tag: Busy: 0 Value: 6.0 R8: Tag: Busy: 0 Value: 5.0 R9: Tag: Busy: 0 Value: 6.0 R10: Tag: Busy: 0 Value: 11.0 R11: Tag: M2 Busy: 1 Value: -1.0

R12: Tag: Busy: 0 Value: -1.0 Busy: 0 Value: -1.0 R13: Tag:

```
R14: Tag:
             Busy: 0 Value: -1.0
Memory:
M0: 0.0
M1: 1.0
M2: 2.0
M3: 0.0
M4: 3.0
M5: 0.0
M6: 4.0
M7: 0.0
M8: 5.0
M9: 6.0
M10: 0.0
M11: 0.0
M12: 0.0
M13: 0.0
M14: 0.0
Common Data Bus:
Tag: A1 Value: 5.0
Instructions To Write:
Clock Cycle: 14
PC Value: 6
Reservation Stations:
Adder:
Adder position0: Tag: A1
                            Start Cycle: -1 Execute End Cycle: -1 Busy: 0 Instruction
                                    A: Duration left: -1
                                                           Ready To Write: false
Type: None Vj: Vk:
                      Qi:
                             Qk:
Adder position1: Tag: A2
                            Start Cycle: -1 Execute End Cycle: -1 Busy: 1 Instruction
Type: ADD Vj: 5.0 Vk:
                               Qk: M2 A: Duration left: 4 Ready To Write: false
                         Qi:
                            Start Cycle: -1 Execute End Cycle: -1 Busy: 0 Instruction
Adder position2: Tag: A3
Type: None Vj: Vk: Qj: Qk: A: Duration left: -1
                                                           Ready To Write: false
Multiplier:
Multiplier position0:
Tag: M1 Start Cycle: -1 Execute End Cycle: -1 Busy: 0 Instruction Type: None Vj:
     Qk:
           A:
                 Duration left: -1 Ready To Write: false
Multiplier position1:
Tag: M2 Start Cycle: 11 Execute End Cycle: 16 Busy: 1 Instruction Type: MUL Vj: 6.0 Vk:
11.0
        Qj:
              Qk: A:
                          Duration left: 3
                                          Ready To Write: false
Load Buffers:
Load buffer position0:
Tag: L1 Busy: 0 Effective Address: -1 Start Cycle: -1 Execute End Cycle: -1 Duration left:
-1
      Ready To Write: false
Load buffer position1:
Tag: L2 Busy: 0 Effective Address: -1 Start Cycle: -1 Execute End Cycle: -1 Duration left:
-1
      Ready To Write: false
Load buffer position2:
Tag: L3 Busy: 0 Effective Address: -1 Start Cycle: -1 Execute End Cycle: -1 Duration left:
      Ready To Write: false
-1
```

Store Buffers: Store buffer position0: Tag: S1 Busy: 0 Effective Address: -1 Start Cycle: -1 Execute End Cycle: -1 Duration left: -1 Ready To Write: false Store buffer position1: Tag: S2 Busy: 0 Effective Address: -1 Start Cycle: -1 Execute End Cycle: -1 Duration left: Ready To Write: false Store buffer position2: Tag: S3 Busy: 0 Effective Address: -1 Start Cycle: -1 Execute End Cycle: -1 Duration left: Ready To Write: false -1 Register File: R0: Tag: Busy: 0 Value: -1.0 R1: Tag: Busy: 0 Value: 1.0 R2: Tag: Busy: 0 Value: 2.0 Busy: 0 Value: 2.0 R3: Tag: R4: Tag: Busy: 0 Value: 3.0 R5: Tag: A2 Busy: 1 Value: -1.0 R6: Tag: Busy: 0 Value: 4.0 R7: Tag: Busy: 0 Value: 6.0 R8: Tag: Busy: 0 Value: 5.0 Busy: 0 Value: 6.0 R9: Tag: R10: Tag: Busy: 0 Value: 11.0 R11: Tag: M2 Busy: 1 Value: -1.0 R12: Tag: Busy: 0 Value: -1.0 R13: Tag: Busy: 0 Value: -1.0 R14: Tag: Busy: 0 Value: -1.0 Memory: M0: 0.0 M1: 1.0 M2: 2.0 M3: 0.0 M4: 3.0 M5: 0.0 M6: 4.0 M7: 0.0 M8: 5.0 M9: 6.0 M10: 0.0 M11: 0.0 M12: 0.0 M13: 0.0 M14: 0.0

Common Data Bus: Tag: A1 Value: 5.0 Instructions To Write:

-----

Clock Cycle: 15 PC Value: 6

Reservation Stations:

Adder:

Adder position0: Tag: A1 Start Cycle: -1 Execute End Cycle: -1 Busy: 0 Instruction Type: None Vj: Vk: Qj: Qk: A: Duration left: -1 Ready To Write: false Adder position1: Tag: A2 Start Cycle: -1 Execute End Cycle: -1 Busy: 1 Instruction Type: ADD Vj: 5.0 Vk: Qj: Qk: M2 A: Duration left: 4 Ready To Write: false Adder position2: Tag: A3 Start Cycle: -1 Execute End Cycle: -1 Busy: 0 Instruction Type: None Vj: Vk: Qj: Qk: A: Duration left: -1 Ready To Write: false

Multiplier:

Multiplier position0:

Tag: M1 Start Cycle: -1 Execute End Cycle: -1 Busy: 0 Instruction Type: None Vj: Vk: Qj: Qk: A: Duration left: -1 Ready To Write: false

Multiplier position1:

Tag: M2 Start Cycle: 11 Execute End Cycle: 16 Busy: 1 Instruction Type: MUL Vj: 6.0 Vk:

11.0 Qj: Qk: A: Duration left: 2 Ready To Write: false

Load Buffers:

Load buffer position0:

Tag: L1 Busy: 0 Effective Address: -1 Start Cycle: -1 Execute End Cycle: -1 Duration left:

-1 Ready To Write: false

Load buffer position1:

Tag: L2 Busy: 0 Effective Address: -1 Start Cycle: -1 Execute End Cycle: -1 Duration left:

-1 Ready To Write: false

Load buffer position2:

Tag: L3 Busy: 0 Effective Address: -1 Start Cycle: -1 Execute End Cycle: -1 Duration left:

-1 Ready To Write: false

Store Buffers:

Store buffer position0:

Tag: S1 Busy: 0 Effective Address: -1 Start Cycle: -1 Execute End Cycle: -1 Duration left:

-1 Ready To Write: false

Store buffer position1:

Tag: S2 Busy: 0 Effective Address: -1 Start Cycle: -1 Execute End Cycle: -1 Duration left:

-1 Ready To Write: false

Store buffer position2:

Tag: S3 Busy: 0 Effective Address: -1 Start Cycle: -1 Execute End Cycle: -1 Duration left:

-1 Ready To Write: false

Register File:

Busy: 0 Value: -1.0 R0: Tag: R1: Tag: Busy: 0 Value: 1.0 Busy: 0 Value: 2.0 R2: Tag: R3: Tag: Busy: 0 Value: 2.0 Busy: 0 Value: 3.0 R4: Tag: R5: Tag: A2 Busy: 1 Value: -1.0 R6: Tag: Busy: 0 Value: 4.0 R7: Tag: Busy: 0 Value: 6.0 R8: Tag: Busy: 0 Value: 5.0

R9: Tag: Busy: 0 Value: 6.0 R10: Tag: Busy: 0 Value: 11.0

R11: Tag: M2 Busy: 1 Value: -1.0

```
R12: Tag:
             Busy: 0 Value: -1.0
R13: Tag:
             Busy: 0 Value: -1.0
             Busy: 0 Value: -1.0
R14: Tag:
Memory:
M0: 0.0
M1: 1.0
M2: 2.0
M3: 0.0
M4: 3.0
M5: 0.0
M6: 4.0
M7: 0.0
M8: 5.0
M9: 6.0
M10: 0.0
M11: 0.0
M12: 0.0
M13: 0.0
M14: 0.0
Common Data Bus:
Tag: A1 Value: 5.0
Instructions To Write:
Clock Cycle: 16
PC Value: 6
Reservation Stations:
Adder:
Adder position0: Tag: A1
                            Start Cycle: -1 Execute End Cycle: -1 Busy: 0 Instruction
Type: None Vj: Vk: Qj:
                              Qk: A: Duration left: -1
                                                           Ready To Write: false
Adder position1: Tag: A2
                            Start Cycle: -1 Execute End Cycle: -1 Busy: 1 Instruction
Type: ADD Vj: 5.0 Vk:
                         Qi: Qk: M2 A: Duration left: 4 Ready To Write: false
Adder position2: Tag: A3
                            Start Cycle: -1 Execute End Cycle: -1 Busy: 0 Instruction
Type: None Vj: Vk: Qj: Qk: A: Duration left: -1
                                                           Ready To Write: false
Multiplier:
Multiplier position0:
Tag: M1 Start Cycle: -1 Execute End Cycle: -1 Busy: 0 Instruction Type: None Vj:
                 Duration left: -1 Ready To Write: false
Qj:
     Qk: A:
Multiplier position1:
Tag: M2 Start Cycle: 11 Execute End Cycle: 16 Busy: 1 Instruction Type: MUL Vi: 6.0 Vk:
11.0
         Qj:
              Qk: A:
                          Duration left: 1
                                          Ready To Write: true
Load Buffers:
Load buffer position0:
Tag: L1 Busy: 0 Effective Address: -1 Start Cycle: -1 Execute End Cycle: -1 Duration left:
      Ready To Write: false
Load buffer position1:
Tag: L2 Busy: 0 Effective Address: -1 Start Cycle: -1 Execute End Cycle: -1 Duration left:
```

-1

Ready To Write: false

Load buffer position2:

```
Tag: L3 Busy: 0 Effective Address: -1 Start Cycle: -1 Execute End Cycle: -1 Duration left:
-1
      Ready To Write: false
Store Buffers:
Store buffer position0:
Tag: S1 Busy: 0 Effective Address: -1 Start Cycle: -1 Execute End Cycle: -1 Duration left:
      Ready To Write: false
Store buffer position1:
Tag: S2 Busy: 0 Effective Address: -1 Start Cycle: -1 Execute End Cycle: -1 Duration left:
      Ready To Write: false
Store buffer position2:
Tag: S3 Busy: 0 Effective Address: -1 Start Cycle: -1 Execute End Cycle: -1 Duration left:
      Ready To Write: false
Register File:
R0: Tag:
             Busy: 0 Value: -1.0
R1: Tag:
             Busy: 0 Value: 1.0
R2: Tag:
             Busy: 0 Value: 2.0
R3: Tag:
             Busy: 0 Value: 2.0
R4: Tag:
             Busy: 0 Value: 3.0
              Busy: 1 Value: -1.0
R5: Tag: A2
R6: Tag:
             Busy: 0 Value: 4.0
             Busy: 0 Value: 6.0
R7: Tag:
             Busy: 0 Value: 5.0
R8: Tag:
R9: Tag:
             Busy: 0 Value: 6.0
R10: Tag:
             Busy: 0 Value: 11.0
R11: Tag: M2 Busy: 1 Value: -1.0
             Busy: 0 Value: -1.0
R12: Tag:
             Busy: 0 Value: -1.0
R13: Tag:
R14: Tag:
             Busy: 0 Value: -1.0
Memory:
M0: 0.0
M1: 1.0
M2: 2.0
M3: 0.0
M4: 3.0
M5: 0.0
M6: 4.0
M7: 0.0
M8: 5.0
M9: 6.0
M10: 0.0
M11: 0.0
M12: 0.0
M13: 0.0
M14: 0.0
Common Data Bus:
Tag: A1 Value: 5.0
Instructions To Write:
```

MUL R11, R7, R10

-----

Instruction to be written: MUL R11, R7, R10

Clock Cycle: 17 PC Value: 6

**Reservation Stations:** 

Adder:

Adder position0: Tag: A1 Start Cycle: -1 Execute End Cycle: -1 Busy: 0 Instruction Type: None Vj: Vk: Qj: Qk: A: Duration left: -1 Ready To Write: false Adder position1: Tag: A2 Start Cycle: -1 Execute End Cycle: -1 Busy: 1 Instruction Qk: A: Type: ADD Vj: 5.0 Vk: 66.0 Qj: Duration left: 4 Ready To Write: false Start Cycle: -1 Execute End Cycle: -1 Busy: 0 Instruction Adder position2: Tag: A3 A: Duration left: -1 Ready To Write: false Type: None Vi: Vk: Qi: Qk: Multiplier:

Multiplier position0:

Tag: M1 Start Cycle: -1 Execute End Cycle: -1 Busy: 0 Instruction Type: None Vj: Vk:

Qj: Qk: A: Duration left: -1 Ready To Write: false

Multiplier position1:

Tag: M2 Start Cycle: -1 Execute End Cycle: -1 Busy: 0 Instruction Type: None Vj: Vk:

Qj: Qk: A: Duration left: -1 Ready To Write: false

Load Buffers:

Load buffer position0:

Tag: L1 Busy: 0 Effective Address: -1 Start Cycle: -1 Execute End Cycle: -1 Duration left:

-1 Ready To Write: false

Load buffer position1:

Tag: L2 Busy: 0 Effective Address: -1 Start Cycle: -1 Execute End Cycle: -1 Duration left:

-1 Ready To Write: false

Load buffer position2:

Tag: L3 Busy: 0 Effective Address: -1 Start Cycle: -1 Execute End Cycle: -1 Duration left:

-1 Ready To Write: false

Store Buffers:

Store buffer position0:

Tag: S1 Busy: 0 Effective Address: -1 Start Cycle: -1 Execute End Cycle: -1 Duration left:

-1 Ready To Write: false

Store buffer position1:

Tag: S2 Busy: 0 Effective Address: -1 Start Cycle: -1 Execute End Cycle: -1 Duration left:

-1 Ready To Write: false

Store buffer position2:

Tag: S3 Busy: 0 Effective Address: -1 Start Cycle: -1 Execute End Cycle: -1 Duration left:

-1 Ready To Write: false

Register File:

Busy: 0 Value: -1.0 R0: Tag: R1: Tag: Busy: 0 Value: 1.0 Busy: 0 Value: 2.0 R2: Tag: R3: Tag: Busy: 0 Value: 2.0 R4: Tag: Busy: 0 Value: 3.0 Busy: 1 Value: -1.0 R5: Tag: A2 R6: Tag: Busy: 0 Value: 4.0 Busy: 0 Value: 6.0 R7: Tag:

```
R8: Tag:
             Busy: 0 Value: 5.0
R9: Tag:
             Busy: 0 Value: 6.0
R10: Tag:
             Busy: 0 Value: 11.0
             Busy: 0 Value: 66.0
R11: Tag:
             Busy: 0 Value: -1.0
R12: Tag:
             Busy: 0 Value: -1.0
R13: Tag:
R14: Tag:
             Busy: 0 Value: -1.0
Memory:
M0: 0.0
M1: 1.0
M2: 2.0
M3: 0.0
M4: 3.0
M5: 0.0
M6: 4.0
M7: 0.0
M8: 5.0
M9: 6.0
M10: 0.0
M11: 0.0
M12: 0.0
M13: 0.0
M14: 0.0
Common Data Bus:
Tag: M2 Value: 66.0
Instructions To Write:
Clock Cycle: 18
PC Value: 6
Reservation Stations:
Adder:
                            Start Cycle: -1 Execute End Cycle: -1 Busy: 0 Instruction
Adder position0: Tag: A1
Type: None Vj: Vk: Qj:
                              Qk:
                                    A: Duration left: -1
                                                           Ready To Write: false
Adder position1: Tag: A2
                            Start Cycle: 18 Execute End Cycle: 21 Busy: 1 Instruction
Type: ADD Vj: 5.0 Vk: 66.0
                                Qj:
                                     Qk: A:
                                                Duration left: 4
                                                                   Ready To Write: false
                            Start Cycle: -1 Execute End Cycle: -1 Busy: 0 Instruction
Adder position2: Tag: A3
Type: None Vj: Vk: Qj:
                             Qk: A: Duration left: -1
                                                           Ready To Write: false
Multiplier:
Multiplier position0:
Tag: M1 Start Cycle: -1 Execute End Cycle: -1 Busy: 0 Instruction Type: None Vj:
                                                                                  Vk:
                 Duration left: -1 Ready To Write: false
     Qk:
           A:
Multiplier position1:
Tag: M2 Start Cycle: -1 Execute End Cycle: -1 Busy: 0 Instruction Type: None Vj:
                                                                                  Vk:
                 Duration left: -1 Ready To Write: false
     Qk: A:
Load Buffers:
Load buffer position0:
```

Tag: L1 Busy: 0 Effective Address: -1 Start Cycle: -1 Execute End Cycle: -1 Duration left:

-1

Ready To Write: false

```
Load buffer position1:
Tag: L2 Busy: 0 Effective Address: -1 Start Cycle: -1 Execute End Cycle: -1 Duration left:
      Ready To Write: false
Load buffer position2:
Tag: L3 Busy: 0 Effective Address: -1 Start Cycle: -1 Execute End Cycle: -1 Duration left:
      Ready To Write: false
Store Buffers:
Store buffer position0:
Tag: S1 Busy: 0 Effective Address: -1 Start Cycle: -1 Execute End Cycle: -1 Duration left:
-1
      Ready To Write: false
Store buffer position1:
Tag: S2 Busy: 0 Effective Address: -1 Start Cycle: -1 Execute End Cycle: -1 Duration left:
-1
      Ready To Write: false
Store buffer position2:
Tag: S3 Busy: 0 Effective Address: -1 Start Cycle: -1 Execute End Cycle: -1 Duration left:
-1
      Ready To Write: false
Register File:
R0: Tag:
             Busy: 0 Value: -1.0
             Busy: 0 Value: 1.0
R1: Tag:
             Busy: 0 Value: 2.0
R2: Tag:
             Busy: 0 Value: 2.0
R3: Tag:
R4: Tag:
             Busy: 0 Value: 3.0
R5: Tag: A2
              Busy: 1 Value: -1.0
R6: Tag:
             Busy: 0 Value: 4.0
R7: Tag:
             Busy: 0 Value: 6.0
             Busy: 0 Value: 5.0
R8: Tag:
             Busy: 0 Value: 6.0
R9: Tag:
R10: Tag:
             Busy: 0 Value: 11.0
R11: Tag:
             Busy: 0 Value: 66.0
R12: Tag:
             Busy: 0 Value: -1.0
R13: Tag:
             Busy: 0 Value: -1.0
             Busy: 0 Value: -1.0
R14: Tag:
Memory:
M0: 0.0
M1: 1.0
M2: 2.0
M3: 0.0
M4: 3.0
M5: 0.0
M6: 4.0
M7: 0.0
M8: 5.0
M9: 6.0
```

M10: 0.0 M11: 0.0 M12: 0.0 M13: 0.0 M14: 0.0 Common Data Bus: Tag: M2 Value: 66.0 Instructions To Write:

-----

Clock Cycle: 19 PC Value: 6

Reservation Stations:

Adder:

Adder position0: Tag: A1 Start Cycle: -1 Execute End Cycle: -1 Busy: 0 Instruction Type: None Vj: Vk: Qj: Qk: A: Duration left: -1 Ready To Write: false Adder position1: Tag: A2 Start Cycle: 18 Execute End Cycle: 21 Busy: 1 Instruction Type: ADD Vj: 5.0 Vk: 66.0 Duration left: 3 Ready To Write: false Qi: Qk: A: Adder position2: Tag: A3 Start Cycle: -1 Execute End Cycle: -1 Busy: 0 Instruction Type: None Vj: Vk: Qj: Qk: A: Duration left: -1 Ready To Write: false Multiplier:

Multiplier position0:

Tag: M1 Start Cycle: -1 Execute End Cycle: -1 Busy: 0 Instruction Type: None Vj: Vk:

Qj: Qk: A: Duration left: -1 Ready To Write: false

Multiplier position1:

Tag: M2 Start Cycle: -1 Execute End Cycle: -1 Busy: 0 Instruction Type: None Vj: Vk:

Qi: Qk: A: Duration left: -1 Ready To Write: false

Load Buffers:

Load buffer position0:

Tag: L1 Busy: 0 Effective Address: -1 Start Cycle: -1 Execute End Cycle: -1 Duration left:

-1 Ready To Write: false

Load buffer position1:

Tag: L2 Busy: 0 Effective Address: -1 Start Cycle: -1 Execute End Cycle: -1 Duration left:

-1 Ready To Write: false

Load buffer position2:

Tag: L3 Busy: 0 Effective Address: -1 Start Cycle: -1 Execute End Cycle: -1 Duration left:

-1 Ready To Write: false

Store Buffers:

Store buffer position0:

Tag: S1 Busy: 0 Effective Address: -1 Start Cycle: -1 Execute End Cycle: -1 Duration left:

-1 Ready To Write: false

Store buffer position1:

Tag: S2 Busy: 0 Effective Address: -1 Start Cycle: -1 Execute End Cycle: -1 Duration left:

-1 Ready To Write: false

Store buffer position2:

Tag: S3 Busy: 0 Effective Address: -1 Start Cycle: -1 Execute End Cycle: -1 Duration left:

-1 Ready To Write: false

Register File:

R0: Tag: Busy: 0 Value: -1.0
R1: Tag: Busy: 0 Value: 1.0
R2: Tag: Busy: 0 Value: 2.0
R3: Tag: Busy: 0 Value: 2.0
R4: Tag: Busy: 0 Value: 3.0
R5: Tag: A2 Busy: 1 Value: -1.0

```
R6: Tag:
             Busy: 0 Value: 4.0
R7: Tag:
             Busy: 0 Value: 6.0
             Busy: 0 Value: 5.0
R8: Tag:
             Busy: 0 Value: 6.0
R9: Tag:
             Busy: 0 Value: 11.0
R10: Tag:
R11: Tag:
             Busy: 0 Value: 66.0
R12: Tag:
             Busy: 0 Value: -1.0
R13: Tag:
             Busy: 0 Value: -1.0
R14: Tag:
             Busy: 0 Value: -1.0
Memory:
M0: 0.0
M1: 1.0
M2: 2.0
M3: 0.0
M4: 3.0
M5: 0.0
M6: 4.0
M7: 0.0
M8: 5.0
M9: 6.0
M10: 0.0
M11: 0.0
M12: 0.0
M13: 0.0
M14: 0.0
Common Data Bus:
Tag: M2 Value: 66.0
Instructions To Write:
Clock Cycle: 20
PC Value: 6
Reservation Stations:
Adder:
Adder position0: Tag: A1
                             Start Cycle: -1 Execute End Cycle: -1 Busy: 0 Instruction
Type: None Vj: Vk: Qj:
                              Qk:
                                    A: Duration left: -1
                                                           Ready To Write: false
Adder position1: Tag: A2
                             Start Cycle: 18 Execute End Cycle: 21 Busy: 1 Instruction
Type: ADD Vj: 5.0 Vk: 66.0
                                                Duration left: 2
                                                                   Ready To Write: false
                                Qi:
                                      Qk: A:
Adder position2: Tag: A3
                            Start Cycle: -1 Execute End Cycle: -1 Busy: 0 Instruction
Type: None Vj: Vk: Qj:
                                    A: Duration left: -1
                                                            Ready To Write: false
                              Qk:
Multiplier:
Multiplier position0:
Tag: M1 Start Cycle: -1 Execute End Cycle: -1 Busy: 0 Instruction Type: None Vi:
                                                                                   Vk:
           A:
                 Duration left: -1 Ready To Write: false
     Qk:
Multiplier position1:
Tag: M2 Start Cycle: -1 Execute End Cycle: -1 Busy: 0 Instruction Type: None Vj:
                                                                                   Vk:
     Qk: A:
                 Duration left: -1 Ready To Write: false
Qi:
Load Buffers:
Load buffer position0:
```

```
Tag: L1 Busy: 0 Effective Address: -1 Start Cycle: -1 Execute End Cycle: -1 Duration left:
-1
      Ready To Write: false
Load buffer position1:
Tag: L2 Busy: 0 Effective Address: -1 Start Cycle: -1 Execute End Cycle: -1 Duration left:
-1
      Ready To Write: false
Load buffer position2:
Tag: L3 Busy: 0 Effective Address: -1 Start Cycle: -1 Execute End Cycle: -1 Duration left:
      Ready To Write: false
Store Buffers:
Store buffer position0:
Tag: S1 Busy: 0 Effective Address: -1 Start Cycle: -1 Execute End Cycle: -1 Duration left:
      Ready To Write: false
Store buffer position1:
Tag: S2 Busy: 0 Effective Address: -1 Start Cycle: -1 Execute End Cycle: -1 Duration left:
      Ready To Write: false
Store buffer position2:
Tag: S3 Busy: 0 Effective Address: -1 Start Cycle: -1 Execute End Cycle: -1 Duration left:
      Ready To Write: false
Register File:
R0: Tag:
             Busy: 0 Value: -1.0
R1: Tag:
             Busy: 0 Value: 1.0
R2: Tag:
             Busy: 0 Value: 2.0
R3: Tag:
             Busy: 0 Value: 2.0
R4: Tag:
             Busy: 0 Value: 3.0
R5: Tag: A2
              Busy: 1 Value: -1.0
R6: Tag:
             Busy: 0 Value: 4.0
R7: Tag:
             Busy: 0 Value: 6.0
R8: Tag:
             Busy: 0 Value: 5.0
R9: Tag:
             Busy: 0 Value: 6.0
R10: Tag:
             Busy: 0 Value: 11.0
R11: Tag:
             Busy: 0 Value: 66.0
R12: Tag:
             Busy: 0 Value: -1.0
R13: Tag:
             Busy: 0 Value: -1.0
R14: Tag:
             Busy: 0 Value: -1.0
Memory:
M0: 0.0
M1: 1.0
M2: 2.0
M3: 0.0
M4: 3.0
M5: 0.0
M6: 4.0
M7: 0.0
M8: 5.0
M9: 6.0
M10: 0.0
M11: 0.0
```

M12: 0.0

M13: 0.0 M14: 0.0

Common Data Bus: Tag: M2 Value: 66.0 Instructions To Write:

\_\_\_\_\_

Clock Cycle: 21 PC Value: 6

Reservation Stations:

Adder:

Adder position0: Tag: A1 Start Cycle: -1 Execute End Cycle: -1 Busy: 0 Instruction A: Duration left: -1 Ready To Write: false Type: None Vi: Vk: Qi: Adder position1: Tag: A2 Start Cycle: 18 Execute End Cycle: 21 Busy: 1 Instruction Type: ADD Vj: 5.0 Vk: 66.0 Qk: A: Duration left: 1 Ready To Write: true Qj: Adder position2: Tag: A3 Start Cycle: -1 Execute End Cycle: -1 Busy: 0 Instruction Type: None Vj: Vk: Qj: Qk: A: Duration left: -1 Ready To Write: false Multiplier:

Multiplier position0:

Tag: M1 Start Cycle: -1 Execute End Cycle: -1 Busy: 0 Instruction Type: None Vj: Vk:

Qj: Qk: A: Duration left: -1 Ready To Write: false

Multiplier position1:

Tag: M2 Start Cycle: -1 Execute End Cycle: -1 Busy: 0 Instruction Type: None Vj: Vk:

Qj: Qk: A: Duration left: -1 Ready To Write: false

Load Buffers:

Load buffer position0:

Tag: L1 Busy: 0 Effective Address: -1 Start Cycle: -1 Execute End Cycle: -1 Duration left:

-1 Ready To Write: false

Load buffer position1:

Tag: L2 Busy: 0 Effective Address: -1 Start Cycle: -1 Execute End Cycle: -1 Duration left:

-1 Ready To Write: false

Load buffer position2:

Tag: L3 Busy: 0 Effective Address: -1 Start Cycle: -1 Execute End Cycle: -1 Duration left:

-1 Ready To Write: false

Store Buffers:

Store buffer position0:

Tag: S1 Busy: 0 Effective Address: -1 Start Cycle: -1 Execute End Cycle: -1 Duration left:

-1 Ready To Write: false

Store buffer position1:

Tag: S2 Busy: 0 Effective Address: -1 Start Cycle: -1 Execute End Cycle: -1 Duration left:

-1 Ready To Write: false

Store buffer position2:

Tag: S3 Busy: 0 Effective Address: -1 Start Cycle: -1 Execute End Cycle: -1 Duration left:

-1 Ready To Write: false

Register File:

R0: Tag: Busy: 0 Value: -1.0 R1: Tag: Busy: 0 Value: 1.0 R2: Tag: Busy: 0 Value: 2.0 R3: Tag: Busy: 0 Value: 2.0

```
R4: Tag:
             Busy: 0 Value: 3.0
R5: Tag: A2
              Busy: 1 Value: -1.0
             Busy: 0 Value: 4.0
R6: Tag:
             Busy: 0 Value: 6.0
R7: Tag:
             Busy: 0 Value: 5.0
R8: Tag:
R9: Tag:
             Busy: 0 Value: 6.0
R10: Tag:
             Busy: 0 Value: 11.0
R11: Tag:
             Busy: 0 Value: 66.0
R12: Tag:
             Busy: 0 Value: -1.0
R13: Tag:
             Busy: 0 Value: -1.0
R14: Tag:
             Busy: 0 Value: -1.0
Memory:
M0: 0.0
M1: 1.0
M2: 2.0
M3: 0.0
M4: 3.0
M5: 0.0
M6: 4.0
M7: 0.0
M8: 5.0
M9: 6.0
M10: 0.0
M11: 0.0
M12: 0.0
M13: 0.0
M14: 0.0
Common Data Bus:
Tag: M2 Value: 66.0
Instructions To Write:
ADD R5, R5, R11
Instruction to be written: ADD R5, R5, R11
Clock Cycle: 22
PC Value: 6
Reservation Stations:
Adder:
Adder position0: Tag: A1
                             Start Cycle: -1 Execute End Cycle: -1 Busy: 0 Instruction
Type: None Vi:
                                    A: Duration left: -1
                                                            Ready To Write: false
                  Vk:
                        Qj:
                              Qk:
Adder position1: Tag: A2
                             Start Cycle: -1 Execute End Cycle: -1 Busy: 0 Instruction
Type: None Vj:
                                    A: Duration left: -1
                                                            Ready To Write: false
                  Vk:
                        Qj:
                              Qk:
Adder position2: Tag: A3
                             Start Cycle: -1 Execute End Cycle: -1 Busy: 0 Instruction
Type: None Vj:
                                                            Ready To Write: false
                  Vk:
                        Qj:
                              Qk:
                                    A: Duration left: -1
Multiplier:
Multiplier position0:
Tag: M1 Start Cycle: -1 Execute End Cycle: -1 Busy: 0 Instruction Type: None Vj:
                                                                                    Vk:
                  Duration left: -1 Ready To Write: false
Qj:
     Qk:
           A:
Multiplier position1:
```

```
Tag: M2 Start Cycle: -1 Execute End Cycle: -1 Busy: 0 Instruction Type: None Vj: Vk:
Qj:
     Qk:
           A:
                  Duration left: -1 Ready To Write: false
Load Buffers:
Load buffer position0:
Tag: L1 Busy: 0 Effective Address: -1 Start Cycle: -1 Execute End Cycle: -1 Duration left:
      Ready To Write: false
Load buffer position1:
Tag: L2 Busy: 0 Effective Address: -1 Start Cycle: -1 Execute End Cycle: -1 Duration left:
      Ready To Write: false
Load buffer position2:
Tag: L3 Busy: 0 Effective Address: -1 Start Cycle: -1 Execute End Cycle: -1 Duration left:
      Ready To Write: false
Store Buffers:
Store buffer position0:
Tag: S1 Busy: 0 Effective Address: -1 Start Cycle: -1 Execute End Cycle: -1 Duration left:
      Ready To Write: false
-1
Store buffer position1:
Tag: S2 Busy: 0 Effective Address: -1 Start Cycle: -1 Execute End Cycle: -1 Duration left:
      Ready To Write: false
-1
Store buffer position2:
Tag: S3 Busy: 0 Effective Address: -1 Start Cycle: -1 Execute End Cycle: -1 Duration left:
      Ready To Write: false
-1
Register File:
R0: Tag:
             Busy: 0 Value: -1.0
R1: Tag:
             Busy: 0 Value: 1.0
R2: Tag:
             Busy: 0 Value: 2.0
             Busy: 0 Value: 2.0
R3: Tag:
             Busy: 0 Value: 3.0
R4: Tag:
R5: Tag:
             Busy: 0 Value: 71.0
             Busy: 0 Value: 4.0
R6: Tag:
R7: Tag:
             Busy: 0 Value: 6.0
R8: Tag:
             Busy: 0 Value: 5.0
R9: Tag:
             Busy: 0 Value: 6.0
R10: Tag:
             Busy: 0 Value: 11.0
R11: Tag:
             Busy: 0 Value: 66.0
R12: Tag:
             Busy: 0 Value: -1.0
             Busy: 0 Value: -1.0
R13: Tag:
R14: Tag:
             Busy: 0 Value: -1.0
Memory:
M0: 0.0
M1: 1.0
M2: 2.0
M3: 0.0
M4: 3.0
M5: 0.0
M6: 4.0
M7: 0.0
```

M8: 5.0

M9: 6.0 M10: 0.0 M11: 0.0 M12: 0.0 M13: 0.0 M14: 0.0

Common Data Bus: Tag: A2 Value: 71.0 Instructions To Write:

\_\_\_\_\_